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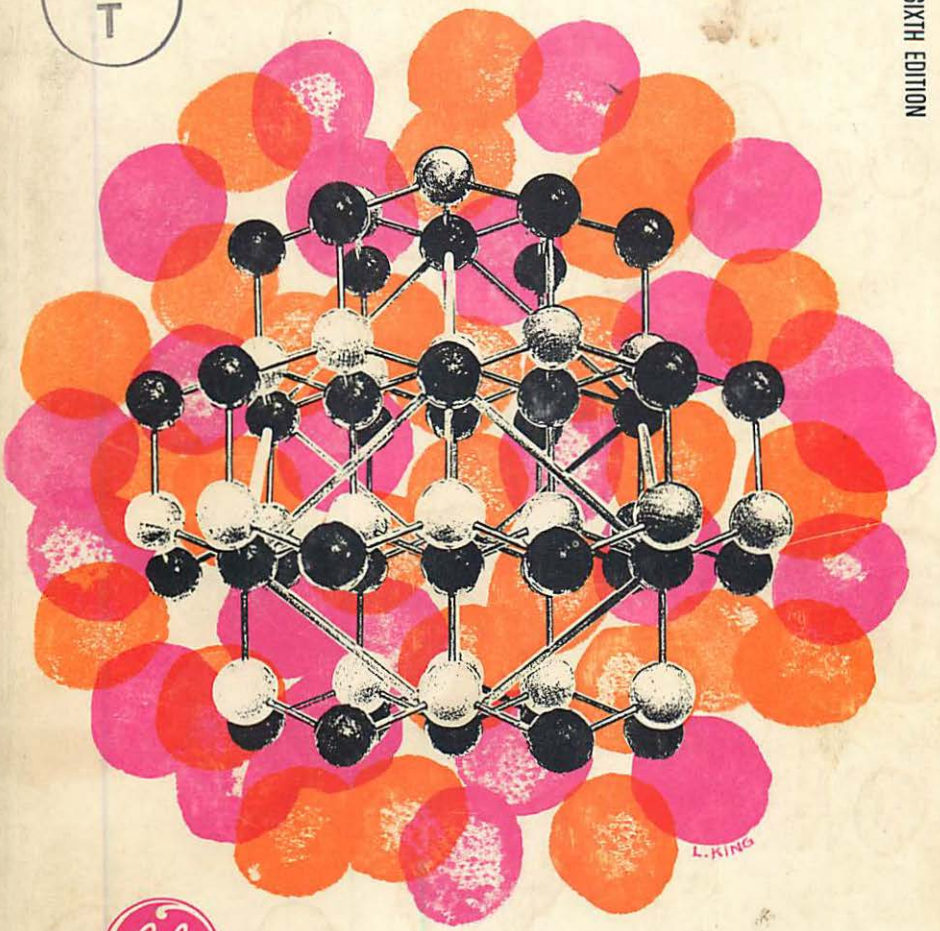


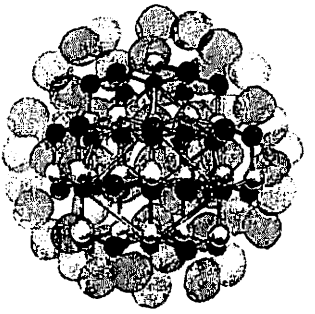

# TRANSISTOR MANUAL

## INCLUDING SIGNAL DIODES

APPLICATIONS · CIRCUITS · SPECIFICATIONS

# TRANSISTOR MANUAL

SIXTH EDITION

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# CONTENTS

# FOREWORD

During the past year and a half, many new processes and developments in semiconductors have been introduced. The Sixth Edition of the General Electric Transistor Manual has been completely rewritten and expanded by over 100 pages to include these many improvements.

New processes and developments have been responsible for the creation of totally new product lines. These new lines include the General Electric Family of Silicon Planar Epitaxial Passivated Transistors (PEP), the NPNP Silicon Controlled Switch, PEP Controlled Conductance Diodes with ultra fast switching speeds, and many other new transistor and diode types. These new devices, with their unique characteristics have opened up many new areas of applications and have ultimately produced higher reliability, less complex circuitry and lower cost.

At the same time, General Electric has been actively engaged in a major program to increase reliability in semiconductor devices by several orders of magnitude. The MINUTEMAN Product Improvement Program is designed to accomplish the reliability objective of 0.001% failure rate per 1,000 hours. While this product improvement program is directed specifically to the MINUTEMAN types, process improvements developed and confirmed in this activity are fed into other product manufacturing lines. This assures constantly improved devices for circuit applications where reliability is of utmost importance.

The addition of all these latest improvements to your Sixth Edition General Electric Transistor Manual will assure its continued usefulness as your handy reference guide.

H. Brainard Fancher

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General Manager
Semiconductor Products Department
Syracuse, New York

# SEMICONDUCTOR THEORY

CHAPTER 1

In 1833, Michael Faraday, the famed English scientist, made what is perhaps the first significant contribution to semiconductor research. During an experiment with silver sulphide Faraday observed that its resistance varied inversely with temperature. This was in sharp contrast with other conductors where an increase in temperature caused an increase in resistance and, conversely, a decrease in temperature caused a decrease in resistance. Faraday's observation of negative temperature coefficient of resistance, occurring as it did over 100 years before the birth of the practical transistor, may well have been the "gleam in the eye" of the future.

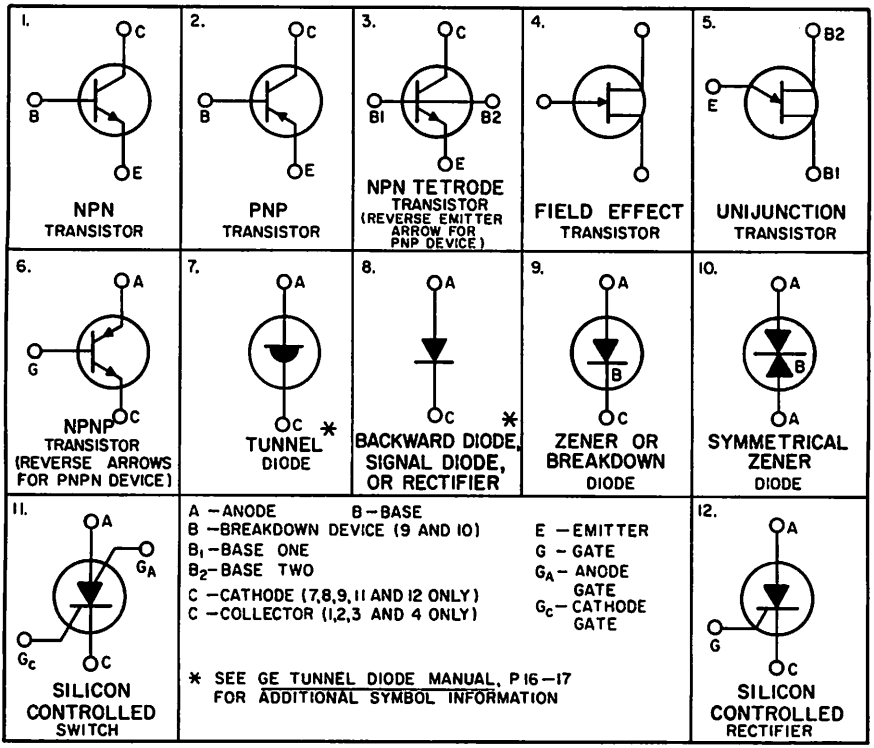
For since its invention in 1948 the transistor has played a steadily increasing part not only in the electronics industry, but in the lives of the people as well. First used in hearing aids and portable radios, it is now used in every existing branch of electronics. Transistors are used by the thousands in automatic telephone exchanges, digital computors, industrial and military control systems, and telemetering transmitters for satellites. A modern satellite may contain as many as 2500 transistors and 3500 diodes as part of a complex control and signal system. In contrast, but equally as impressive, is the two transistor "pacemaker," a tiny electronic pulser. When imbedded in the human chest and connected to the heart the pacemaker helps the ailing heart patient live a nearly normal life. What a wonderful device is the tiny transistor. In only a few short years it has proved its worth – from crystal set to regulator of the human heart.

But it is said that progress moves slowly. And this is perhaps true of the first hundred years of semiconductor research, where time intervals between pure research and practical application were curiously long. But certainly this cannot be said of the years that followed the invention of the transistor. For since 1948 the curve of semiconductor progress has been moving swiftly and steadily upward. The years to come promise an even more spectacular rise. Not only will present frequency and power limitations be surpassed but, in time, new knowledge of existing semiconductor materials . . . new knowledge of *new* materials . . . improved methods of device fabrication . . . the micro-miniaturization of semiconductor devices . . . complete micro-circuits . . . all, will spread forth from the research and engineering laboratories to further influence and improve our lives.

Already, such devices as the tunnel diode, the mesa transistor, and the high-speed diode can perform with ease well into the UHF range; transistors, that only a short time ago were limited to producing but a few milliwatts of power, can today produce thousands upon thousands of milliwatts of power; special transistors and diodes such as the unijunction transistor, the high-speed diode, and the tunnel diode can simplify and make more economical normally complex and expensive timing and switching circuits. Intricate and sophisticated circuitry that normally would require excessive space, elaborate cooling equipment, and expensive power supply components can today be designed and built to operate inherently cooler within a substantially smaller space, and with less imposing power components, by designing with semiconductors. In almost all areas of electronics the semiconductors have brought immense increases in efficiency and in reliability.

In the short span of years since the advent of the transistor a variety of semiconductor devices have been developed. Symbols representing these devices are shown

in Figure 1.1. Numerous individual types are today commercially available from each category to answer the needs of the professional electronic equipment designer, the radio amateur, and the experimenter. It goes without saying that with time more and newer devices will be added.




**STANDARD SYMBOLS FOR SEMICONDUCTOR DEVICES**

**Figure 1.1**

For the most part this chapter is concerned with the terminology and theory of semiconductors as both pertain to diodes and junction transistors. The variety of semiconductor devices available preclude a complete and exhaustive treatment of theory and characteristics for all types. Such devices as the silicon controlled rectifier and the tunnel diode are well covered in other General Electric Manuals;* treatment of the unijunction transistor will be found in Chapter 13 of this manual. Other pertinent literature will be found in Chapter 21.

Although a complete understanding of the physical concepts and operational theory of the transistor and diode are not necessary to design and construct successful transistor circuits, they can be helpful. The professional electronics engineer, the radio amateur, and the serious experimenter can all obtain practical and rewarding benefits from a general understanding of the basic physics and theory of semiconductors. Such

*See Reference List

understanding will often aid in solving special circuit problems, will help in understanding and using the newer semiconductor devices as they become available, and surely will help clarify much of the technical literature that more and more abounds with semiconductor terminology.

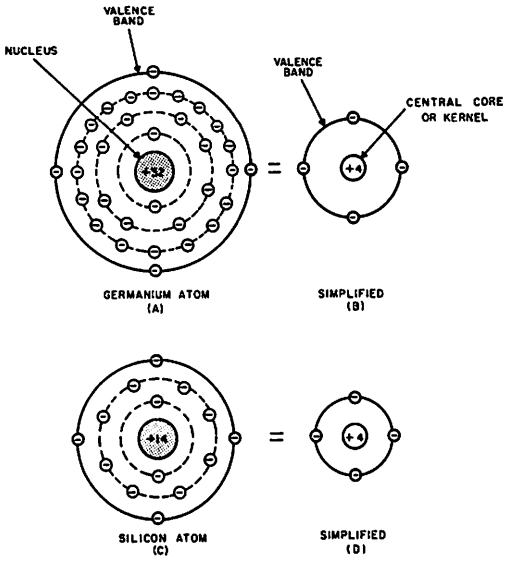
## SEMICONDUCTORS

Semiconductor technology is usually referred to as *solid-state*. This suggests, of course, that the *matter* used in the fabrication of the various devices is a solid, as opposed to liquid or gaseous matter – or even the near perfect vacuum as found in the thermionic tube – and that conduction of electricity occurs within solid material. "But how," it might be asked, "can electrical charges move through solid material as they must, if electrical conduction is to take place?" With some thought the answer becomes obvious: the so-called solid is *not* solid, but only partially so. In the microcosmos, the world of the atom, there is mostly space. It is from close study of this intricate and complicated "little world," made up mostly of space, that scientists have uncovered the basic ingredients that make up solid state devices – the *semiconductors*. Transistors and diodes, as we know them today, are made from semiconductors, so-called because they lie between the metals and the insulators in their ability to conduct electricity. There are many semiconductors, but none quite as popular at the present time as germanium and silicon, both of which are hard, brittle crystals by nature. In their natural state they are impure in contrast, for example, to the nearly pure crystalline structure of high quality diamond. In terms of electrical resistance the relationship of each to well known conductors and insulators is shown in Chart 1.

| MATERIAL | RESISTANCE IN OHMS PER CENTIMETER CUBE ($R/CM^3$) | CATEGORY |
|---|---|---|
| Silver<br>Aluminum | $10^{-6}$<br>$10^{-5}$ | Conductor |
| Pure Germanium<br>Pure Silicon | 50-60<br>50,000-60,000 | Semiconductor |
| Mica<br>Polyethlene | $10^{12}$-$10^{13}$<br>$10^{15}$-$10^{16}$ | Insulator |

**Chart 1**

Because of impurities the $R/CM^3$ for each in its natural state is much less than an ohm, depending on the degree of impurity present. Material for use in most practical transistors requires $R/CM^3$ values in the neighborhood of 2 ohms/$CM^3$. The ohmic value of pure germanium and silicon, as can be seen from Chart 1, is much higher. Electrical conduction then, is quite dependent on the impurity content of the material, and precise control of impurities is the most important requirement in the production of transistors. Another important requirement for almost all semiconductor devices is that single crystal material be used in their fabrication. To better appreciate the construction of single crystals made from germanium and silicon, some attention must be first given to the makeup of their individual atoms. Figure 1.2(A) and (C) show both as represented by Bohr models of atomic structure, so named after the Danish physicist Neils Bohr.




**BOHR MODELS OF GERMANIUM AND SILICON ATOMS**

**Figure 1.2**

Germanium is shown to possess a positively charged nucleus of +32 while the silicon atom's nucleus possesses a positive charge of +14. In each case the total positive charge of the nucleus is equalized by the total effective negative charge of the electrons. This equalization of charges results in the atom possessing an effective charge that is neither positive nor negative, but neutral. The electrons, traveling within their respective orbits, possess energy since they are a definite mass in motion.* Each electron in its relationship with its parent nucleus thus exhibits an energy value and functions at a definite and distinct energy level. This energy level is dictated by the electron's momentum and its physical proximity to the nucleus. The closer the electron to the nucleus the greater the holding influence of the nucleus on the electron and the greater the energy required for the electron to break loose and become free. Likewise, the further away the electron from the nucleus the less its influence on the electron.

Outer orbit electrons can therefore be said to be stronger than inner orbit electrons because of their ability to break loose from the parent atom. For this reason they are called *valence electrons,* from the Latin valere, to be strong. The weaker inner orbital electrons and the nucleus combine to make a *central core* or *kernel.* The outer orbit in which valence electrons exist is called the *valence band* or *valence shell.* It is the electrons from this band that are dealt with in the practical discussion of transistor physics, as it is rare for inner orbital electrons – those existing at energy levels below the valence band – to break loose and enter into transistor action. With this in mind the complex atoms of germanium and silicon as shown in (A) and (C) of Figure 1.2 can be simplified to those models shown in (B) and (C) and used in further discussion.

The most important characteristic of most atoms is their valency, the ability of the valence band electrons of one atom to bond together with the valence bands of other atoms. This important and basic atomic action can be visualized as shown in Figure 1.3.

*Mass of electron = $9.108 \times 10^{-28}$ gram.

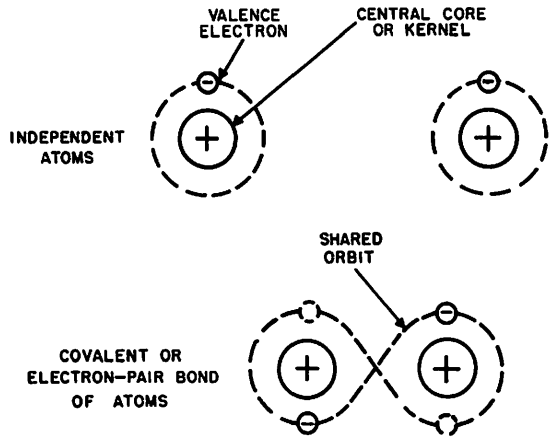
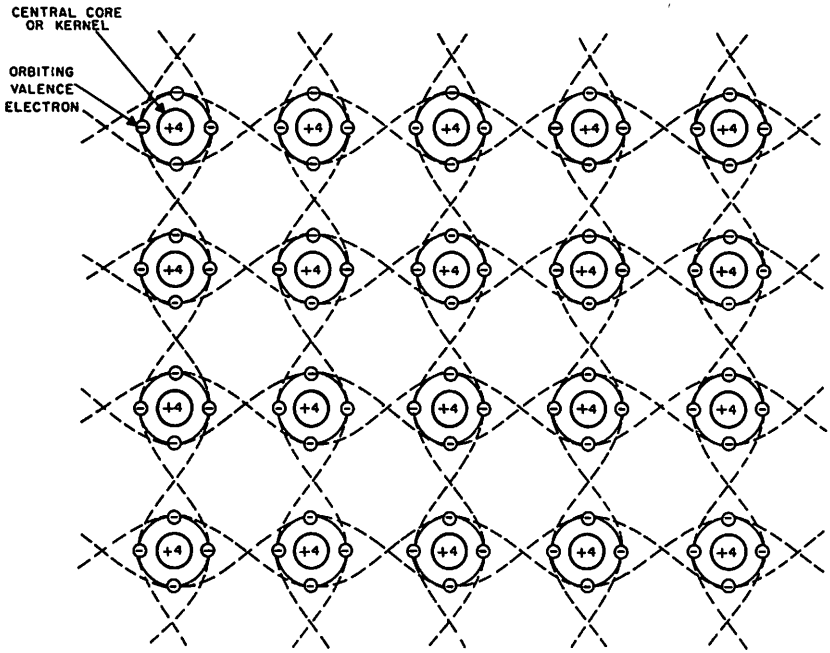



**Figure 1.3**

Through orbit sharing by interchange of orbital position the electrons become mutually related to one another and to the parent cores, binding the two atoms together in a strong spaced locking action. A *covalent bond* or *electron-pair bond* is said to exist. This simple concept when applied to germanium and silicon crystals will naturally result in a more involved action, one the reader may find at first difficult to visualize.

In the structure of pure germanium and pure silicon single crystals the molecules are in an ordered array. This orderly arrangement is descriptively referred to as a diamond lattice, since the atoms are in a lattice-like structure as found in high quality diamond crystals. A definite and regular pattern exists among the atoms due to space equality. For equal space to exist between all atoms in such a structure, however, the following has been shown to be true: the greatest number of atoms that can neighbor any single atom at equal distance and still be equadistant from one another is *four*. Figure 1.4 is a two dimensional presentation of a germanium lattice structure showing covalent bonding of atoms. (Better understanding and more clear spatial visualization of Figure 1.4 may be had by construction of a three dimensional diamond lattice model using the technique shown in Figure 1.5). Figure 1.4 could just as well represent a silicon lattice since the silicon atom also contains four electrons in its outer valence band. With all valence electrons in covalent bondage no excess electrons are free to drift throughout the crystal as electrical charge carriers. In theory, this represents a perfect and stable diamond lattice of single crystal structure and, ideally, would be a perfect insulator.

But such perfect single crystals are not possible in practice. Even in highly purified crystals, charge carriers are present to freely move about, making the crystal a poor conductor rather than a non-conductor. At the start of the manufacturing process modern and reliable transistors require as near perfect single crystal material as possible. That is, crystal that exhibits an orderly arrangement of equally spaced atoms, free from structural irregularities such as *grains* and *grain boundaries* as found in polycrystalline structures. Polycrystals do not readily allow charge carriers to freely flow and are impractical to reproduce with any regularity. Futhermore, surface structure varies considerably from crystal to crystal and makes reproduction of transistors to definite specifications difficult.




**TWO DIMENSIONAL GERMANIUM LATTICE STRUCTURE**

**Figure 1.4**

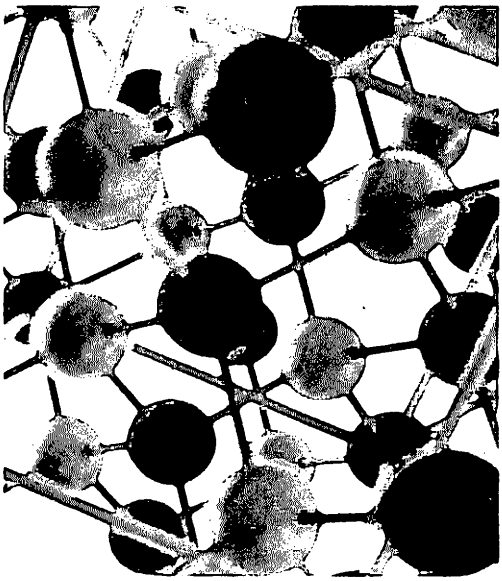


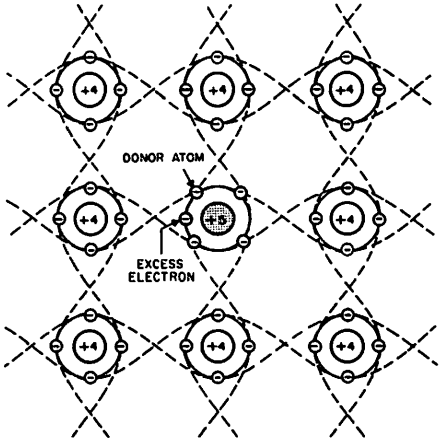
**Figure 1.5**

## CONDUCTION

As already mentioned, to be of practical use transistors require crystal material of greater conductivity (lower $R/CM^3$) than found in highly purified germanium and silicon. The conductivity can be increased by either heating the crystal or by adding other types of materials *(impurities)* to the crystal when it is formed.

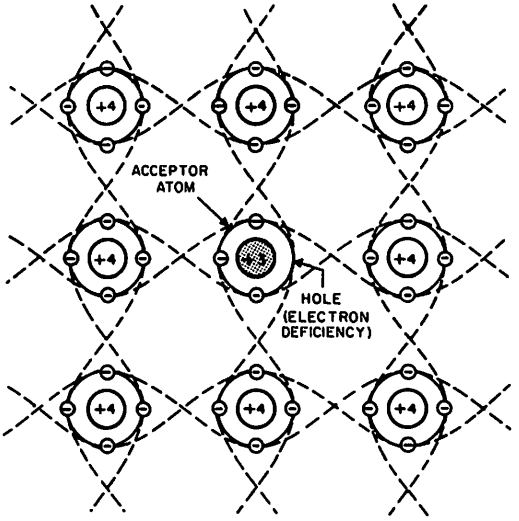
Heating the crystal will cause vibration of the atoms which form the crystal. Occasionally one of the valence electrons will acquire enough energy *(ionization energy)* to break away from its parent atom and move through the crystal. When the parent atom loses an electron it will assume a positive charge equal in magnitude to the charge of the electron. Once an atom has lost an electron it can acquire an electron from one of its neighboring atoms. This neighboring atom may in turn acquire an electron from one of its neighbors. Thus it is evident that each *free* electron which results from the breaking of a covalent bond will produce an electron deficiency which can move through the crystal as readily as the free electron itself. It is convenient to consider these electron deficiencies as particles which have positive charges and which are called *holes.* Each time an electron is generated by breaking a covalent bond a hole is generated at the same time. This process is known as the *thermal generation* of *hole-electron pairs.* The average time either carrier exists as a free carrier is known as *lifetime.* If a hole and a free electron collide, the electron will fill the electron deficiency which the hole represents and both the hole and electron will cease to exist as free charge carriers. This process is known as *recombination.*

Conductivity can also be increased by adding impurities to the semiconductor crystal when it is formed. These impurities may be *donors,* such as arsenic which "donates" extra free electrons to the crystal since each arsenic atom contains five electrons in its valence band; or *acceptors,* such as aluminum which "accepts" electrons from the crystal to produce free holes since each aluminum atom contains only three electrons in its valence band. A donor atom, which has five valence electrons, takes the place of a semiconductor atom in the crystal structure. Four of the five valence electrons are used to form covalent bonds with the neighboring semiconductor atoms. The fifth electron is easily freed from the atom and can move through the crystal. The donor atom assumes a positive charge, but remains fixed in the crystal. A semiconductor which contains donor atoms is called an *n-type* semiconductor since conduction occurs by virtue of free electrons (negative charge). A two dimensional model of n-type semiconductor is shown in Figure 1.6.




**N-TYPE SEMICONDUCTOR**
**Figure 1.6**

An acceptor atom, which has three valence electrons, can also take the place of a semiconductor atom in the crystal structure. All three of the valence electrons are used to form covalent bonds with the neighboring atoms. The fourth electron which is needed can be acquired from a neighboring atom, thus giving the acceptor atom a negative charge and producing a free hole in the crystal. A semiconductor which contains acceptor atoms is called a *p-type* semiconductor since conduction occurs by virtue of free holes in the crystal (positive charge). A two dimensional model of p-type semiconductor is shown in Figure 1.7.




**P-TYPE SEMICONDUCTOR**
**Figure 1.7**

To summarize, solid-state conduction takes place by means of free holes and free electrons *(carriers)* in semiconductor crystals. These holes or electrons may originate either from donor or acceptor impurities in the crystal, or from the thermal generation of hole-electron pairs. During the manufacture of the crystal it is possible to control conductivity, and make the crystal either n-type or p-type by adding controlled amounts of donor or acceptor impurities. A variety of such impurities are shown in Chart 2. On the other hand, thermally generated hole-electron pairs cannot be controlled other than by varying the temperature of the crystal.

## SPACE CHARGE NEUTRALITY

One of the most important principles involved in the operation of semiconductor devices is the *principle of space charge neutrality.* In simple terms, this principle states that the total number of positive charges (holes plus donor atoms) in any region of a semiconductor must equal the total number of negative charges (electrons plus acceptor atoms) in the same region provided that there are no large differences in voltage within the region. Use of this principle can frequently result in a simpler and more accurate interpretation of the operation of semiconductor devices. For example, in explaining the characteristics of an n-type semiconductor it is usually stated that the function of the donor atoms is to produce free electrons in the crystal. However, using the principle of space charge neutrality it is more accurate to say that the function of the donor atoms is to provide positive charges within the crystal which permit an equal number of free electrons to flow through the crystal.

| ELEMENT (SYMBOL) | GROUP IN PERIODIC TABLE | NUMBER VALENCE ELECTRONS | APPLICATIONS IN SEMICONDUCTOR DEVICES |
|---|---|---|---|
| boron (B)<br>aluminum (Al)<br>gallium (Ga)<br>indium (In) | III | 3 | acceptor elements, form p-type semiconductors, each atom substitutes for a Ge or Si atom in the semiconductor crystal and can take on or accept an extra electron thus producing a hole |
| germanium (Ge)<br>silicon (Si) | IV | 4 | basic semiconductor materials, used in crystal form with controlled amounts of donor or acceptor impurities |
| phosphorus (P)<br>arsenic (As)<br>antimony (Sb) | V | 5 | donor elements, form n-type semiconductors, each atom substitutes for a Ge or Si atom in the semiconductor crystal and can give up or donate an extra electron to the crystal |

**MATERIALS USED IN THE CONSTRUCTION OF TRANSISTORS AND OTHER SEMICONDUCTOR DEVICES**

**Chart 2**

## DIFFUSION AND DRIFT

Carriers can move through a semiconductor by two different mechanisms: diffusion or drift. *Diffusion* occurs whenever there is a difference in the concentration of the carriers in any adjacent regions of the crystal. The carriers have a random motion owing to the temperature of the crystal so that carriers will move in a random fashion from one region to another. However, more carriers will move from the region of higher concentration to the region of lower concentration than will move in the opposite direction. This is shown in Figure 1.8.

*Drift* of carriers occurs whenever there is a difference in voltage between one region of the semiconductor and another. The voltage difference produces a force on the carriers causing the holes to move toward the more negative voltage and the electrons to move toward the more positive voltage. The mechanism of drift is illustrated in Figure 1.9 for both n-type and p-type semiconductors. For the n-type material, the electrons enter the semiconductor at the lower electrode, move upwards through the semiconductor and leave through the upper electrode, passing then through the wire to the positive terminal of the battery. Note that in accordance with the principle

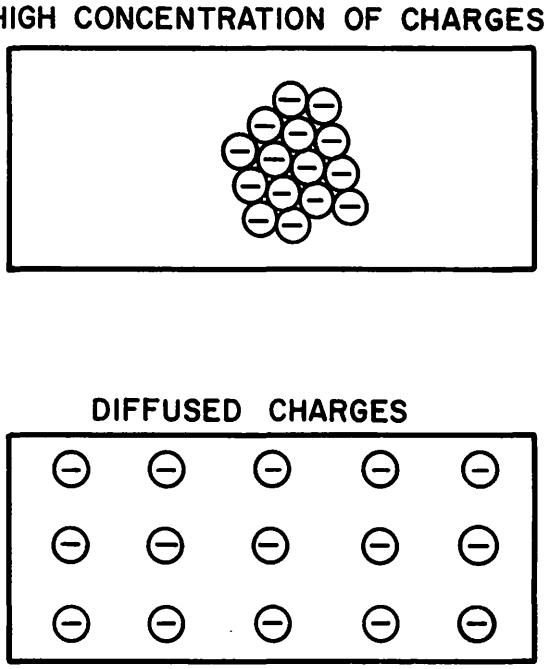
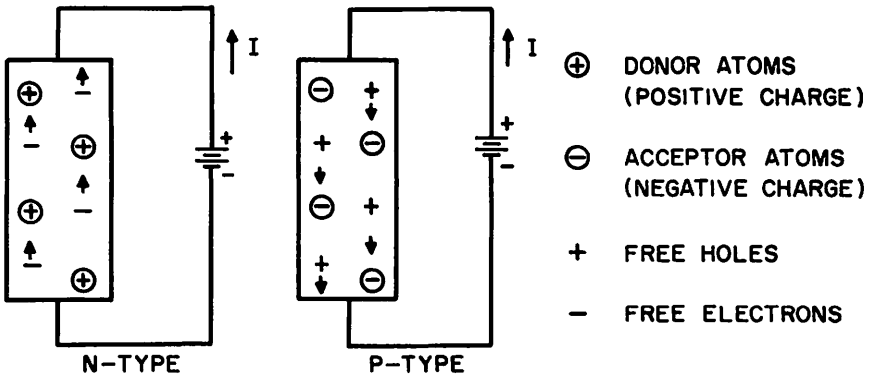



**Figure 1.8**

of space charge neutrality, the total number of electrons in the semiconductor is determined by the total number of acceptor atoms in the crystal. For the case of the p-type semiconductor, hole-electron pairs are generated at the upper terminal. The electrons flow through the wire to the positive terminal of the battery and the holes move downward through the semiconductor and recombine with electrons at the lower terminal.

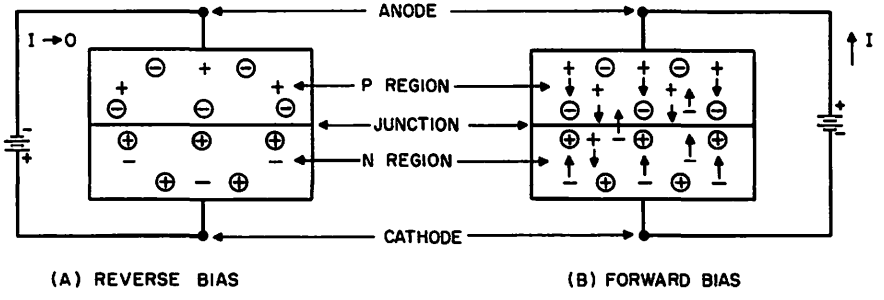



**CONDUCTION IN N-TYPE AND P-TYPE SEMICONDUCTORS**

**Figure 1.9**

## DIODES

If a p-type region and an n-type region are formed in the same crystal structure, we have a device known as a *diode.* The boundary between the two regions is called a *junction,* the terminal connected to the p-region is called the *anode,* and the terminal connected to the n-region is called the *cathode.* A diode is shown in Figure 1.10 for two conditions of applied voltage. In Figure 1.10(A) the anode is at a negative voltage with respect to the cathode and the diode is said to be *reverse biased.* The holes in the p-region are attracted toward the anode terminal (away from the junction) and the electrons in the n-region are attracted toward the cathode terminal (away from the junction). Consequently, no carriers can flow across the junction and no current will flow through the diode. Actually a small *leakage current* will flow because of the few hole-electron pairs which are thermally generated in the vicinity of the junction. Note that there is a region near the junction where there are no carriers *(depletion layer).* The charges of the donor and acceptor atoms in the depletion layer generate a voltage which is equal and opposite to the voltage which is applied between the anode and cathode terminals. As the applied voltage is increased, a point will be reached where the electrons crossing the junction (leakage current) can acquire enough energy to produce additional hole-electron pairs on collision with the semiconductor atoms *(avalanche multiplication).* The voltage at which this occurs is called the *avalanche voltage* or *breakdown voltage* of the junction. If the voltage is increased above the breakdown voltage, large currents can flow through the junction and, unless limited by the external circuitry, this current can result in destruction of the diode.



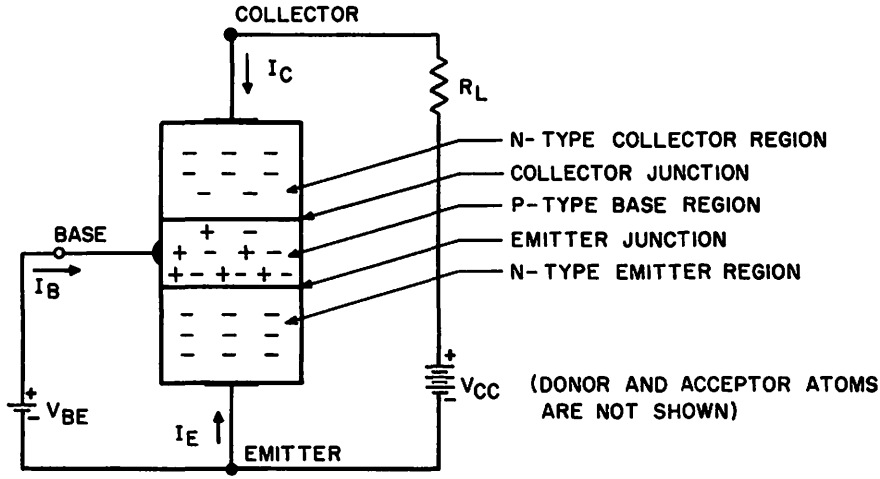

**CONDUCTION IN A PN JUNCTION DIODE**
**Figure 1.10**

In Figure 1.10(B) the anode of the diode is at a positive voltage with respect to the cathode and the rectifier is said to be *forward biased.* In this case, the holes in the p-region will flow across the junction and recombine with electrons in the n-region. Similarly, the electrons in the n-region will flow across the junction and recombine with the holes in the p-region. The net result will be a large current through the diode for only a small applied voltage.

## TRANSISTORS

An NPN transistor is formed by a thin p-region between two n-regions as shown in Figure 1.11. The center p-region is called the *base* and in practical transistors *is* generally less than .001 inch wide. One junction is called the *emitter* junction and the

other junction is called the *collector* junction. In most applications the transistor is used in the common emitter configuration as shown in Figure 1.11 where the current through the output or load ($R_L$) flows between the emitter and collector and the control or input signal ($V_{BE}$) is applied between the emitter and base. In the normal mode of operation, the collector junction is reverse biased by the supply voltage $V_{CC}$ and the emitter junction is forward biased by the applied base voltage $V_{BE}$. As in the case of the diode, electrons flow across the forward biased emitter junction into the base region. These electrons are said to be emitted or injected by the emitter into the base. They diffuse through the base region and flow across the collector junction and then through the external collector circuit. Transistor action is therefore one of *injection, diffusion,* and *collection.*




**CONDUCTION IN AN NPN JUNCTION TRANSISTOR**
(COMMON EMITTER CONFIGURATION)

**Figure 1.11**

If the principle of space charge neutrality is used in the analysis of the transistor, it is evident that the collector current is controlled by means of the positive charge (hole concentration) in the base region. As the base voltage $V_{BE}$ is increased the positive charge in the base region will be increased, which in turn will permit an equivalent increase in the number of electrons flowing between the emitter and collector across the base region. In an ideal transistor it would only be necessary to allow base current to flow for a short time to establish the desired positive charge. The base circuit could then be opened and the desired collector current would flow indefinitely. The collector current could be stopped by applying a negative voltage to the base and allowing the positive charge to flow out of the base region. In actual transistors, however, this can not be done because of several basic limitations. Some of the holes in the base region will flow across the emitter junction and some will combine with the electrons in the base region. For this reason, it is necessary to supply a current to the base to make up for these losses. The ratio of the collector current to the base current is known as the current gain of the transistor $h_{FE} = I_C/I_B$. For a-c signals the current gain is $\beta = h_{fe} = i_c/i_b$. The ratio of the a-c collector current to a-c emitter current is designated by $\alpha = h_{fb} = i_c/i_e$.

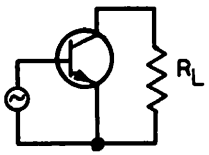
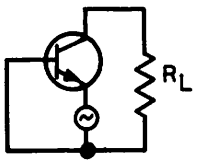
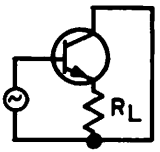
When a transistor is used at higher frequencies, the fundamental limitation is the

time it takes for carriers to diffuse across the base region from the emitter to the collector. Obviously, the time can be reduced by decreasing the width of the base region. The frequency capabilities of the transistor are usually expressed in terms of the *alpha cutoff frequency* ($f_{\alpha fb}$). This is defined as the frequency at which $\alpha$ decreases to 0.707 of its low frequency value. The alpha cutoff frequency may be related to the base charge characteristic and the base width by the equations:

$$T_E = \frac{Q_B}{I_E} = \frac{W^2}{2D} = \frac{0.19}{f_{\alpha fb}}$$

where $T_E$ is the emitter time constant, $Q_B$ is the base charge required for an emitter current $I_E$, W is the base width, and D is the diffusion constant which depends on the semiconductor material in the base region.

The operation of the transistor has been described in terms of the *common* emitter configuration. The term *grounded* emitter is frequently used instead of common emitter, but both terms mean only that the emitter is common to both the input circuit and output circuit. It is possible and often advantageous to use transistors in the common base or common collector configuration. The different configurations are shown in Figure 1.12 together with their comparative characteristics in class A amplifiers.

| CIRCUIT CONFIGURATION | | CHARACTERISTICS* | |
|---|---|---|---|
| COMMON EMITTER (CE) |   | moderate input impedance<br>moderate output impedance<br>high current gain<br>high voltage gain<br>highest power gain | (1.3 K)<br>(50 K)<br>(35)<br>(−270)<br>(40 db) |
| COMMON BASE (CB) |   | lowest input impedance<br>highest output impedance<br>low current gain<br>high voltage gain<br>moderate power gain | (35 Ω)<br>(1 M)<br>(−0.98)<br>(380)<br>(26 db) |
| COMMON COLLECTOR (CC) (EMITTER FOLLOWER) |   | highest input impedance<br>lowest output impedance<br>high current gain<br>unity voltage gain<br>lowest power gain | (350 K)<br>(500 Ω)<br>(−36)<br>(1.00)<br>(15 db) |

*Numerical values are typical for the 2N525 at audio frequencies with a bias of 5 volts and 1 ma., a load resistance of 10K, and a source (generator) resistance of 1K.

**TRANSISTOR CIRCUIT CONFIGURATIONS**
**Figure 1.12**

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# TRANSISTOR CONSTRUCTION TECHNIQUES

CHAPTER 2

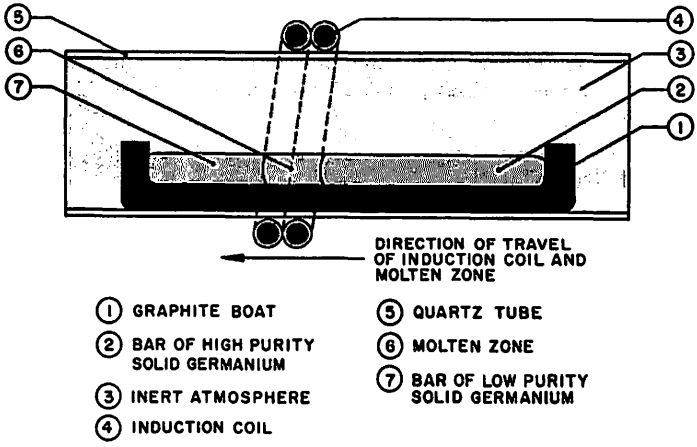
The knowledge of many sciences is required to build transistors. Physicists use the mathematics of atomic physics for design. Metallurgists study semiconductor alloys and crystal characteristics to provide data for the physicist. Chemists contribute in every facet of manufacturing through chemical reactions which etch, clean and stabilize transistor surfaces. Mechanical engineers design intricate machines for precise handling of microminiature parts. Electronic engineers test transistors and develop new uses for them. Statisticians design meaningful life test procedures to determine reliability. Their interpretation of life test and quality control data leads to better manufacturing procedures.

The concerted effort of this sort of group has resulted in many different construction techniques. All these techniques attempt to accomplish the same goal – namely to construct two parallel junctions as close together as possible. Therefore, these techniques have in common the fundamental problems of growing suitable crystals, forming junctions in them, attaching leads to the structure and encapsulating the resulting transistor. The remainder of this chapter discusses these problems.

## METAL PREPARATION

Depending on the type of semiconductor device being made, the structure of the semiconductor material varies from nearly perfect single crystal to polycrystalline. The theory of transistors and rectifiers, however, is based on the properties of single crystals. Defects in a single crystal produce generally undesirable effects.

Germanium and silicon metal for use in transistor manufacture must be so purified that the impurity concentration is less than one part in $10^{10}$. Donor and acceptors are then added in the desired amounts and the material is then grown into a single crystal.




**SIMPLIFIED ZONE REFINING APPARATUS**

**Figure 2.1**

The initial purification of germanium and silicon typically involves reactions which produce the chemical compounds germanium and silicon tetrachloride or dioxide. These compounds can be processed to give metallic germanium or silicon of relatively high purity. The metal so prepared is further purified by a process called zone refining. This technique makes use of the fact that many impurities are more soluble when the metal is in its liquid state, thus enabling purification to result by progressive solidification from one end of a bar of metal.

In practical zone refining a narrow molten zone is caused to traverse the length of a bar. A cross-sectional view of a simplified zone refining furnace is shown in Figure 2.1. High purity metal freezes out of the molten zone as the impurities remain in solution. By repeating the process a number of times, the required purity level can be reached. During the process it is important that the metal be protected from the introduction of impurities. This is done by using graphite or quartz parts to hold the metal, and by maintaining an inert atmosphere or vacuum around it. The heating necessary to produce a narrow molten zone is generally accomplished by induction heating, i.e., by coils carrying radio frequency energy and encircling the metal bar in which they generate heat.

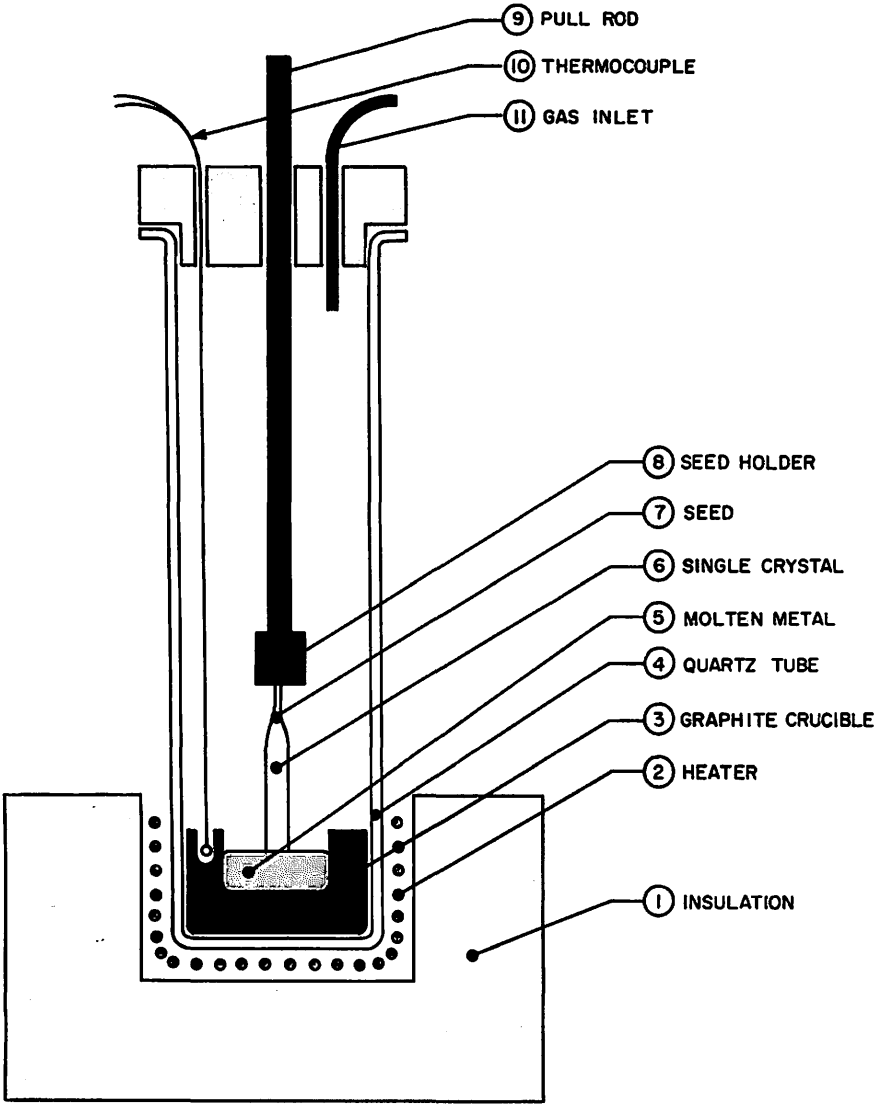
The purified metal is now ready for doping and growing into a single crystal. A common method for growing single crystals is the Czochralski method illustrated in Figure 2.2. In it a crucible maintains molten metal a few degrees above its melting point. A small piece of single crystal called a seed is lowered into the molten metal and then slowly withdrawn. If the temperature conditions are properly maintained a single crystal of the same orientation, i.e., molecular pattern as the seed grows on it until all the metal is grown into the crystal. Doping materials can be added to the molten metal in the crucible to produce appropriate doping. The rate at which doping impurities are transferred from the molten metal to the crystal can be varied by the crystal growing rate, making it possible to grow transistor structures directly into the single crystal. This is discussed in detail in the next section.

The floating zone technique for both refining and growing single crystals has recently been introduced. It is quite similar in principle to zone refining except that the graphite container for the bar is eliminated, reducing the risk of contamination. In place of it, clamps at both ends hold the bar in a vertical position in the quartz tube. The metal in the molten zone is held in place by surface tension. Doping agents added at one end of the bar can be uniformly distributed through the crystal by a single cycle of zone refining. This technique has had much success in producing high quality silicon metal.

## JUNCTION FORMATION

A junction is a surface separating two regions of a semiconductor, one with n type and the other with p type conductivity. Since transistors consist of two closely spaced junctions, it is necessary to establish highly non-uniform distributions of n and p type impurities in the semiconductor lattice. The techniques used for establishing these impurity distributions provide the basis for the different types of transistors being made today.

Three basic techniques are used, individually or in combination, in establishing the desired impurity distribution. The first of these is to form an alloy of the semiconductor and a material which acts as either a donor or acceptor in the semiconductor lattice. The most common materials used for this purpose are indium, which is used for making the emitter and collector regions of germanium alloy transistors such as the 2N43A and the 2N396, and aluminum, which is used for making the emitter region of



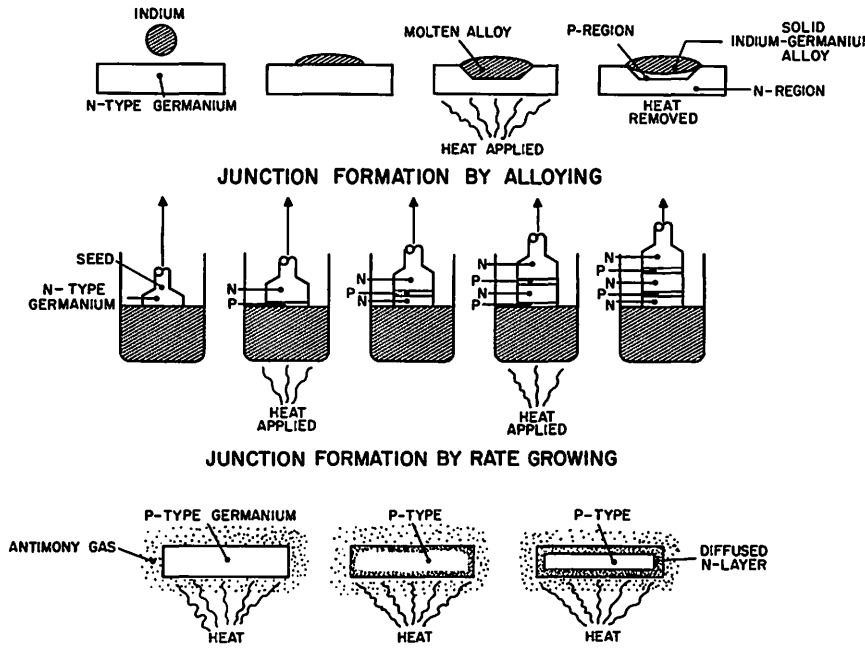

**SIMPLIFIED CRYSTAL GROWING FURNACE**

**Figure 2.2**

germanium mesa transistors such as the 2N705 and 2N711. In these cases, an alloy is formed with the metal and some of the n type germanium. Upon freezing, a p type semiconductor layer is deposited creating a pn junction.

A second method is to change the impurity concentration in the crystal as it is being grown from the liquid state. Ordinarily, crystals are grown so as to produce some constant level of impurity throughout. Because of a tendency for most impurities to remain in the melt rather than deposit in the solid, which is also the basis of zone refining, the concentration does not remain uniform as the crystal is grown, but increases continuously due to the increasing impurity concentration in the melt. The concentration of impurities deposited in the solid is affected by the rate at which the crystal is grown, in the case of some impurities. By a proper selection of impurities and the inclusion of both p and n type impurities in the melt, pn junctions can be grown into the crystal by periodically changing the growth rate.

Diffusion is a third method of impurity control. It consists of a gradual movement of impurity atoms through the semiconductor lattice while the semiconductor remains a solid. Because this movement is a function of the thermal energy of the impurity atoms, the rate of movement is temperature sensitive and appreciable movement takes place at high temperatures. Temperatures used in diffusion range from 500°C to 800°C for germanium and from 900°C to 1300°C for silicon.




**JUNCTION FORMATIONS**

**Figure 2.3**

One diffusion technique is to place the semiconductor in a gas containing the desired impurity and heating. A variation of this is to coat the surface with a chemical containing the desired impurity and heating. In both cases, the impurity enters into the semiconductor from the outside. In another case, the desired diffusion takes place entirely within the semiconductor body which is grown with abrupt changes in the impurity concentration. In each of the above cases, diffusion takes place from the region of the high impurity concentration to the region of low concentration.

Diffusion generally involves times of several hours, rather than seconds as in the case of rate growing techniques. This makes it easier to obtain good process control. In addition, diffusion makes it possible to vary the impurity concentration over a wide range. This is in sharp contrast to both rate growing and alloying, and together with its good process control makes diffusion a highly attractive technique for the manufacture of transistors.

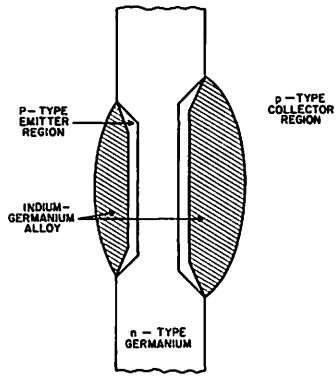
## ALLOY TRANSISTORS

The alloy transistor is made by alloying metal into opposite sides of a thin piece of semiconductor to form an emitter and collector region. In order to achieve uniformity of the transistor characteristics, the pellet thickness, the quantity of metal to be alloyed, the area of contact of the metal to the semiconductor and the alloying temperature must be carefully controlled. Each of these variables affects the base width of the transistor, which in turn affects most electrical characteristics. Because of the large number of variables, thin base widths cannot be achieved consistently; therefore, a practical lower limit exists for the base width and with it an upper limit on the operating frequency is also established. One measure of the maximum operating frequency is $f_{hfb}$; this is the frequency at which the current gain of the transistor is 3 db below its low frequency value, commonly referred to as the alpha cutoff frequency. Typical values of $f_{hfb}$ for alloy transistors range from 1 mc for the 2N43 to 8 mc for the 2N396.

On the other hand, the emitter and collector regions of an alloy transistor are quite thin and have a high electrical conductivity. Because of this alloy transistors have a very low saturation resistance. The saturation resistance is a measure of how nearly the transistor can be made to appear as a short circuit when it is turned *on* in switching circuits, and in most transistors it is made up primarily of the parasitic resistance of the emitter and collector bodies. A typical value for the 2N396 is 1.6 ohms at 50 ma.

The microalloy transistor is a variation of the alloy transistor. In order to achieve a thin base width without making the transistor unduly fragile, electrochemical etching techniques are used to provide a very thin region in the middle of an otherwise relatively thick pellet. Metal is then deposited on each side of this thin region and alloyed with a very small amount of germanium. Electrically, the characteristics are those of an alloy transistor with a thin base. Mechanically, the transistor is less fragile than it would be if the entire pellet were the same thickness as the base region.

A variation of the microalloy transistor is the microalloy diffused transistor. In this case, a diffused layer is established over the entire pellet surface prior to etching the thin region in the middle of the pellet. The etching is then done predominantly on one side so as to remove the diffused layer from the region of the collector contact. The other side of the pellet is etched only slightly so that the emitter is adjacent to the diffused region. Both the microalloy and microalloy diffused transistors represent improvements in frequency response over conventional alloy transistors. Typical of these processes are the microalloy 2N393 with $f_{hfb}$ of 40 mc and the microalloy diffused transistor 2N502 with $f_{hfb}$ of 200 mc.



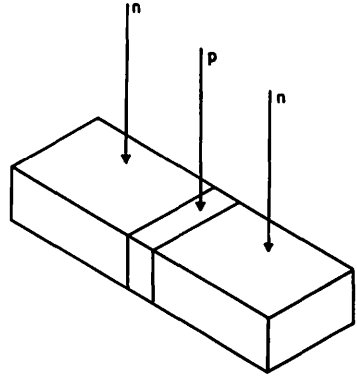

**GERMANIUM PNP ALLOY TRANSISTOR**

**Figure 2.4**

## GROWN JUNCTION TRANSISTORS

Grown junction transistors differ from alloy transistors in that the junctions are created during the growth of the crystal rather than by alloying after the crystal is grown. This results in significant differences in geometry and electrical characteristics. One technique of growing junctions into the crystal is to vary the rate of growth and utilize the variation of segregation coefficient with growth rate. In germanium, a very slow growth speed is used to produce p regions while rapid growth is used to produce n regions, thus creating a series of n and p regions; thirty or more pairs of junctions can be produced in a single crystal in this manner. While both npn and pnp transistors can be produced by rate growing, the npn structures are inherently more attractive and rate growing is not used for making pnp transistors. (In silicon, rate growing is not used because it does not produce transistors competitive with those produced from grown diffused crystals. Grown diffused transistors are discussed on the next page.)

After the crystal is grown each pair of junctions is sawed from the wafer and diced into several hundred individual pellets. Each pellet is thus an npn transistor, requiring only leads and proper mounting. (See Figure 2.5.)




**RATE GROWN PELLET**

**Figure 2.5**

The geometry of this device is such that mechanical strength is not a function of the base width. It is simple to produce a base width as small as desired, but it is difficult to control this consistently, as thermal conditions are not uniform throughout the crystal during growth. Furthermore, it is difficult to achieve a high concentration of p type impurities in the base region. For these reasons, rate grown transistors have a lower limit on the base width, and, therefore, a limited frequency range. The 2N78 and 2N167 are typical rate grown transistors, both of which have an $f_{hfb}$ of 9 mc.

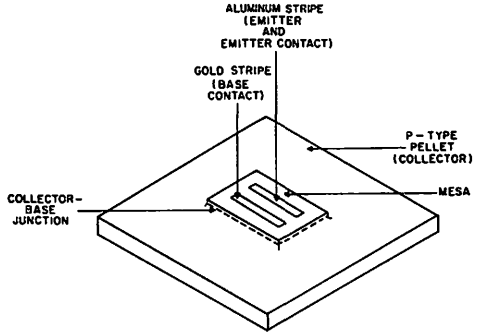
It is necessary to make a contact to the base region of this transistor without significantly altering the original structure. Any portion of the base lead which overlaps the collector or emitter regions reduces the breakdown voltage and adds capacitance to these junctions.

Another transistor with similar geometry is the grown diffused transistor. This transistor utilizes a combination of impurity segregation during growth and diffusion. The segregation and diffusion coefficients are such that npn silicon and pnp germanium transistors are produced by this process. In the case of silicon, a lightly doped n type crystal is dipped into molten silicon containing n and p type impurities. A highly conducting n type region is grown which also contains a considerable quantity of p type impurities. After a short time at elevated temperatures these p type impurities diffuse from the newly grown layer into the lightly doped n type material, thus creating a p type base region between a heavily doped n type emitter region and a lightly doped n type collector region. This technique provides better control of the base width and a higher concentration of impurities in the base than can be achieved by rate growing. Such transistors will therefore operate at higher frequencies even though the base lead overlap still limits the performance. The 2N338 is a typical grown diffused transistor with an $f_{hfb}$ of 20 mc.

All grown junction transistors are mounted and supported by contacts to their emitter and collector regions. Various methods have been used; the most reliable is the use of a ceramic disc which has metallized regions to which the emitter and collector regions are alloyed. This is known as *fixed-bed* construction. The rigid disc prevents stresses in the semiconductor material which arise from vibration of the header leads.

## GERMANIUM MESA TRANSISTORS

The limitations characteristic of alloy and grown junction transistors can be overcome by use of *mesa* construction, shown in Figure 2.6 below.




**GERMANIUM MESA PELLET**

**Figure 2.6**

The mechanical reliability is not affected by the thickness of the base region because it is diffused into the pellet from the surface. The use of diffusion results in excellent control of the base width. In addition, resistivity of the base and collector regions can be varied at will over a wide range to obtain optimum device characteristics.

The metal stripes are evaporated onto the surface of the diffused pellet. One stripe is gold which provides a non-rectifying contact to the base region; the other stripe is aluminum which forms a rectifying contact and thus serves as an emitter. Most of the diffused layer outside the stripes is removed by etching so as to reduce the collector junction capacitance and give better collector diode characteristics. The fabrication is completed by mounting the pellet onto a header and bonding small gold wires to the metal stripes. The thermal impedance between the junctions and the header is low since the pellet is mounted directly on the header. High speed switching transistors with an excellent reliability record have been made with this process.

The conventional mesa transistor utilizes a collector resistivity which is a compromise between a high resistivity for a high $BV_{CBO}$ and low capacitance on one hand, and a low resistivity for a low saturation voltage on the other hand. The need for compromise can be largely eliminated by using a combination of high and low resistivity material in a single pellet. This is achieved by growing a high resistivity film onto a low resistivity pellet.

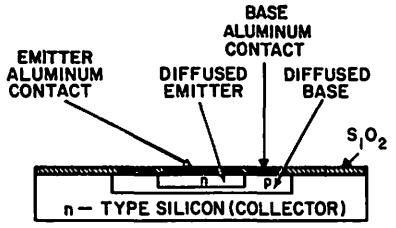
Such films are called *epitaxial* films because the atoms are aligned in a continuation of the original crystalline structure, resulting in one single crystal pellet. The base region is then diffused into the thin film and the rest of the fabrication is the same as for the conventional mesa. Epitaxial transistors represent a substantial improvement over the conventional mesas in that a higher $BV_{CBO}$, lower capacitance, and lower saturation voltage can be achieved simultaneously. These improved characteristics in turn permit higher switching speeds and operation at higher current levels. The 2N994 is an epitaxial transistor which is similar to the non-epitaxial 2N705. $C_{ob}$ is 30% smaller, however, and $V_{CE(SAT)}$ is 50% smaller. In addition, the 2N994 provides a 400% increase in current handling capability together with a 50% reduction in switching time.

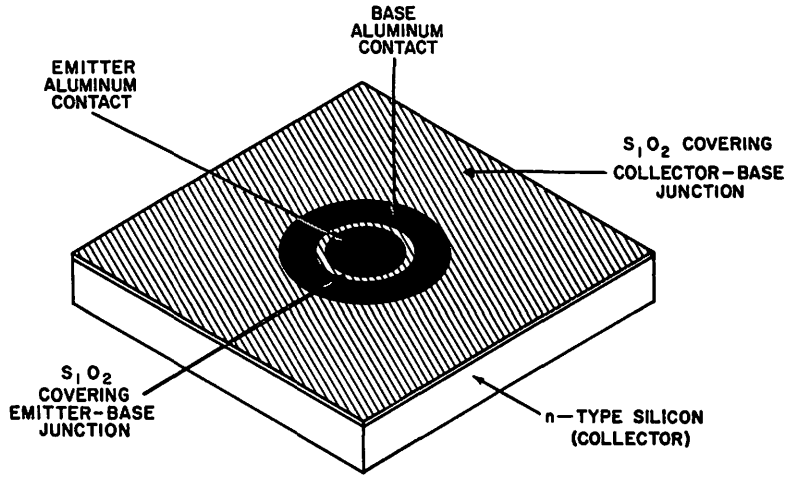
## SILICON PLANAR TRANSISTORS

This transistor is made by diffusing the emitter as well as the base. A diffused emitter is desirable because of the same control and ability to select the desired impurity level that makes a diffused base desirable. In addition, no mesa forming etch is used. These differences result from the fact that silicon dioxide can be formed on the surface of silicon pellets to act as a mask to prevent the diffusion of impurities into the silicon. The base and emitter regions are formed by selectivity removing portions of the silicon dioxide to permit diffusion into the silicon. The two regions are formed sequentially; oxidation and selective removal of the oxide take place prior to each diffusion. Aluminum is deposited on both the base and emitter regions to provide low resistance, mechanically reliable contacts.

The oxide covers the junctions of the completed transistors, thereby preventing ambient gases from reaching the junction. This results in a *passivated* device with excellent electrical stability.

This protective oxide can also be formed on epitaxial films. The resulting improvements in $BV_{CBO}$, $C_{ob}$, $V_{CE(SAT)}$ and current handling capability are similar to those achieved with germanium epitaxial transistors.




**SILICON PLANAR PELLET**

**Figure 2.7**

## ENCAPSULATION

The term encapsulation is used here to describe the processing from the completion of the transistor structure to the final sealed unit. The primary purpose of encapsulation is to ensure reliability. This is accomplished by protecting the transistor from mechanical damage and providing a seal against harmful impurities. Encapsulation also governs thermal ratings and the stability of electrical characteristics.

The transistor structure is prepared for encapsulation by etching to dissolve the surface metal which may have acquired impurities during manufacture. Following etching, a controlled atmosphere prevents subsequent surface contamination. The transistor now is raised to a high temperature, is evacuated to eliminate moisture and is refilled with a controlled atmosphere. Then the cap, into which a getter may be placed, is welded on.

In some respects the design of the case, through its contribution to transistor reliability, is as important as that of the transistor structure. Mechanically, users expect to drop transistors, snap them into clips or bend their leads without any damage. Ther-

mally, users expect the header lead seals to withstand the thermal shock of soldering, the junctions to be unaffected by heating during soldering, and the internal contacts to be unchanged by thermal cycling. Considerable design skill and manufacturing cost is necessary to meet the users expectations. Within the transistor structure, coefficients of expansion are matched to prevent strain during thermal cycling. Kovar lead seals withstand the shock of soldering and do not fatigue and lose their effectiveness after thermal cycling. Hard solders and welds maintain constant thermal impedance with time, avoiding possible crystallization of soft solders.

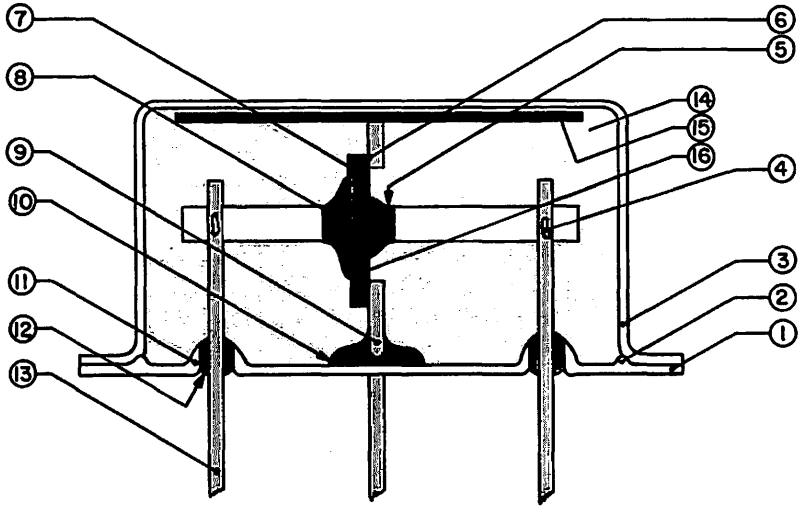
For the stability of electrical characteristics, hermetic seals cannot be overemphasized. They not only preserve the carefully controlled environment in which the transistor is sealed but they exclude moisture which causes instability. Moisture can be responsible for slow reversible drifts in electrical characteristics as operating conditions are changed. Also, while a transistor is warming up after exposure to low temperatures, precipitated moisture may cause a large temporary increase in $I_{CO}$. Kovar glass lead seals are used in transistors designed for reliability. Kovar does not have the low thermal impedance or ductility of copper, however, and therefore seal integrity is paid for by a lower dissipation rating and a lower tolerance to lead bending.

The case design governs the transistor's thermal impedance, which should be as low as possible and consistent from unit to unit. Very small cases minimize the junction to case impedance while increasing the case to air impedance. Larger cases such as the JEDEC 370 mil TO-9 combine a lower case to air impedance, with a lead configuration and indexing tab permitting automatic insertion of transistors into printed circuit boards.

## RELIABILITY

In principal, transistors have no known failure mechanism which should limit their life expectancy. However, in practice, failure mechanisms do exist. To date sufficient data has been collected to show that with careful construction techniques, transistors are capable of operation in excess of 40,000 hours at maximum ratings without appreciable degradation. There is no reason to believe this is the limit of operating life. Since transistors can perform logical operations at very low dissipation and amplify at high efficiency, the resulting low dissipation reduces the ambient temperature for other components, enhancing their reliability as well. The transistor's small physical size and its sensitivity to small voltage changes at the base results in low circuit capacitances and low power requirements, permitting large safety factors in design. The variety of manufacturing processes being used by the industry permits choosing the optimum transistor for any circuit requirement. For example, rate grown transistors offer low $I_{CO}$ and low $C_C$ for applications requiring low collector current. Alloy transistors offer high peak power capabilities, great versatility in application, and are available in both PNP and NPN types. Mesa and planar epitaxial transistors give high speed at high voltage ratings and with good saturation characteristics.

While reliability must be built in, it has seldom proved practical in the past to make an absolute measurement of a specific transistor's reliability. Transistors currently are sufficiently reliable that huge samples and considerable expense in manpower, equipment, and inventory are necessary to get a true measure of their reliability. However, tests can readily show if a transistor falls far short of the required reliability; therefore, they are useful in assigning ratings, in obtaining rate of degradation measurements, and as a measure of quality control or process variability. Figures 2.8, 2.9, 2.10 and 2.11 show some of the considerations in designing reliable transistors.




① KOVAR METAL FOR BEST HERMETIC SEAL

② RIDGE ASSURES BETTER PRECISION IN WELDING

③ COPPER CLAD STEEL FOR STRAIN FREE FABRICATION, SALT SPRAY RESISTANCE AND MECHANICAL STRENGTH

④ WELDED CONTACTS BETWEEN COLLECTOR AND EMITTER TABS, AND HEADER LEADS

⑤ SPECIAL ALLOYS AND PROCESSING TO PREVENT POOR WETTING AND CONSEQUENT INTERMITTENT CONTACT

⑥ SPECIAL ALLOYS BETWEEN WAFER AND SUPPORTING WINDOW TO CONTROL STRESSES DUE TO THERMAL EXPANSION, TO GET GOOD WETTING BETWEEN WINDOW AND WAFER REDUCING THERMAL IMPEDANCE AND SERIES BASE RESISTANCE, TO GET PURELY OHMIC CONTACT

⑦ CRYSTAL ORIENTATION CHOSEN TO PREVENT DOT SPREADING

⑧ COLLECTOR DOT CENTERED EXACTLY OPPOSITE EMITTER DOT FOR HIGH CURRENT GAIN

⑨ THICK WINDOW TO MINIMIZE THERMAL IMPEDANCE TO CASE

⑩ TWO LARGE WELDS PROVIDE HEAT PATH FROM WINDOW TO CASE

⑪ SHOULDER ON SEAL FOR STRENGTH

⑫ KOVAR TO HARD GLASS MATCHED COEFFICIENT SEAL

⑬ KOVAR LEADS HELP REDUCE JUNCTION HEATING DURING SOLDERING

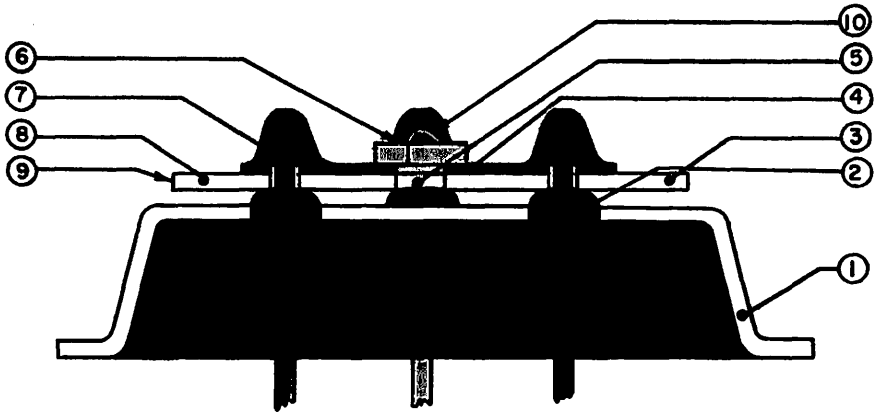
⑭ GASEOUS ATMOSPHERE AVOIDS THE MIGRATION OF IONS POSSIBLE WITH FLUID TYPE FILLERS

⑮ GETTER TABLET TO PERMANENTLY ABSORB ANY MOISTURE DUE TO OUTGASSING

⑯ SPECIAL ETCHING AND SURFACE TREATMENT RESULTS IN STABLE $I_{CO}$ AT ALL TEMPERATURES, VERY LOW NOISE FIGURE, AND SMALL $I_{CO}$ VARIATION WITH COLLECTOR VOLTAGE.

**ALLOY TRANSISTOR**
DESIGN FOR RELIABILITY
(TYPES 2N43, 2N396, 2N525)

**Figure 2.8**




① KOVAR METAL HEADER FOR BEST HERMETIC SEAL

② RAISED GLASS BEAD TO PREVENT POSSIBLE OCCLUSION OF CONTAMINANTS

③ CERAMIC DISK WITH COEFFICIENT OF THERMAL EXPANSION MATCHING THAT OF SILICON

④ GOLD STRIPS BONDED TO CERAMIC BY TECHNIQUES PERFECTED FOR CERAMIC TUBE

⑤ SLIT IN DISK CUT TO ±0.001" TOLERANCE

⑥ BASE REGION PLACED CLOSE TO COLLECTOR CONTACT FOR LOW THERMAL IMPEDANCE AND LOW SATURATION RESISTANCE

⑦ HARD SOLDER PREVENTS THERMAL FATIQUE PROBLEMS

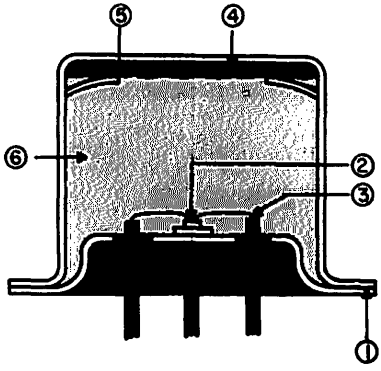
⑧ SPECIAL NON-POROUS CERAMIC IS IMPERVIOUS TO PROCESSING CHEMICALS

⑨ DISK DIAMETER SMALL ENOUGH TO PREVENT ANY CONTACT WITH CASE

⑩ BASE LEAD ATTACHED TO GOLD STRIP

**GROWN DIFFUSED TRANSISTOR**
FIXED BED MOUNTING DESIGN FOR RELIABILITY
(TYPES 2N335, 2N337, 2N491)

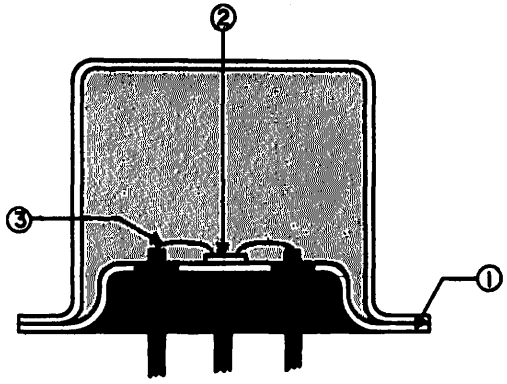
**Figure 2.9**




① KOVAR METAL HEADER FOR BEST HERMETIC SEAL
② DIRECT MOUNTING OF PELLET TO HEADER ASSURES BEST MECHANICAL AND THERMAL CHARACTERISTICS
③ THERMOCOMPRESSION BONDED LEADS ASSURE HIGHEST RELIABILITY
④ GETTER TO ASSUE DRY AMBIENT
⑤ ASSEMBLY TO ASSURE MECHANICAL STABILITY OF GETTER
⑥ GAS FILLED INTERIOR FOR MAXIMUM ELECTRICAL STABILITY

**GERMANIUM MESA TRANSISTOR**
DESIGN FOR RELIABILITY
(TYPES 2N705, 2N781, 2N994)

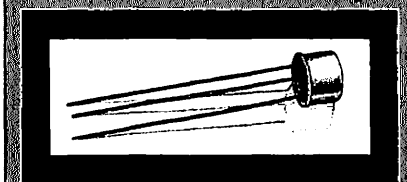
**Figure 2.10**




①KOVAR METAL HEADER FOR BEST HERMETIC SEAL
②DIRECT MOUNTING OF PELLET TO HEADER ASSURES BEST MECHANICAL AND THERMAL CHARACTERISTICS
③THERMOCOMPRESSION BONDED LEADS ASSURE HIGHEST RELIABILITY

**SILICON PLANAR PASSIVATED TRANSISTOR**
DESIGN FOR RELIABILITY
(TYPICAL TYPES 2N914, 2N2192)

**Figure 2.11**



# PLANAR EPITAXIAL TRANSISTORS

**NPN**

SILICON TYPES

**2N2193**
**2N2193A**
**2N2194**
**2N2194A**
**2N2195**
**2N2195A**

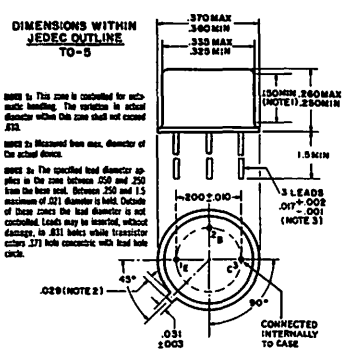
This family of General Electric devices are PLANAR EPITAXIAL transistors designed for high speed switching and high frequency amplifier circuits.

**FEATURES:**
- Low Leakage Current
- Low $V_{CE(SAT)}$
- Guaranteed current gain from 0.1 to 1000 ma.
- High Breakdown Voltage

## absolute maximum ratings (25°C unless otherwise specified)

| | | 2N2193 2N2193A | 2N2194 2N2194A | 2N2195 2N2195A | |
|---|---|---|---|---|---|
| **Voltage** | | | | | |
| Collector to Base | $V_{CBO}$ | 80 | 60 | 45 | volts |
| Collector to Emitter | $V_{CEO}$ | 50 | 40 | 25 | volts |
| Emitter to Base | $V_{EBO}$ | 8 | 5 | 5 | volts |
| **Current** | | | | | |
| Collector | $I_C$ | 1.0 | 1.0 | 1.0 | amp |
| **Transistor Dissipation** | | | | | |
| (Free Air 25°C)* | $P_T$ | 0.8 | 0.8 | | watts |
| (Free Air 25°C)** | $P_T$ | | | 0.6 | watts |
| (Case Temperature 25°C)*** | $P_T$ | 2.8 | 2.8 | 2.8 | watts |
| (Case Temperature 100°C)*** | $P_T$ | 1.6 | 1.6 | 1.6 | watts |
| **Temperature** | | | | | |
| Storage | $T_{STG}$ | ← −65 to +300 → | | | °C |
| Operating Junction | $T_J$ | ← −65 to +200 → | | | °C |

*Derate 4.6 mw/°C increase in ambient temperature above 25°C
**Derate 3.4 mw/°C increase in ambient temperature above 25°C
***Derate 16.0 mw/°C increase in case temperature above 25°C



## electrical characteristics: (25C° unless otherwise specified)

| | | 2N2193 2N2193A | | 2N2194 2N2194A | | 2N2195 2N2195A | | |
|---|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | Min. | Max. | Min. | Max. | Min. | Max. | |
| ▶ Collector to Base Voltage ($I_C = 100\ \mu a$) | $V_{CBO}$ | 80 | | 60 | | 45 | | volts |
| ▶ Collector to Emitter Voltage ($I_C = 25$ ma)† | $V_{CEO}$ | 50 | | 40 | | 25 | | volts |
| Emitter to Base Voltage ($I_E = 100\ \mu a$) | $V_{EBO}$ | 8 | | 5 | | 5 | | volts |
| Forward Current Transfer Ratio | | | | | | | | |
| ($I_C = 150$ ma, $V_{CE} = 10$ V)† | $h_{FE}$ | 40 | 120 | 20 | 60 | 20 | | |
| ($I_C = 10$ ma, $V_{CE} = 10$ V) | $h_{FE}$ | 30 | | 15 | | | | |
| ($I_C = 1000$ ma, $V_{CE} = 10$ V)† | $h_{FE}$ | 15 | | | | | | |
| ($I_C = 0.1$ ma, $V_{CE} = 10$ V) | $h_{FE}$ | 15 | | | | | | |
| ($I_C = 500$ ma, $V_{CE} = 10$ V)† | $h_{FE}$ | 20 | | 12 | | | | |
| ($I_C = 10$ ma, $V_{CE} = 10$ V, $T_A = -55°C$) | $h_{FE}$ | 20 | | | | | | |
| Base Saturation Voltage ($I_C = 150$ ma, $I_B = 15$ ma) | $V_{BE(SAT)}$ | | 1.3 | | 1.3 | | 1.3 | volts |
| ▶ Collector Saturation Voltage ($I_C = 150$ ma, $I_B = 15$ ma) | $V_{CE(SAT)}$ | | (0.35 volts max., 2N2193, 94, 95 only) | | | | | |
| | $V_{CE(SAT)}$ | | (0.25 volts max., 2N2193A, 94A, 95A only) | | | | | |
| | $V_{CE(SAT)}$ | | (0.16 volts typ., 2N2193A, 94A, 95A only) | | | | | |
| **CUTOFF CHARACTERISTICS** | | | | | | | | |
| ▶ Collector Leakage Current ($V_{CB} = 30$ V) | $I_{CBO}$ | | | | 10 | | 100 | mμa |
| ($V_{CB} = 30$ V, $T_A = 150°C$) | $I_{CBO}$ | | | | 25 | | 50 | μa |
| ($V_{CB} = 60$ V) | $I_{CBO}$ | | 10 | | | | | mμa |
| ($V_{CB} = 60$ V, $T_A = 150°C$) | $I_{CBO}$ | | 25 | | | | | μa |
| Emitter Base Cutoff Current ($V_{EB} = 5$ V) | $I_{EBO}$ | | 50 | | | | | mμa |
| ▶ Emitter Base Leakage Current ($V_{EB} = 3$ V) | $I_{EBO}$ | | | | 50 | | 100 | mμa |
| **HIGH FREQUENCY CHARACTERISTICS** | | | | | | | | |
| Current Transfer Ratio ($I_C = 50$ ma, $V_{CB} = 10$ V, $f = 20$ mc) | $h_{fe}$ | 2.5 | | 2.5 | | 2.5 | | |
| Collector Capacitance ($I_B = 0$, $V_{CB} = 10$ V, $f = 1$ mc) | $C_{ob}$ | | 20 | | 20 | | 20 | pf |
| **SWITCHING CHARACTERISTICS (See Figure 1)** ($V_{IN} = 15$V, $V_L = 15$V) | | | | | | | | |
| Rise Time | $t_r$ | | 70 | | 70 | | | nsec |
| Storage Time | $t_s$ | | 150 | | 150 | | | nsec |
| Fall Time | $t_f$ | | 50 | | 50 | | | nsec |

†Pulse width ≤300 μsec, duty cycle ≤2%

GENERAL ELECTRIC

The published transistor specification sheet is fully as important as the device it describes since it provides the description necessary for sensible use of the subject transistor.

Four general categories of information are presented. These are

1. a statement of broad device capabilities and intended service
2. absolute maximum ratings
3. electrical characteristics
4. generic or family electrical characteristics

Let's study each of these categories in some detail and use the specification sheet for 2N2193 through 2N2195 as a guide.

## 1. GENERAL DEVICE CAPABILITIES

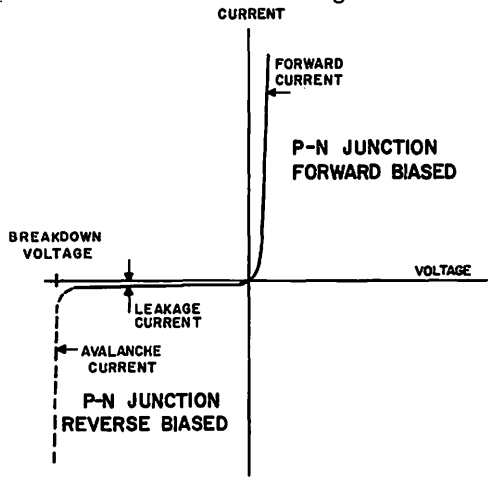
The lead paragraph found at the top of the sheet furnishes the user with a concise statement of the most likely applications and salient electrical characteristics of the device. It is useful in first comparison of devices as one selects the proper device for a particular application.

## 2. ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings specify those electrical, mechanical, and thermal ratings of a semiconductor device which, as limiting values, define the maximum stresses beyond which either initial performance or service life is impaired.

### VOLTAGE

The voltages specified in the *Absolute Maximum Ratings* portion of the sheet are breakdown voltages with reverse voltage applied to one selected junction, or across two junctions with one junction reverse biased and the second junction in some specified state of bias. Single junction breakdown either between collector and base or between emitter and base has the form shown in Figure 3.1.

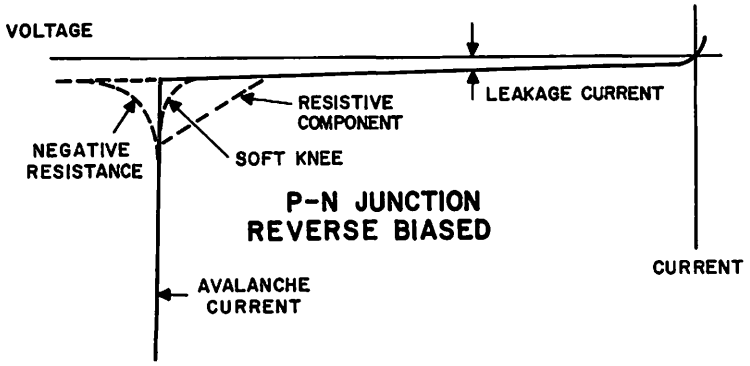



**TYPICAL VOLTAGE CURRENT CHARACTERISTICS OF A P-N JUNCTION**

**Figure 3.1**

The solid portion of the curve is the active, normally used portion of a diode or any compound junction device. The dotted portion exhibits large dramatic changes in reverse current for small changes in applied voltage. This region of abrupt change is called the *breakdown* region. If breakdown occurs at relatively low voltage, the mechanism is through tunneling or "zener" breakdown. The means of conduction is through electrons which have "tunneled" from valence to conduction energy levels. A more complete explanation of tunneling is contained in the Tunnel Diode Manual.*

At higher voltage levels conduction is initiated and supported by solid ionization. When the junction is reverse biased, minority current flow (leakage current) is made up of holes from the N-type material and electrons from the P-type material. The high field gradient supplies carriers with sufficient energy to dislodge other valence electrons, raising their energy level to the conduction band resulting in a chain generation of hole-electron pairs. This process is called *avalanche*. While theory predicts an abrupt, sharp (sometimes called *hard*) characteristic in the breakdown region, a *soft* or gradual breakdown often occurs. Another possibility is the existence of a negative resistance "hook." The hook usually occurs when zener breakdown is the predominant mechanism. Figure 3.2 graphically illustrates these possibilities. In practice, silicon, because of lower leakage current, exhibits a sharper knee than does germanium.




**TYPICAL VARIATIONS IN BREAKDOWN CHARACTERISTIC OF A P-N JUNCTION**

**Figure 3.2**

The family of the 2N2193 to 2N2195 silicon devices are measured for individual junction breakdown voltages at a current of 100 microamperes. $V_{CBO}$, the collector-base diode breakdown voltage— with emitter open circuited or floating — is shown to be a minimum of 80 volts for the 2N2193 and 2N2193A.

$V_{EBO}$, the emitter-base breakdown voltage — with collector open circuited or floating — is specified at 8 volts minimum for the 2N2193 and 2N2193A.

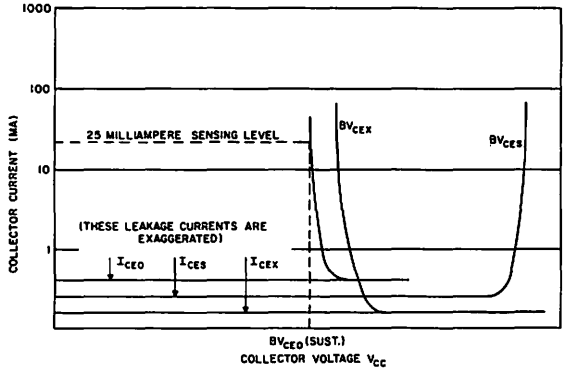
The breakdown voltage between collector and emitter is a more complex process. The collector-base junction in any configuration involving breakdown is always reverse biased. On the other hand, the condition applied to the emitter-base diode depends upon the nature of base lead connection. The most stringent requirement is realized by allowing the base to float. The next most stringent requirement is connecting the

*See references at end of Chapter 1.

base to the emitter through a resistor. A more lenient measurement is with base and emitter shorted. Finally, the condition yielding the highest breakdown voltage is that which applies reverse bias to the emitter-base junction. The symbols for the breakdown voltage, collector to emitter, under the foregoing base connection conditions are $V_{CEO}$, $V_{CER}$, $V_{CES}$, and $V_{CEX}$ respectively. On some specification sheets the letter B, signifying breakdown, precedes the voltage designation, i.e., $BV_{CEO}$.

The generic shape of breakdown characteristics differs among transistors fabricated by different processes. Figure 3.3 is typical of the planar epitaxial 2N2193. Note that the $BV_{CEO}$ curve exhibits little current flow ($I_{CEO}$) until breakdown is initiated. At breakdown a region of negative resistance appears and disappears at increased collector voltage. The region of negative resistance is not suitable for measurement and specification because of instability. The low current positive resistance region below (in voltage) the breakdown region is so low as to cause instrumentation difficulties. It is desirable, therefore, to measure breakdown voltage at a current, in the breakdown region, where the slope is positive. This current for the 2N2193 family is 25 ma.

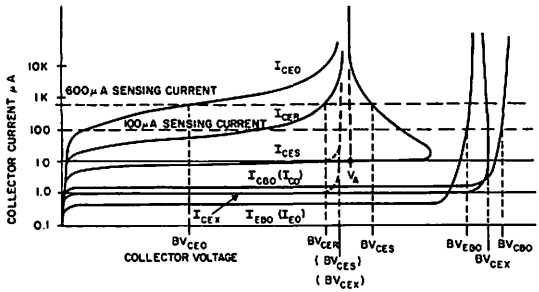
Since $BV_{CER}$ and $BV_{CEX}$ as well as $BV_{CEO}$ exhibit a negative resistance region, they must also be measured in a region of positive resistance. The voltage thus measured is always less than voltage needed to establish breakdown. For this reason it has been suggested that these voltages be named differently than breakdown voltages. One proposal is to designate them as "sustaining" voltages with the prefix letter L substituted for B, i.e., $LV_{CER}$. The nomenclature $V_{CER\,(sust.)}$ has also been used.




**TYPICAL PLANAR EPITAXIAL COLLECTOR BREAKDOWN CHARACTERISTICS**

**Figure 3.3**

The behavior of alloy devices is sufficiently different to warrant separate consideration. Figure 3.4 illustrates a typical family of breakdown characteristics. Since leakage currents are appreciable in this class of devices they form an important part of breakdown consideration. In the specification of $BV_{CEO}$, consideration must be given to $I_{co}$ multiplication. In this connection $I_{ceo}$ is approximately $h_{FE} \times I_{co}$. This product may exceed 100 $\mu$a (the usual $BV_{CBO}$ sensing current) at voltages well below breakdown. For this reason it is common to specify breakdown at a collector current of 600 $\mu$a. Figure 3.4 shows the realistic increase in voltage resulting from the use of a 600 $\mu$a sensing current. The earlier statement that $BV_{CEO}$ is a very conservative rating is particularly true of germanium alloy devices. It is primarily applicable to circuits with little or no stabilization.




**TYPICAL FAMILY OF ALLOY TRANSISTOR BREAKDOWN CHARACTERISTICS**

**Figure 3.4**

$BV_{CES}$ is measured with the base shorted to the emitter. It is an attempt to indicate more accurately the voltage range in which the transistor is useful. In practice, using a properly stabilized circuit, such as those described in Chapter 7, the emitter junction is normally forward biased to give the required base current. As temperature is increased, the resulting increase in $I_{co}$ and $h_{FE}$ requires that the base current decrease if a constant, i.e., stabilized, emitter current is to be maintained. In order that base current decrease, the forward bias voltage must decrease. A properly designed biasing circuit performs this function. If temperature continues to increase the biasing circuit will have to reverse bias the emitter junction to control the emitter current. This is illustrated by Figure 7.1 which shows that $V_{BE} = 0$ when $I_c = 0.5$ ma at 70°C for the 2N525. $V_{BE} = 0$ is identically the same condition as a base to emitter short as far as analysis is concerned. Therefore, the $BV_{CES}$ rating indicates what voltage can be applied to the transistor when the base and emitter voltages are equal, regardless of the circuit or environmental conditions responsible for making them equal. Figure 3.4 indicates a negative resistance region associated with $I_{CES}$. At sufficiently high currents the negative resistance disappears. The 600 $\mu$a sensing current intersects $I_{CES}$ in the negative resistance region in this example. Oscillations may occur depending on the circuit stray capacitance and the circuit load line. In fact, "avalanche" transistor oscillators are operated in just this mode.

Conventional circuit designs must avoid these oscillations. If the collector voltage does not exceed $V_A$ (Figure 3.4) there is no danger of oscillation. $V_A$ is the voltage at which the negative resistance disappears at high current.

To avoid the problems of negative resistance associated with $BV_{CES}$, $BV_{CER}$ was introduced. The base is connected to the emitter through a specified resistor. This condition falls between $BV_{CEO}$ and $BV_{CES}$ and for most germanium alloy transistors avoids creating a negative resistance region. For most low power transistors the resistor is 10,000Ω. The significance of $BV_{CER}$ requires careful interpretation. At low voltages the resistor tends to minimize the collector current as shown by equation (5q), in Chapter 5. Near breakdown the resistor becomes less effective permitting the collector current to increase rapidly.

Both the value of the base resistor and the voltage to which it is returned are important. If the resistor is connected to a forward biasing voltage the resulting base drive may saturate the transistor giving the illusion of a collector to emitter short. Returning the base resistor to the emitter voltage is the standard $BV_{CER}$ test condition. If the resistor is returned to a voltage which reverse biases the emitter junction, the

collector current will approach $I_{co}$. For example, many computer circuits use an emitter reverse bias of about 0.5 volts to keep the collector current at cut-off. The available power supplies and desired circuit functions determine the value of base resistance. It may range from 100 to 100,000 ohms with equally satisfactory performance provided the reverse bias voltage is maintained.

In discussing the collector to emitter breakdown so far, in each case the collector current is $I_{co}$ multiplied by a circuit dependent term. In other words all these collector to emitter breakdowns are related to the collector junction breakdown. They all depend on avalanche current multiplication.

Another phenomenon associated with collector to emitter breakdown is that of *reach-through* or *punch-through*. Silicon devices as typified by grown diffused, double diffused, planar, mesa, and planar epitaxial structures (see Chapter 2) do not exhibit this characteristic. The phenomenon of reach-through is most prevalent in alloy devices having thin base regions, and lighter base region doping than collector region doping. As reverse voltage is increased the depletion layer spreads more in the base than in the collector and eventually "reaches" into the emitter. An abrupt increase in current results.

The dotted lines in Figure 3.4 indicate the breakdown characteristics of a reach through limited transistor. Several methods are used to detect reach through. $BV_{CEX}$ (breakdown voltage collector to emitter with base reverse biased) is one practical method. The base is reverse biased by 1 volt. The collector current $I_{CEX}$ is monitored. If the transistor is avalanche limited $BV_{CEX}$ will approach $BV_{CBO}$. If it is reach-through limited it will approach $BV_{CES}$.

Note that $I_{CEX}$ before breakdown is less than $I_{co}$. Therefore, if $I_{co}$ is measured at a specified test voltage and then the emitter is connected with a reverse bias of 1 volt, the $I_{co}$ reading will decrease if reach-through is above the test voltage and will increase if it is below.

"Emitter floating potential" is another test for reach-through. If the voltage on an open-circuited emitter is monitored while the collector to base voltage is increased, it will remain within 500 mv of the base voltage until the reach-through voltage is reached. The emitter voltage then increases at the same rate as the collector voltage. $V_{RT}$ is defined as $(V_{CB} - 1)$ where $V_{CB}$ is the voltage at which $V_{EB} = 1v$.

## CURRENT

The absolute maximum collector current, shown as 1 ampere for the 2N2193, is a pulse current rating. In this case it is the maximum collector current for which $h_{FE}$ is specified. In some cases the current level at which $h_{FE}$ drops from its maximum value by 50% is specified. In all cases judgement concerning adverse life affects is a major consideration. Also in all cases no other absolute maximum rating can be exceeded in using this rating. In cases of very short, high current pulses, the power dissipated in transition from cutoff to saturation must be considered so that thermal ratings are not exceeded.

## TRANSISTOR DISSIPATION

Transistor dissipation ratings are thermal ratings, verified by life test, intended to limit junction temperature to a safe value. Device dissipation is shown for three cases. The first indicates the transistor in free air at an ambient temperature of 25°C. The 2N2193 under these conditions is capable of dissipating .8 watt. Further, we must derate at a rate of 4.6 mw/°C for an ambient temperature above 25°C. This thermal derating factor can be interpreted as the absolute maximum thermal conductance

junction to air, under the specified conditions. If dissipation and thermal conductance are specified at 25°C case temperature an infinite heat sink is implied and both dissipation and thermal conductance reach their largest allowable values. For the 2N2193 these are 2.8 watts and 16 mw/°C respectively.

Both free air and infinite heat sink ratings are valuable since they give limit application conditions from which intermediate (in thermal conductance) methods of heat sinking may be estimated.

### TEMPERATURE

The 2N2193 family carries a storage temperature rating extending from −65°C to +300°C. High temperature storage life tests substantiate continued compliance with the upper temperature extreme. Further, the mechanical design is such that thermal/mechanical stresses generated by rated temperature extremes cause no electrical characteristic degradation.

Operating junction temperature although stated implicitly by thermal ratings is also stated explicitly as an absolute maximum junction temperature.

## 3. ELECTRICAL CHARACTERISTICS

Electrical characteristics are the important properties of a transistor which are controlled to insure circuit interchangeability and describe electrical parameters.

### DC CHARACTERISTICS

The first characteristics shown are the voltage ratings, repeated in the order of the absolute maximum ratings, but this time showing the conditions of test. Note that these and subsequent electrical parameters are measured at 25°C ambient temperature unless otherwise noted. The 2N2193 has the highest rated breakdown voltages of the series at $V_{CBO} = 80V$, $V_{CEO} = 50V$, and $V_{EBO} = 8V$.

Forward current transfer ratio, $h_{FE}$, is specified over four decades of collector current from 100 microamperes to 1 ampere. Such wide range in collector current is feasible only in transistors having very small leakage currents. Note that $h_{FE}$ measurements at 150, 500 and 1000 ma. are made at a 2% duty cycle and pulse widths less than or equal to 300 microseconds. This precaution is necessary to avoid exceeding thermal ratings. Both the 2N2193 and 2N2193A have a specified minimum current gain at −55°C. A collector current of 10 ma. was chosen as being most useful to the circuit designer who wishes to predict low temperature circuit performance.

Base saturation, $V_{BE\ (SAT)}$, specifies the base input voltage characteristic under the condition of both junctions being foreward biased. The conditions of measurement specify a base current of 15 ma. and a collector current of 150 ma. Base-emitter drop is then 1.3 volts. This parameter is of particular interest in switch designs and is covered in further detail in Chapter 5 (Equations 5s & 5t).

Collector saturation voltage, $V_{CE\ (SAT)}$, is the electrical characteristic describing the voltage drop from collector to emitter with both base-emitter and collector-base junctions foreward biased. Base and collector currents are stipulated. For the 2N2193 through 2N2195 these are 15 ma. and 150 ma. respectively. The quotient of collector and base currents is termed "forced Beta."

The principal difference between "A" and "non-A" versions of the 2N2193 family lie in their maximum collector saturation voltages. "A" versions exhibit .16 volts typically and are specified at .25 volts maximum. The "non-A" versions are specified at .35 volts maximum. It is interesting to note that the 1.05 volt (minimum) difference

between $V_{BE\ (SAT)}$ and $V_{CE\ (SAT)}$ is the level of false trigger (noise immunity level) for DCTL switches. In germanium alloy devices this level is generally less than .3 volt and is seldom greater than .7 volt in other silicon devices (see Chapter 6). The wide difference in $V_{BE\ (SAT)}$ and $V_{CE\ (SAT)}$ is undesirable if Darlington connection of devices is desired for saturated switching. The collector saturation characteristic of the compound device demonstrates that the lead section is incapable of saturating the output section. Modification of the circuit to provide separate connection of the input section collector directly to the joint collector supply will provide the needed $V_{BE\ (SAT)}$ to allow output section saturation.

## CUTOFF CHARACTERISTICS

Chapter 6 contains a detailed study of transistor leakage currents. This examination deals with phenomena which predominate in alloy structures. The principal differences in planar epitaxial devices lie in the relative magnitudes of the leakage current components. The complete protection afforded by the passivation layer reduces surface leakage to a very small value. Further, it reduces the surface thermal component by decreasing recombination velocity. Figure 6.6(D) shows the variation with temperature of $I_{CBO}$ for units of the 2N2193 family. It is interesting to note that the theoretical semi-log plot of $I_{CBO}$ vs. temperature is a straight line. At high temperatures planar devices follow predicted behavior quite well. At lower temperatures, the temperature rate is considerably less than that which would be predicted by the theoretical model.

The 25°C $I_{CBO}$ and $I_{EBO}$ maximum limits are both 100 nanoamperes. $I_{CBO}$ rises to 25 microamperes at 150°C, typically, and carries a 150°C upper limit of 50 $\mu$a.

## HIGH FREQUENCY CHARACTERISTICS

The small-signal foreward current transfer ratio, $h_{fe}$, is shown as a minimum of 2.5 at 20 mc. This parameter is specified for those amplifier applications requiring control of high frequency $h_{fe}$. Chapter 15 treats the measurement of high frequency $h_{fe}$ in detail.

## SWITCHING CHARACTERISTICS

Chapters 6 and 15 on switching and measurements, respectively, discuss and define transient response times $t_d$, $t_r$, $t_s$, and $t_f$. The circuit used to measure $t_r$, $t_s$, and $t_f$ is shown in Figure 3.5. The specified maximum *rise, storage,* and *fall times* are measured in this circuit. The base of the transistor under test is clamped at approximately −1.5 volts by the diode returned to a −1 volt bus. As the point $V_{in}$ is raised in potential the base is unclamped and the transistor moved through the active region to saturation. As noted in the referenced chapters, the switching times measured are highly circuit

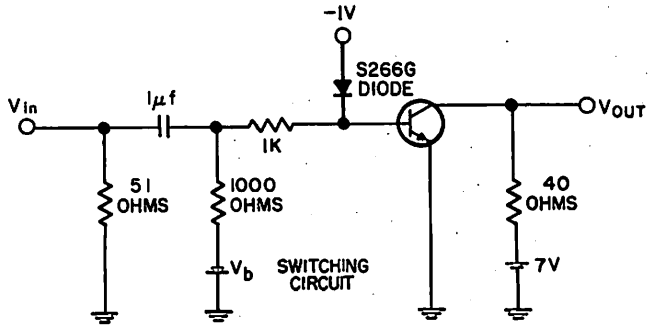


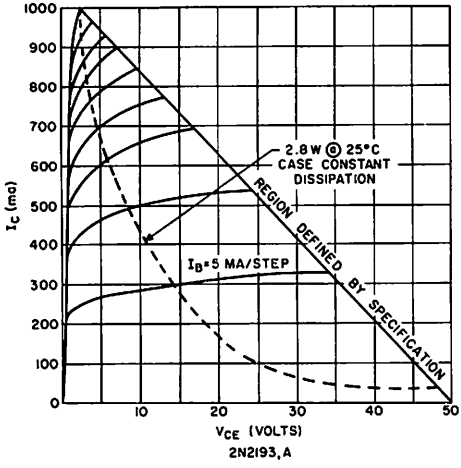

**Figure 3.5**

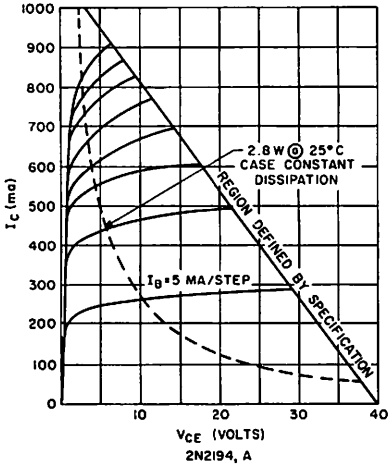
(2N2193, 2N2193A, 2N2194 AND 2N2194A ONLY)

dependent. By the time this description is published more thorough switching characterization will be made available, which specify $t_d$, $t_r$, $t_s$, and $t_f$ as a function of the ratio of collector current to foreward base current (forced beta).

## GENERIC CHARACTERISTICS

Much information about the behavior of semiconductor devices is conveyed by showing *typical* behavior. This information is presented graphically and differs from other electrical specifications by not bearing the high statistical assurance associated with maximum and minimum limits. Statistical confidence is assigned the generic characteristics of some devices by showing 5th, 50th, and 95th percentile points of a given characteristic. This sort of specification is found as part of very thoroughly characterized devices such as the 2N335 and 2N396.



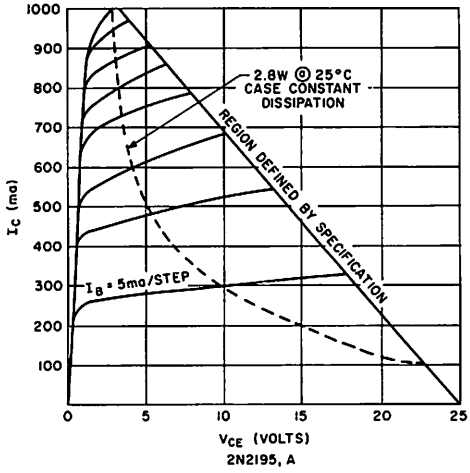




**Figure 3.6**

The specification sheet for the 2N2193 family includes collector family data for the 2N2193, 2N2194 and 2N2195 and associated "A" versions. The hyperbola of constant 2.8 watt 25°C dissipation is shown in Figure 3.6 to demark the area of permissible static operation as defined by previously discussed thermal limitations. In addition, a triangular area bounded by the collector current and collector voltage axes and a line noted as "region defined by specification" is specified. This area is one that defines the safe boundary for transient operation and should at no time be exceeded.

Semiconductor manufacturers go to great lengths in constructing their product specification sheets because they realize the value of offering the designer adequate information. If the device described therein is to be of use to the design engineer, is to be used properly for optimum performance and reliability by the designer within the limits specified by the manufacturer, the specification sheet must be accurate, complete, and reliable. This requires precise and time consuming measurements, coupled with costly hours of anlysis and preparation of the final specification sheet. The transistor specification sheet is, without doubt, the most important work tool the electronics circuit designer has at his disposal. When understood by the designer and used intelligently, many labor hours can be saved.

## EXPLANATION OF PARAMETER SYMBOLS

SYMBOL ELEMENTS

| | |
|---|---|
| A | Ampere (a.c., r.m.s or d.c.), ambient, anode electrode |
| a | Ampere (peak or instantaneous) |
| B, b | Base electrode, breakdown |
| C, c | Capacitance, collector electrode, cathode electrode |
| Δ | (Delta) A small change in the value of the indicated variable |
| E, e | Emitter electrode |
| F, f | Frequency, forward transfer ratio |
| G, g | Gain, acceleration of gravity, gate electrode |
| h | General symbol for hybrid parameter |
| I, i | Current, input, intrinsic region of device |
| J, j | Reference electrode |
| K, k | Unspecified (general) measurement electrode |
| L | Inductance |
| N, n | n-region of device |
| O, o | Output, open circuit |
| P, p | Power, P-region of device |
| Q | Charge |
| R, r | Resistance, reverse transfer ratio |
| T | Temperature |
| t | Time |

| | |
|---|---|
| V | Voltage (max., avg. or r.m.s) |
| v | Volt (peak or instantaneous) |
| W | Watt (Max., avg. or r.m.s) |
| w | Watt (peak or instantaneous) |
| X | Unspecified (general) parameter |
| Y | General symbol for an admittance parameter |
| θ | (Theta) Thermal resistance |
| Z, z | General symbol for impedance, impedance parameter |

## DECIMAL MULTIPLIERS

| Prefix | Abbreviation | Multiplier | Prefix | Abbreviation | Multiplier |
|---|---|---|---|---|---|
| tera | T | $10^{12}$ | milli | m | $10^{-3}$ |
| giga | G | $10^{9}$ | micro | $\mu$ | $10^{-6}$ |
| mega | M or Meg | $10^{6}$ | nano | n | $10^{-9}$ |
| kilo | K or k | $10^{3}$ | pico | p | $10^{-12}$ |

## PARAMETER SYMBOLS

| | |
|---|---|
| $BV_{CBO}$ | *DC breakdown voltage collector to base junction reverse biased, emitter open-circuited (value of $I_C$ should be specified). |
| $BV_{CEO}$ | *DC breakdown voltage, collector to emitter, with base open-circuited. This may be a function of both "m" (the charge carrier multiplication factor) and the $h_{fb}$ of the transistor. Specify $I_C$. |
| $BV_{CER}$ | *DC breakdown voltage, similar to $BV_{CEO}$ except a resistor value "R" between base and emitter. |
| $BV_{CES}$ | *DC breakdown voltage, similar to $BV_{CEO}$ but base shorted to emitter. |
| $BV_{CEV}$ | *DC breakdown voltage, similar to $BV_{CEO}$ but emitter to base junction reverse biased. |
| $BV_{CEX}$ | *DC breakdown voltage, similar to $BV_{CEO}$ but emitter to base junction reverse biased through a specified circuit. |
| $BV_{EBO}$ | *DC breakdown voltage, emitter to base junction reverse biased, collector open-circuited. Specify $I_E$. |
| $BV_R$ | DC breakdown voltage, reverse biased diode. |
| $C_c$ | Barrier capacitance. |
| $C_{eb}$ | *(Common base) capacitance emitter to base, collector open. |
| $C_{ij}$ | Input capacitance. |
| $C_{ob}$ | *(Common base) collector to base — Output capacitance measured across the output terminals. |
| $C_{oe}$ | *(Common emitter) collector to emitter. — Output capacitance measured across the output terminals. |

| | |
|---|---|
| f | Frequency at which measurement is performed. |
| $f_{hfb}$ ($f_{\alpha b}$) | (Common base) small-signal short-circuit forward current transfer ratio cut-off frequency. |
| $f_{hfe}$ ($f_{\alpha e}$) | (Common emitter) small-signal short-circuit forward current transfer ratio cut-off frequency. |
| $f_{max}$ ($f_{osc}$) | Maximum frequency of oscillation. |
| $f_t$ | Gain bandwidth product frequency at which the small signal, common emitter, short-circuit, forward current, transfer ratio ($h_{fe}$) is unity or zero db. |
| $-g$ | Negative Conductance. |
| $G_{pb}$ | *(Common base) small-signal power gain. |
| $G_{PE}$ | *(Common emitter) large-signal power gain. |
| $G_{pe}$ | *(Common emitter) small-signal power gain. |
| $G_{pe}$ (CONV.) | *(Common emitter) conversion gain. |
| $h_{fb}$ | (Common base) — Small-signal short-circuit forward current transfer ratio, output ac short-circuited. |
| $h_{fc}$ | (Common collector) |
| $h_{fe}$ | (Common emitter) |
| $h_{fj}$ | (General) |
| $h_{FE}$ | *(Common emitter) static value of forward current transfer ratio, $h_{FE} = \frac{I_C}{I_B}$ |
| $h_{FE}$ (inv.) | Inverted $h_{FE}$ (emitter and collector leads switched) |
| $h_{ib}$, $h_{ie}$, $h_{ic}$, $h_{ij}$ | (Common base, common emitter, common collector, general) small-signal input impedance, output ac short-circuited. |
| $h_{IE}$ | (Common emitter) static value of the input resistance. |
| $h_{ie}$ (real) | (Common emitter) real part of the small-signal value of the short-circuit input impedance at high frequency. |
| $h_{ob}$, $h_{oe}$, $h_{oc}$, $h_{oj}$ | (Common base, common emitter, common collector, general) small-signal, output admittance, input ac open-circuited. |
| $h_{rb}$, $h_{re}$, $h_{rc}$, $h_{rj}$ | (Common base, common emitter, common collector, general) small-signal, reverse voltage transfer ratio, input ac open-circuited. |
| I, i | Region of a device which is intrinsic and in which neither holes nor electrons predominate. |

| | |
|---|---|
| $I_B$, $I_C$, $I_E$ | DC currents into base, collector, or emitter terminal. |
| $I_b$ | Base current (rms) |
| $i_b$ | Base current ( instantaneous) |
| $I_{BX}$ | DC base current with both the emitter and collector junctions reverse biased. |
| $I_c$ | Collector current (rms) |
| $i_c$ | Collector current (instantaneous) |
| $I_{CBO}$ ( $I_{CO}$) | *DC collector current when collector junction is reverse biased and emitter is open-circuited. |
| $I_{CEO}$ | *DC collector current with collector junction reverse biased and base open-circuited. |
| $I_{CER}$ | *DC collector current with collector junction reverse biased and a resistor of value "R" between base and emitter. |
| $I_{CES}$ | *DC collector current with collector junction reverse biased and base shorted to emitter. |
| $I_{CEV}$ | *DC collector current with collector junction reverse biased and with a specified base-emitter voltage. |
| $I_{CEX}$ | *DC collector current with collector junction reverse biased and with a specified base-emitter circuit connection. |
| $I_e$ | Emitter current (rms) |
| $i_e$ | Emitter current (instantaneous) |
| $I_{EBO}$ ($I_{EO}$) | *DC emitter current when emitter junction is reverse biased and collector is open-circuited. |
| $I_{ECS}$ | *DC emitter current with emitter junction reverse biased and base shorted to collector. |
| $I_F$ | *DC forward current. |
| $i_F$ | Forward current (instantaneous). |
| $I_P$ | Peak Point current. |
| $I_P/I_V$ | Peak to Valley current ration. |
| $I_R$ | Reverse Current (DC). |
| $i_R$ | Reverse Current (instantaneous). |

| | |
|---|---|
| $I_V$ | Valley Point Current. |
| $L_c$ | Conversion loss – ratio of available signal power to the available intermediate frequency power. |
| $L_S$ | Total series inductance. |
| N, n | Region of a device where electrons are the majority carriers. |
| $\eta$ | Intrinsic stand-off ratio (unijunction). |
| NF | Noise Figure. |
| P, p | Region of a device where holes are the majority carriers. |
| $p_t$ (peak) | Peak collector power dissipation for a specified time duration, duty cycle and wave shape. |
| $P_C$ | Average continuous collector power dissipation. |
| $P_o$ | Power output. |
| pt (peak) | Peak total power dissipation for a specified time, duration, duty cycle and wave shape. |
| $P_T$ | Average continuous total power dissipation. |
| $Q_{SB}$ | Stored base charge. |
| $r_b'$ | Base spreading resistance equals $h_{ie}$ (real) when $h_{ie}$ (imaginary) = 0. |
| $r_{B1B2_0}$ ($r_{BBO}$) | Device resistance between base 1 and base 2, emitter open-circuited (interbase resistance – unijunction). |
| $r_{CE(SAT)}$ | Device resistance, collector to emitter, under saturation conditions (saturation resistance, steady state). |
| RE | Rectification Efficiency (voltage). |
| $R_{KJ}$ | Circuit resistance between terminals K and J. |
| $R_L$ | Load resistance. |
| $r_s$ | Small signal series resistance. |
| $T_A$ | Operating Temperature (ambient) |
| $T_J$ | Junction Temperature |

| | |
|---|---|
| $T_{STG}$ | Storage Temperature |
| $V_{KJ}$ | Circuit voltage between terminals K and J. |
| $V_P$ | Peak point voltage. |
| $V_R$ | DC reverse voltage. |
| $V_{RT}$ | DC voltage reach-through (formerly called punch-through $C_{PT}$). At collector voltages above reach-through $V_{RT} = V_{CB} - V_{EB}$. ($V_{EB}$ normally defined as 1 volt). |
| $V_V$ | Valley point voltage. |
| $y_{fj}$ | Small signal short circuit forward transfer admittance. |
| $z_{ij}$ | Input impedance. |
| $z_{oj}$ | Output impedance. |

*Test conditions must be specified.

NOTE: DC voltage and current terminologies (as listed herein) are valid only when measurements are made under non-oscillating conditions. Care must be exercised with Avalanche Transistors as they may oscillate when making these measurements and give erroneous readings.

## ABBREVIATED DEFINITIONS OF TERMS

1. Absolute Max. Ratings – the value when so specified is an "absolute limit" and the device is not guaranteed if it is exceeded.

2. Applied Voltage – voltage applied between a terminal and the reference point.

*3. Constant Current – one that does not produce a parameter value change greater than the required precision of the measurement when the generator impedance is halved.

*4. Constant Voltage – one that does not produce a parameter value change greater than the required precision of the measurement when the genrator impedance is doubled.

*5. Breakdown Voltage (BV) – that value of applied reverse voltage which remains essentially constant over a considerable range of current values, or where the incremental resistance = 0 at the lowest current in avalanche devices.

6. Limits – the minimum and maximum values specified.

7. Noise Figure (NF) – at a selected input frequency, the noise figure (usually 10 log of base 10 of ratio) is the ratio of the total noise power per unit bandwidth at a corresponding output frequency delivered to the output termination, to the portion thereof engendered at the input frequency by the input termination, (whose noise temperature is standard 290°K).

8. Open Circuit – a condition such that halving the magnitude of the terminating impedance does not produce a change in the parameter measured greater than the required precision of the measurement.

9. Pulse – a flow of energy of short duration which conveys intelligence.

10. Pulse Average Time ($t_w$) – the time duration from a point on the leading edge which is 50% of the maximum amplitude to a point on the trailing edge which is 50% of the maximum amplitude.

11. Pulse Delay Time ($t_d$) – the time interval from a point on the leading edge of the input pulse which is 10% of its maximum amplitude to a point on the leading edge of the output pulse which is 10% of its maximum amplitude.

12. Pulse Fall Time ($t_f$) – the time duration during which the amplitude of its trailing edge decreases from 90 to 10% of the maximum amplitude.

13. Pulse Rise Time ($t_r$) – the time duration during which the amplitude of its leading edge increases from 10 to 90% of the maximum amplitude.

14. Pulse Storage Time ($t_s$) – the time interval from a point 10% down from the maximum amplitude on the trailing edge of the input pulse to a point 10% down from the maximum amplitude on the trailing edge of the output pulse.

15. Pulse Time ($t_p$) – the time interval from a point on the leading edge which is 90% of the maximum amplitude to a point on the trailing edge which is 90% of the maximum amplitude.

16. Short Circuit – a condition where doubling the magnitude of the terminating impedance does not produce a change in the parameter being measured that is greater than the required precision of the measurement.

17. Small Signal – a signal is considered small when halving its magnitude does not produce a change in the parameter being measured that is greater than the required precision of the measurement.

18. Spike – an unintended flow of electrical energy of short duration.

19. Supply Voltage ($V_{BB}$, $V_{CC}$, $V_{EE}$) – the potential of the circuit power source.

20. Thermal Equilibrium – a condition where doubling the test time does not produce a change in the parameter that is greater than the required precision of the measurement.

21. Thermal Resistance ($\Theta$) – the temperature rise per unit power dissipation of the junction above the device case or ambient temperature under conditions of steady-state operation (where applicable, "case" means device mounting surface).

22. Thermal Response Time ($\gamma_r$) – the time required for the junction temperature to reach 90% of the final value of junction temperature change caused by a step function in power dissipation when the device case or ambient temperature is held constant.

23. Thermal Time Constant ($\gamma_t$) – the time required for the junction temperature to reach 63.2% of the final value of junction temperature change caused by step function in power dissipation when the device case or ambient temperature is held constant.

24. Base Voltage ($V_{BJ}$) – the voltage between the base terminal and the reference point (J).

25. Collector Voltage ($V_{CJ}$) – the voltage between the collector terminal and the reference point (J).

26. Cut-off Current ($I_{KJO}$, $I_{KJR}$, $I_{KJS}$, $I_{KJV}$, $I_{KJX}$) – the measured value of (K) electrode DC current when it is reverse-biased by a voltage less than the breakdown voltage and the other electrode(s) is (are) DC open-circuited ($I_{KJO}$) or:

1. returned to the reference electrode (J) through a given resistance ($I_{KJR}$)
2. DC short circuited to the reference electrode (J) ($I_{KJS}$)
3. reverse-biased by a specified voltage ($I_{KJV}$)
4. under a specified set of conditions different from the above ($I_{KJX}$).

27. Depletion Layer Capacitance (C dep) – the transition capacitance of a reverse-biased PN junction. (Small signal as well as DC conditions to be stated).

28. Diffusion Capacitance (C dif) – the transition capacitance of a forward biased (with an appreciable current flow) PN junction.

29. Emitter Voltage ($V_{EJ}$) – the voltage between the emitter terminal and the reference point (J).

30. Floating Potential ($V_{KJF}$) – the DC voltage between the open circuit terminal (K) and the reference point (J) when a DC voltage is applied to the third terminal and the reference terminal.

31. Input Capacitance ($C_{ij}$) – the shunt capacitance at the input terminals.

32. Input Terminals – the terminals to which input voltage and current are applied.

33. Inverse Electrical Characteristics [$X_{KJ}$(INV)] – those characteristics obtained when the collector and emitter terminals are interchanged.

34. Large-signal Short Circuit Forward-current Transfer Ratio ($h_{FJ}$) – ratio of the change in output current ($\Delta I_o$) to the corresponding change in input current ($\Delta I_i$).

35. Large-signal Transconductance ($G_{MJ}$) – the ration of the change in output current ($\Delta I_o$) to the corresponding change in input voltage ($\Delta V_i$).

36. Large-signal Power Gain ($G_P$) – the ratio of the ac output power to the ac input power under the large signal conditions. Usually expressed in decibels (db). (ac conditions must be specified).

37. Maximum Frequency of Oscillation ($f_{osc}$ or $f_{max}$) – the highest frequency at which a device will oscillate in a particular circuit.

38. Output Capacitance ($C_{oj}$) – the shunt capacitance at the output terminals.

39. Output Terminals – the terminals at which the output voltage and current may be measured.

40. Power Gain Cut-off Frequency ($f_{pj}$) – that frequency at which the power output has dropped 3 db from its value at a reference test frequency ($G_P(f) = \text{constant}$) with constant input power.

41. Reach Through Voltage ($V_{RT}$) (formerly referred to as "punch through voltage") – that value of reverse voltage at which the reverse-biased PN junction spreads sufficiently to electrically contact any other junction or contact, and thus act as a short circuit.

42. Real Part of Small Signal Short-circuit Input Impedance [$h_{ij}$ (real)] – the real part of the ratio of ac input voltage to the ac input current with zero ac output voltage.

43. Reference Point (electrical) – the terminal that is common to both the input and output circuits.

44. Saturation Resistance [$r_{KJ}(SAT)$] – the ratio of saturation voltage to the measurement (K) electrode DC current.

45. Saturation Voltage [$V_{KJ}(SAT)$] – the DC voltage between the measurement electrode (K) and the reference electrode (J) for the saturation conditions specified.

46. Small-signal Open-circuit Forward Transfer Impedance ($z_{fj}$) – the ratio of the ac output voltage to the ac input current with zero ac output current.

47. Small-signal Open-circuit Input Impedance ($z_{ij}$) – the ratio of the ac input voltage to the ac input current with zero ac output current.

48. Small-signal Open-circuit Output Admittance ($h_{oj}$) – the ratio of the ac output current to the ac voltage applied to the output terminals with zero ac input current.

49. Small-signal Open-circuit Output Impedance ($z_{oj}$) – the ratio of the ac voltage applied to the output terminals to the ac output current with zero ac input current.

50. Small-signal Open-circuit Reverse Transfer Impedance ($z_{rj}$) – the ratio of the ac input voltage to the ac output current with zero ac input current.

51. Small-signal Open-circuit Reverse Voltage Transfer Ratio ($h_{rj}$) – the ratio of the ac input voltage to the ac output voltage with zero ac input current.

52. Small-signal Power Gain ($G_p$) – the ratio of the ac output power to the ac input power. Usually expressed in db.

53. Small-signal Short-circuit Forward Current Transfer Ratio ($h_{fj}$) – the ratio of the ac output current to the ac input current with zero ac output voltage.

54. Small-signal Short-circuit Forward Current Transfer Ratio Cut-off Frequency ($f_{hfj}$) – the frequency in cycles per second (cps) at which the absolute value of this ratio is 0.707 times its value at the test frequency specified ($G_p(f)$ = constant).

55. Small-signal Short-circuit Forward Transfer Admittance ($y_{fj}$) – the ratio of the ac output current to the ac input voltage with zero ac output voltage.

56. Small-signal Short-circuit Input Impedance ($h_{ij}$) – the ratio of the ac input voltage to the ac input current with zero ac output voltage.

57. Forward Voltage ($V_{FP}$) – highest value of positive voltage at which the forward current equals the maximum specified peak point current ($I_F = I_P$).

58. Peak Point Current ($I_P$) – value of the static current flowing at the lowest positive voltage at which $\frac{dI}{dV} = 0$.

59. Peak Point Voltage ($V_P$) – the lowest positive voltage at which $\frac{dI}{dV} = 0$.

60. Peak to Valley Ratio $\frac{I_P}{I_V}$ – the ratio of peak point current to valley point current.

61. Valley Point Current ($I_V$) – the value of the static current flowing at the second lowest positive voltage at which $\frac{dI}{dV} = 0$.

62. Valley Point Voltage ($V_V$) – the second lowest positive voltage at which $\frac{dI}{dV} = 0$.

*Test conditions must be specified.

# SMALL SIGNAL CHARACTERISTICS

CHAPTER 4

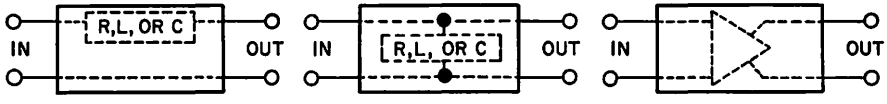
A major area of transistor applications is in various types of low level a-c amplifiers. One example is a phonograph preamplifier where the output of a phonograph pickup (generally about 8 millivolts) is amplified to a level suitable for driving a power amplifier (generally 1 volt or more). Other examples of low level or small signal amplifiers include the IF and RF stages of radio and TV receivers and preamplifiers for servo systems.

As described in Chapter 5, Large Signal Characteristics, a transistor can have very nonlinear characteristics when used at low current and voltage levels. For example, if conduction is to take place in an NPN transistor the base must be positive with respect to the emitter. Thus, if an a-c signal were applied to the base of an NPN transistor, conduction would take place only during the positive half cycle of the applied signal and the amplified signal would be highly distorted. To make possible linear or undistorted amplification of small signals, fixed d-c currents and voltages are applied to the transistor simultaneously with the a-c signal. This is called *biasing* the transistor, and the d-c collector current and d-c collector to emitter voltage are referred to as the *bias conditions*. When bias conditions are chosen so that the largest a-c signal to be amplified is small compared to the d-c bias current and voltage, the transistor is said to be operating in *small signal mode*.

Transistors used in small signal amplifiers are normally biased at currents between 0.5 and 10 ma. and voltages between 2 and 10 volts. Bias currents and voltages below this range can cause problems of distortion, while bias currents and voltages above this range can cause problems of excessive noise and power dissipation.

For the purpose of circuit design, any component, including the transistor, can be considered as a *black-box* (B-B) having two input terminals and two output terminals. With the help of Matrix Theory the circuit designer, knowing the electrical characteristics of the black-box, can calculate the performance of the amplifier when various signal sources are applied to its input and various loads are connected to its output.

Although possibly foreboding in name Matrix Theory is, in fact, easy to understand and apply. The relative ease with which it may be used in circuit analysis, compared to other analysis methods, makes the understanding of it a "must" for the circuit design engineer. When certain stipulations are made, Matrix Theory is perfectly applicable to circuits involving active elements like the transistor. Its use is virtually mandatory in complicated circuits involving feedback, particularly where the preservation of the sanity of the analyst is considered necessary.

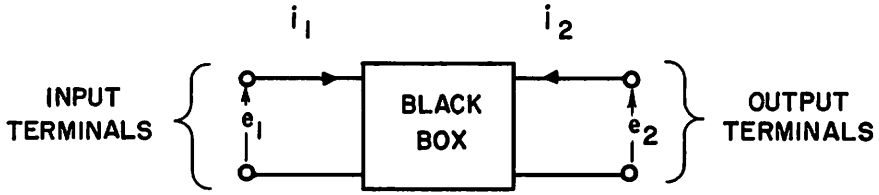



**EXAMPLES OF BLACK-BOXES**

**Figure 4.1**

Basically, the matrix method of analysis involves the black-box concept where the fundamental components or groups of components of a circuit (inductors, capacitors, resistors, and active elements) are considered as black-boxes having two input and two output terminals.

Conventionally the input terminals are on the left side of the box with the corresponding output terminals on the other side. There is also a convention regarding the input and output potentials and currents shown in Figure 4.2.




**BLACK-BOX SHOWING INPUT AND OUTPUT CONVENTION**

**Figure 4.2**

In a sensible black-box, there is a well-defined relationship between the input voltage and current and the corresponding quantities at the output. The most often realized and most easily handled functional relationship is linearity. A pair of linear equations will then completely represent the black-box. As an example, consider the following which are equations expressing the input and output voltages in terms of input and output current

$$e_1 = Z_{11}i_1 + Z_{12}i_2 \tag{4a}$$

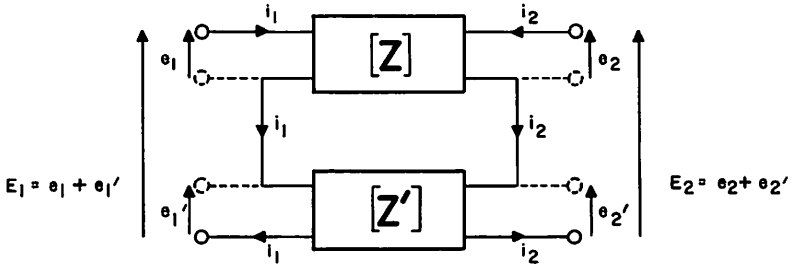
$$e_2 = Z_{21}i_1 + Z_{22}i_2 \tag{4b}$$

$Z_{11}$, $Z_{12}$, $Z_{21}$, $Z_{22}$ have the dimensions of impedance and are called the "impedance parameters" of the black-box.

The matrix equation equivalent to (4a) and (4b) is

$$\begin{bmatrix} e_1 \\ e_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad \text{or more concisely} \quad [e] = [Z]\,[i] \tag{4c}$$

Z parameters are useful when two or more black-boxes are connected together such that their input terminals are connected in series and their output terminals are also in series as shown in Figure 4.3.




**BLACK-BOXES WITH SERIES CONNECTIONS AT INPUT AND OUTPUT**

**Figure 4.3**

Because of the method of connection $i_1$ and $i_2$ are the same as for a single B-B. The $e_1$'s are added, as are the $e_2$'s.

$$\begin{bmatrix} E_1 \\ E_2 \end{bmatrix} = [\text{Z combined}] \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{4d}$$

Z combined is the matrix of the single black-box which is equivalent to the two black-boxes combined. $E_1 = e_1 + e_1'$, $E_2 = e_2 + e_2'$.

$$\begin{bmatrix} E_1 \\ E_2 \end{bmatrix} = \begin{bmatrix} e_1 + e_1' \\ e_2 + e_2' \end{bmatrix} = [Z] \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} + [Z'] \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{4e}$$

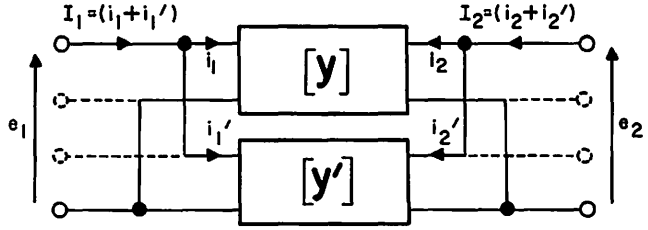
$$[E] = \Big( [Z] + [Z'] \Big) \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{4f}$$

Matrix theory tells us that Z + Z' is obtained by simple summing of the individual terms of the matrixes, i.e.

$$\begin{bmatrix} E_1 \\ E_2 \end{bmatrix} = \begin{bmatrix} Z_{11} + Z_{11}' & Z_{12} + Z_{12}' \\ Z_{21} + Z_{21}' & Z_{22} + Z_{22}' \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{4g}$$

Therefore the two original B-B's may be replaced by one B-B having the parameters shown in equation (4g).

If two black-boxes are to have their input terminals paralleled and their output terminals paralleled also, then a different set of original equations is set up.




**BLACK-BOXES IN PARALLEL**

**Figure 4.4**

The currents are now additive, voltages $e_1$ and $e_2$ are the same for the combination as for the individual B-B's. The currents $i_1$ and $i_2$ have to appear on the left hand side of the two equations.

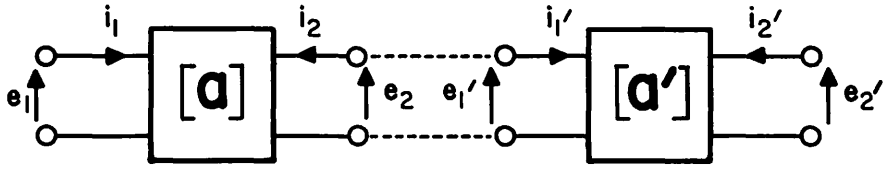
$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} \tag{4h}$$

The "y" parameters have the dimensions of conductance and are called the "admittance parameters." So far the parallel combination of two black-boxes

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} i_1 + i_1' \\ i_2 + i_2' \end{bmatrix} = \Big( [y] + [y'] \Big) \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} \tag{4i}$$

$$[I] = \begin{bmatrix} y_{11} + y_{11}' & y_{12} + y_{12}' \\ y_{21} + y_{21} & y_{22} + y_{22}' \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} \tag{4j}$$

For cascaded black-boxes yet another set of parameters called "a" parameters has to be established and these are perhaps the most useful of any.




**BLACK-BOXES IN CASCADE**
**Figure 4.5**

Notice in Figure 4.5, $e_1'$ is the same as $e_2$ since their respective terminals are connected together. However, $i_1' = -i_2$ but the sign is taken care of by making the basic equation of this form

$$\left.\begin{aligned} e_1 &= a_{11}\, e_2 - a_{12}\, i_2 \\ i_1 &= a_{21}\, e_2 - a_{22}\, i_2 \end{aligned}\right\} \begin{bmatrix} e_1 \\ i_1 \end{bmatrix} = [a] \begin{bmatrix} e_2 \\ -i_2 \end{bmatrix} \tag{4k}$$

So, the over-all equation for the two cascaded B-B's shown in Figure 4.5, is

$$\begin{bmatrix} e_1 \\ i_1 \end{bmatrix} = [A] \begin{bmatrix} e_2' \\ -i_2' \end{bmatrix} \tag{4l}$$

For the individual B-B's the two matrix equations are

$$\begin{bmatrix} e_1 \\ i_1 \end{bmatrix} = [a] \begin{bmatrix} e_2 \\ -i_2 \end{bmatrix} \text{ and } \begin{bmatrix} e_1' \\ i_1' \end{bmatrix} = [a'] \begin{bmatrix} e_2' \\ -i_2' \end{bmatrix} \tag{4m) (4n}$$

but $e_2 = e_1'$, and $-i_2 = i_1'$

therefore

$$\begin{bmatrix} e_1 \\ i_1 \end{bmatrix} = [a] \begin{bmatrix} e_1' \\ i_1' \end{bmatrix} = [a] \times [a'] \begin{bmatrix} e_2' \\ -i_2' \end{bmatrix} \tag{4o}$$

$$[A] = [a] \times [a'] \tag{4p}$$

and the "a" matrix is called the "multiplier matrix" for obvious reasons.

Matrix theory tells us that the expansion of $[a] \times [a']$ is done as follows

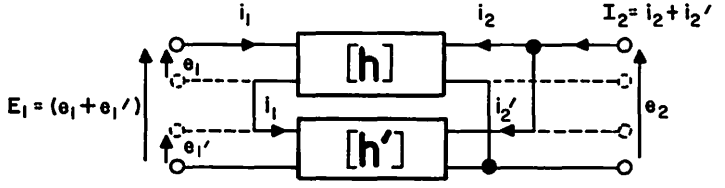
$$[a] \times [a'] = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \times \begin{bmatrix} a_{11}' & a_{12}' \\ a_{21}' & a_{22}' \end{bmatrix}$$

$$= \begin{bmatrix} (a_{11}\, a_{11}' + a_{12}\, a_{21}'), (a_{11}\, a_{12}' + a_{12}\, a_{22}') \\ (a_{21}\, a_{11}' + a_{22}\, a_{21}'), (a_{21}\, a_{12}' + a_{22}\, a_{22}') \end{bmatrix}$$

therefore

$$\begin{bmatrix} e_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} (a_{11}\, a_{11}' + a_{12}\, a_{21}'), (a_{11}\, a_{12}' + a_{12}\, a_{22}') \\ (a_{21}\, a_{11}' + a_{22}\, a_{21}'), (a_{21}\, a_{12}' + a_{22}\, a_{22}') \end{bmatrix} \begin{bmatrix} e_2' \\ -i_2' \end{bmatrix} \tag{4q}$$

When inputs are "seriesed" and outputs "paralleled," a set of parameters called the "h" parameters is obtained to represent the B-B's as shown in Figure 4.6.




**BLACK-BOXES WITH INPUTS IN SERIES AND OUTPUTS IN PARALLEL**

**Figure 4.6**

For the first B-B

$$\begin{bmatrix} e_1 \\ i_2 \end{bmatrix} = [h] \begin{bmatrix} i_1 \\ e_2 \end{bmatrix} \tag{4r}$$

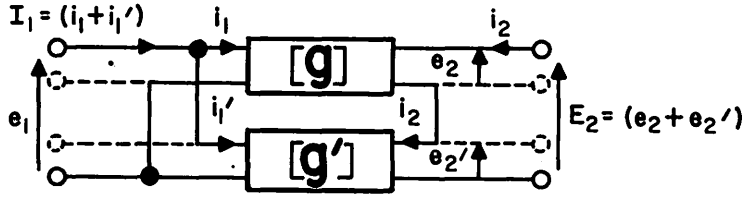
for the second B-B

$$\begin{bmatrix} e_1' \\ i_2' \end{bmatrix} = [h'] \begin{bmatrix} i_1 \\ e_2 \end{bmatrix} \tag{4s}$$

For the combination

$$\begin{bmatrix} E_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} e_1 + e_1' \\ i_2 + i_2' \end{bmatrix} = \Big( [h] + [h'] \Big) \begin{bmatrix} i_1 \\ e_2 \end{bmatrix} \tag{4t}$$

Finally the "g" parameters, those used when analyzing B-B configurations wherein the B-B inputs are "paralleled" and the outputs are "seriesed."




**BLACK-BOXES WITH INPUTS IN PARALLEL AND OUTPUTS IN SERIES**

**Figure 4.7**

For the first B-B

$$\begin{bmatrix} i_1 \\ e_2 \end{bmatrix} = [g] \begin{bmatrix} e_1 \\ i_2 \end{bmatrix} \tag{4u}$$

for the second B-B

$$\begin{bmatrix} i' \\ e_2' \end{bmatrix} = [g'] \begin{bmatrix} e_1 \\ i_2 \end{bmatrix} \tag{4v}$$

therefore for the combination

$$\begin{bmatrix} I_1 \\ E_2 \end{bmatrix} = \begin{bmatrix} i_1 + i_1' \\ e_2 + e_2' \end{bmatrix} = \Big( [g] + [g'] \Big) \begin{bmatrix} e_1 \\ i_2 \end{bmatrix} \tag{4w}$$

Knowing one set of the above established parameters, the others may be worked out, or more conveniently, obtained from Figure 4.8.

## MATRIX INTERRELATIONS

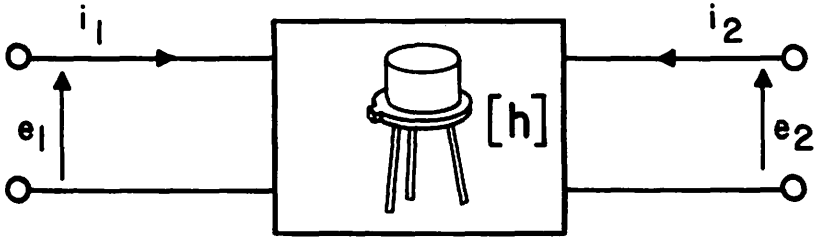
| FROM / TO | → [z] | [y] | [h] | [g] | [a] |
|---|---|---|---|---|---|
| [z] | $z_{11}$ $z_{12}$<br>$z_{21}$ $z_{22}$ | $\frac{y_{22}}{\Delta^y}$ $\frac{-y_{12}}{\Delta^y}$<br>$\frac{-y_{21}}{\Delta^y}$ $\frac{y_{11}}{\Delta^y}$ | $\frac{\Delta^h}{h_{22}}$ $\frac{h_{12}}{h_{22}}$<br>$\frac{-h_{21}}{h_{22}}$ $\frac{1}{h_{22}}$ | $\frac{1}{g_{11}}$ $\frac{-g_{12}}{g_{11}}$<br>$\frac{g_{21}}{g_{11}}$ $\frac{\Delta^g}{g_{11}}$ | $\frac{a_{11}}{a_{21}}$ $\frac{\Delta^a}{a_{21}}$<br>$\frac{1}{a_{21}}$ $\frac{a_{22}}{a_{21}}$ |
| [y] | $\frac{z_{22}}{\Delta^z}$ $\frac{-z_{12}}{\Delta^z}$<br>$\frac{-z_{21}}{\Delta^z}$ $\frac{z_{11}}{\Delta^z}$ | $y_{11}$ $y_{12}$<br>$y_{21}$ $y_{22}$ | $\frac{1}{h_{11}}$ $\frac{-h_{12}}{h_{11}}$<br>$\frac{h_{21}}{h_{11}}$ $\frac{\Delta^h}{h_{11}}$ | $\frac{\Delta^g}{g_{22}}$ $\frac{g_{12}}{g_{22}}$<br>$\frac{-g_{21}}{g_{22}}$ $\frac{1}{g_{22}}$ | $\frac{a_{22}}{a_{12}}$ $\frac{-\Delta^a}{a_{12}}$<br>$\frac{-1}{a_{12}}$ $\frac{a_{11}}{a_{12}}$ |
| [h] | $\frac{\Delta^z}{z_{22}}$ $\frac{z_{12}}{z_{22}}$<br>$\frac{-z_{21}}{z_{22}}$ $\frac{1}{z_{22}}$ | $\frac{1}{y_{11}}$ $\frac{-y_{12}}{y_{11}}$<br>$\frac{y_{21}}{y_{11}}$ $\frac{\Delta^y}{y_{11}}$ | $h_{11}$ $h_{12}$<br>$h_{21}$ $h_{22}$ | $\frac{g_{22}}{\Delta^g}$ $\frac{-g_{12}}{\Delta^g}$<br>$\frac{-g_{21}}{\Delta^g}$ $\frac{g_{11}}{\Delta^g}$ | $\frac{a_{12}}{a_{22}}$ $\frac{\Delta^a}{a_{22}}$<br>$\frac{-1}{a_{22}}$ $\frac{a_{21}}{a_{22}}$ |
| [g] | $\frac{1}{z_{11}}$ $\frac{-z_{12}}{z_{11}}$<br>$\frac{z_{21}}{z_{11}}$ $\frac{\Delta^z}{z_{11}}$ | $\frac{\Delta^y}{y_{22}}$ $\frac{y_{12}}{y_{22}}$<br>$\frac{-y_{21}}{y_{22}}$ $\frac{1}{y_{22}}$ | $\frac{h_{22}}{\Delta^h}$ $\frac{-h_{12}}{\Delta^h}$<br>$\frac{-h_{21}}{\Delta^h}$ $\frac{h_{11}}{\Delta^h}$ | $g_{11}$ $g_{12}$<br>$g_{21}$ $g_{22}$ | $\frac{a_{21}}{a_{11}}$ $\frac{-\Delta^a}{a_{11}}$<br>$\frac{1}{a_{11}}$ $\frac{a_{12}}{a_{11}}$ |
| [a] | $\frac{z_{11}}{z_{21}}$ $\frac{\Delta^z}{z_{21}}$<br>$\frac{1}{z_{21}}$ $\frac{z_{22}}{z_{21}}$ | $\frac{-y_{22}}{y_{21}}$ $\frac{-1}{y_{21}}$<br>$\frac{-\Delta^y}{y_{21}}$ $\frac{-y_{11}}{y_{21}}$ | $\frac{-\Delta^h}{h_{21}}$ $\frac{-h_{11}}{h_{21}}$<br>$\frac{-h_{22}}{h_{21}}$ $\frac{-1}{h_{21}}$ | $\frac{1}{g_{21}}$ $\frac{g_{22}}{g_{21}}$<br>$\frac{g_{11}}{g_{21}}$ $\frac{\Delta^g}{g_{21}}$ | $a_{11}$ $a_{12}$<br>$a_{21}$ $a_{22}$ |

NOTE: Δ REPRESENTS THE DETERMINANT ($\Delta_z = Z_{11} Z_{22} - Z_{21} Z_{12}$)

**Figure 4.8**

The restriction placed on the derivation of the various black-box parameters is that the equations connecting input and output voltages and currents shall be linear. The parameters may be complex (frequency-dependent) but the relationships must be linear. A transistor can be considered linear when the signal excursions within it are small compared to its bias current and voltage conditions. Under these conditions, known as "Small Signal Operation" the transistor may be thoroughly represented as a black-box when any one set of parameters, z, y, a, h, or g are obtained.

The matrix chosen to define a transistor by its manufacturers is naturally enough that involving those parameters which are easiest to measure. Usually, the "h" parameters are measured and, more often than not, with the transistor in the common-base configuration. The reader is referred to Chapter 15 of this manual for practical measurement details. The reason why it is easier to measure the "h" parameters rather than the others may be seen from their definition.




**BLACK-BOX REPRESENTING "h" PARAMETER MEASUREMENTS REFERRED TO IN TEXT**

**Figure 4.9**

$$\begin{bmatrix} e_1 \\ i_2 \end{bmatrix} = [h] \begin{bmatrix} i_1 \\ e_2 \end{bmatrix} \tag{4x}$$

expanded

$$e_1 = h_{11}\, i_1 + h_{12}\, e_2 \tag{4y}$$

$$i_2 = h_{21}\, i_1 + h_{22}\, e_2 \tag{4z}$$

From equation (4y)

$$h_{11} = \frac{e_1}{i_1} \text{ when } e_2 = 0$$

$$h_{12} = \frac{e_1}{e_2} \text{ when } i_1 = 0$$

From equation (4z)

$$h_{21} = \frac{i_2}{i_1} \text{ when } e_2 = 0$$

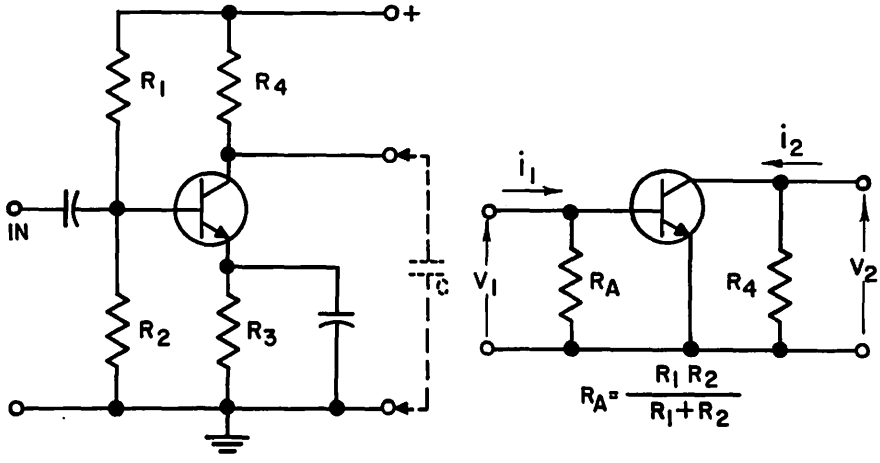
$$h_{22} = \frac{i_2}{e_2} \text{ when } i_1 = 0$$

For the transistor, $h_{11}$ is often called $h_i$, the input impedance. The condition $e_2 = 0$ is the same as saying the output terminals are short-circuited to the signal. In addition, $h_{12}$ is called $h_r$, the reverse voltage transfer ratio. The condition $i_1 = 0$ means open-

circuit input. $h_{21}$ becomes $h_f$, the forward current transfer ratio with output short-circuited to signal currents. And finally, $h_{22}$ is $h_o$, the output admittance with open-circuit input. $h_i$, $h_r$, $h_f$ and $h_o$ usually also have yet another subscript to indicate to which transistor configuration they refer. For example: $h_{ib}$ is the input impedance of a transistor with output signal short-circuited when used in the common-base configuration, and $h_{rc}$ is the reverse voltage transfer ratio with the input of a transistor open circuited when used in the common-collector configuration. It will be noticed that in defining the h parameters two conditions are stipulated:

1. Output short-circuited with respect to signal.
2. Input open-circuited with respect to signal.

The phrase *with respect to signal* is necessary in these two conditions, since in any practical circuit it is necessary to provide for bias currents as in Figure 4.10.




**(A) PRACTICAL CIRCUIT** **(B) EQUIVALENT CIRCUIT**

**Figure 4.10**

"Short-circuited output with respect to signal" would then mean placing a hefty capacitor across the output terminals in the manner shown. The transistor has a fairly low input impedance and a high output impedance, at least in the common-base and common-emitter configurations (measurements are seldom made on a transistor in the common-collector connection owing to its proneness to instability). It is therefore easy to provide a high impedance current source for the input to obtain the open-circuit input condition and a stiff voltage source for the output (i.e. short-circuit). Hence it is easiest, in practice, to measure the h parameters. The letter h, incidentally, stands for *hybrid,* a name which reflects the mixing of input and output voltages and currents in the two h parameter equations of the black-box.

Once the h parameters of a transistor are known for a particular configuration, the z, y, a, and g parameters may be obtained from the conversion table in Figure 4.8. Corresponding h parameters of the other configurations may be found by referring to the table in Figure 4.11 which gives the h parameters in terms of the "T" equivalent circuit as well.

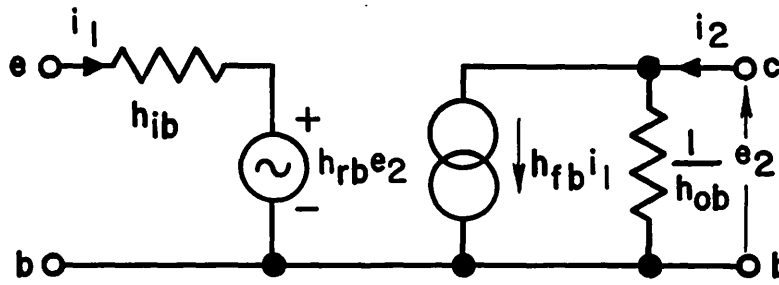
# APPROXIMATE CONVERSION FORMULAE H PARAMETERS AND T EQUIVALENT CIRCUIT

(NUMERICAL VALUES ARE TYPICAL FOR THE 2N525 AT 1MA, 5V)

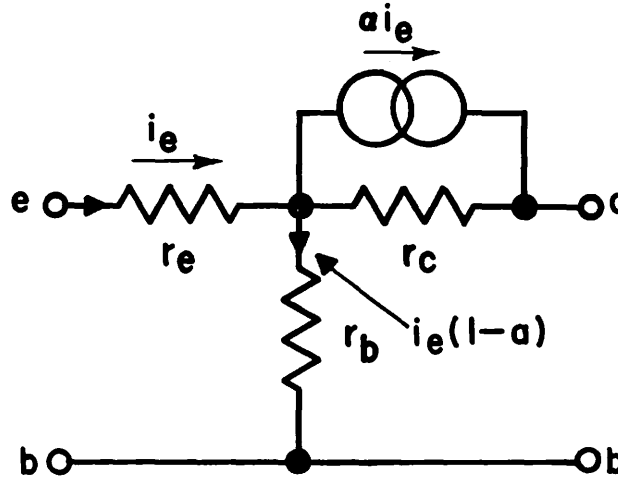
| SYMBOLS IRE | SYMBOLS OTHER | COMMON EMITTER | COMMON BASE | COMMON COLLECTOR | T EQUIVALENT CIRCUIT (APPROXIMATE) |
|---|---|---|---|---|---|
| $h_{ie}$ | $h_{11e}$, $\frac{1}{Y_{11e}}$ | 1400 OHMS | $\frac{h_{ib}}{1+h_{fb}}$ | $h_{ic}$ | $r_b+\frac{r_e}{1-\alpha}$ |
| $h_{re}$ | $h_{12e}$, $\mu_{bc}$ | $3.37 \times 10^{-4}$ | $\frac{h_{ib}h_{ob}}{1+h_{fb}}-h_{rb}$ | $1-h_{rc}$ | $\frac{r_e}{(1-\alpha)r_c}$ |
| $h_{fe}$ | $h_{21e}$, $\beta$ | 44 | $-\frac{h_{fb}}{1+h_{fb}}$ | $-(1+h_{fc})$ | $\frac{\alpha}{1-\alpha}$ |
| $h_{oe}$ | $h_{22e}$, $\frac{1}{Z_{22e}}$ | $27 \times 10^{-6}$ MHOS | $\frac{h_{ob}}{1+h_{fb}}$ | $h_{oc}$ | $\frac{1}{(1-\alpha)r_c}$ |
| $h_{ib}$ | $h_{11}$, $\frac{1}{Y_{11}}$ | $\frac{h_{ie}}{1+h_{fe}}$ | 31 OHMS | $-\frac{h_{ic}}{h_{fc}}$ | $r_e+(1-\alpha)r_b$ |
| $h_{rb}$ | $h_{12}$, $\mu_{ec}$ | $\frac{h_{ie}h_{oe}}{1+h_{fe}}-h_{re}$ | $5 \times 10^{-4}$ | $h_{rc}-1-\frac{h_{ic}h_{oc}}{h_{fc}}$ | $\frac{r_b}{r_c}$ |
| $h_{fb}$ | $h_{21}$, $\alpha$ | $-\frac{h_{fe}}{1+h_{fe}}$ | −0.978 | $-\frac{1+h_{fb}}{h_{fb}}$ | $-\alpha$ |
| $h_{ob}$ | $h_{22}$, $\frac{1}{Z_{22}}$ | $\frac{h_{oe}}{1+h_{fe}}$ | $0.60 \times 10^{-6}$ MHOS | $-\frac{h_{oc}}{h_{fc}}$ | $\frac{1}{r_c}$ |
| $h_{ic}$ | $h_{11c}$, $\frac{1}{Y_{11c}}$ | $h_{ie}$ | $\frac{h_{ib}}{1+h_{fb}}$ | 1400 OHMS | $r_b+\frac{r_e}{1-\alpha}$ |
| $h_{rc}$ | $h_{12c}$, $\mu_{be}$ | $1-h_{re}$ | 1 | 1.00 | $1-\frac{r_e}{(1-\alpha)r_c}$ |
| $h_{fc}$ | $h_{21c}$, $\alpha_{eb}$ | $-(1+h_{fe})$ | $-\frac{1}{1+h_{fb}}$ | −45 | $-\frac{1}{1-\alpha}$ |
| $h_{oc}$ | $h_{22c}$, $\frac{1}{Z_{22c}}$ | $h_{oe}$ | $\frac{h_{ob}}{1+h_{fb}}$ | $27 \times 10^{-6}$ MHOS | $\frac{1}{(1-\alpha)r_c}$ |
| $\alpha$ | | $\frac{h_{fe}}{1+h_{fe}}$ | $-h_{fb}$ | $\frac{1+h_{fc}}{h_{fc}}$ | 0.978 |
| $r_c$ | | $\frac{1+h_{fe}}{h_{oe}}$ | $\frac{1-h_{rb}}{h_{ob}}$ | $-\frac{h_{fc}}{h_{oc}}$ | 1.67 MEG |
| $r_e$ | | $\frac{h_{re}}{h_{oe}}$ | $h_{ib}-\frac{h_{rb}}{h_{ob}}(1+h_{fb})$ | $\frac{1-h_{rc}}{h_{oc}}$ | 12.5 OHMS |
| $r_b$ | | $h_{ie}-\frac{h_{re}}{h_{oe}}(1+h_{fe})$ | $\frac{h_{rb}}{h_{ob}}$ | $h_{ic}+\frac{h_{fc}}{h_{oc}}(1-h_{rc})$ | 840 OHMS |

Figure 4.11

The h parameter equivalent circuit is shown in Figure 4.12 together with the "T" equivalent circuit of the transistor.




(A) HYBRID EQUIVALENT CIRCUIT
(COMMON BASE CONFIGURATION)

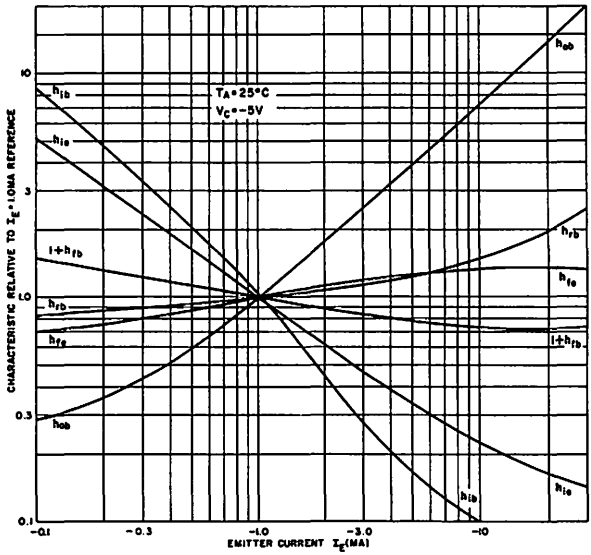



(B) "T" EQUIVALENT CIRCUIT
(COMMON BASE CONFIGURATION)

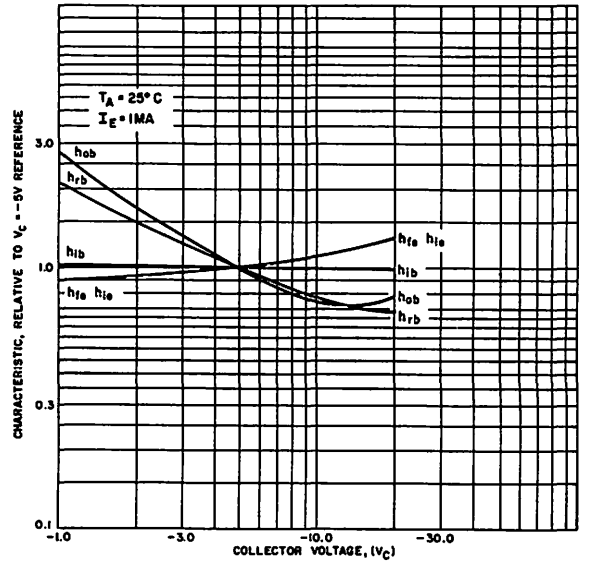
**Figure 4.12**

The "T" equivalent circuit is of interest since it approximates the actual transistor structure. Thus $r_e$ and $r_c$ represent the ohmic resistances of the emitter and collector junctions respectively while $r_b$ represents the ohmic resistance between the base contact and the junctions. The current generator $\alpha i_e$ represents the transfer of current from the emitter junction to the collector junction across the base region. The "T" finds its greatest use in circuit synthesis particularly when the designer is initially laying out his circuit. He knows, for example, that the input impedance of a common-emitter stage is approximately $r_b$ plus $\beta$ times the total impedance appearing in the emitter circuit (which includes $r_e$) — such approximations not being so easily arrived at from a knowledge of hybrid parameters. When it is necessary, however, to analyze the performance of a given circuit with a fair degree of accuracy, four-pole parameters are extremely useful, in some cases almost indispensable. As might be expected from the "small signal" restriction, h parameters vary with operating point. Specification sheets

often carry curves of the variation of the small signal parameters with bias current and voltage. Such curves are shown in Figure 4.13. These are specifically for the 2N525 and are plotted with respect to the values at an operating point defined by a collector potential of 5 volts and an emitter current of 1 ma.




CHARACTERISTICS VS EMITTER CURRENT




CHARACTERISTICS VS COLLECTOR VOLTAGE

**VARIATION OF "H" PARAMETERS WITH BIAS CONDITIONS**

**Figure 4.13**

Suppose, for example, the typical value of $h_{ob}$ is required for the 2N525 at $I_e = 0.5$ ma and $V_e = 10$ volts. From Figure 4.11 the typical value of $h_{ob}$ at 1 ma and 5 volts is $0.6 \times 10^{-6}$ mhos. From Figure 4.13 the correction factor at 0.5 ma is 0.6 and the correction factor at 10 volts is 0.75. Therefore,

$$h_{ob}\ (0.5\ \text{ma, } 10\ \text{volts}) = 0.6 \times 10^{-6} \times 0.6 \times 0.75 = 0.27 \times 10^{-6}\ \text{mhos.} \tag{4aa}$$

Once the h parameters are known for the particular bias conditions and configuration being used, the performance of the transistor in an amplifier circuit can be found for any value of source or load impedance.

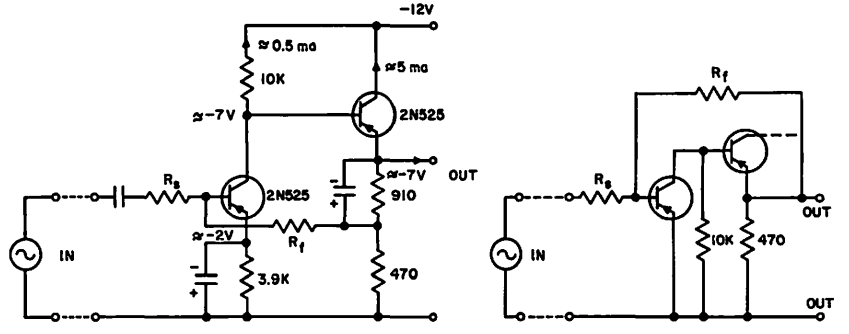
Figure 4.14 gives the equations for determining the input and output impedances, current, voltage, and power gains of any black-box, including the transistor, when any set of its four-pole parameters (z, y, a, h, or g) are known or have been calculated.

## PROPERTIES OF THE TERMINATED FOUR-TERMINAL NETWORK

| | z | y | h | g | a |
|---|---|---|---|---|---|
| $z_i$ | $\frac{\Delta^z + z_{11} z_l}{z_{22} + z_l}$ | $\frac{y_{22} + y_l}{\Delta^y + y_{11} y_l}$ | $\frac{\Delta^h + h_{11} y_l}{h_{22} + y_l}$ | $\frac{g_{22} + z_l}{\Delta^g + g_{11} z_l}$ | $\frac{a_{11} z_l + a_{12}}{a_{21} z_l + a_{22}}$ |
| $z_o$ | $\frac{\Delta^z + z_{22} z_g}{z_{11} + z_g}$ | $\frac{y_{11} + y_g}{\Delta^y + y_{22} y_g}$ | $\frac{h_{11} + z_g}{\Delta^h + h_{22} z_g}$ | $\frac{\Delta^g + g_{22} y_g}{g_{11} + y_g}$ | $\frac{a_{22} z_g + a_{12}}{a_{21} z_g + a_{11}}$ |
| $A_v$ | $\frac{z_{21} z_l}{\Delta^z + z_{11} z_l}$ | $\frac{-y_{21}}{y_{22} + y_l}$ | $\frac{-h_{21} z_l}{h_{11} + \Delta^h z_l}$ | $\frac{g_{21} z_l}{g_{22} + z_l}$ | $\frac{z_l}{a_{12} + a_{11} z_l}$ |
| $A_i$ | $\frac{z_{21}}{z_{22} + z_l}$ | $\frac{-y_{21} y_l}{\Delta^y + y_{11} y_l}$ | $\frac{-h_{21} y_l}{h_{22} + y_l}$ | $\frac{g_{21}}{\Delta^g + g_{11} z_l}$ | $\frac{1}{a_{22} + a_{21} z_l}$ |

**Figure 4.14**

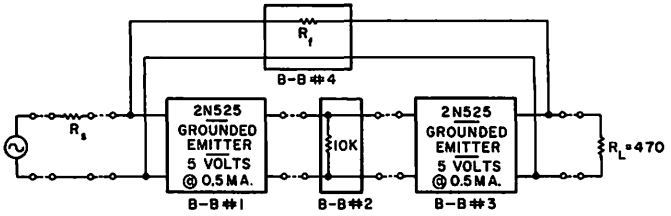
Let us work an example using four-pole parameters to analyze the circuit shown in Figure 4.15.




**(A) PRACTICAL CIRCUIT** **(B) EQUIVALENT CIRCUIT**

**Figure 4.15**

We will concern ourselves with the small signal gain and ignore the D.C. stability. The black-box equivalent at signal frequency is shown in Figure 4.16.




**BLACK-BOX EQUIVALENT AT SIGNAL FREQUENCY OF FIGURE 4.15**

**Figure 4.16**

B-B's 1, 2, and 3 are cascaded, so "a" parameters will be needed. We will first need to derive the h parameters for the 2N525 which is used here under two different operating points and two different configurations, common-emitter and common-collector. Values obtained from Figures 4.11 and 4.13 can be tabulated as follows

| Transistor Type 2N525 Operating Conditions | $h_{11}$ | $h_{12}$ | $1 + h_{21}$ | $h_{21}$ | $h_{22}$ |
|---|---|---|---|---|---|
| **Common Base** $V_c = -5v$, $I_E = 1$ ma | 31 | $5 \times 10^{-4}$ | 0.022 | −0.978 | $0.60 \times 10^{-6}$ |
| $I_E = 0.5$ ma | $31 \times 2 = 62$ | $5 \times 10^{-4} \times 0.92 = 4.6 \times 10^{-4}$ | $0.022 \times 1.2 = 0.026$ | −0.974 | $0.60 \times 10^{-6} \times 0.6 = 0.36 \times 10^{-6}$ |
| **Common Emitter** $V_c = -5v$, $I_E = 0.5$ ma | 2400 | $4.04 \times 10^{-4}$ | | 37.5 | $13.85 \times 10^{-6}$ |
| $V_c = -5v$, $I_E = 5$ ma | 4.96 | $6 \times 10^{-4}$ | 0.0176 | −0.9824 | $2.4 \times 10^{-6}$ |
| **Common Collector** $V_c = -5v$, $I_E = 5$ ma | 280 | 1 | | −56.8 | $136 \times 10^{-6}$ |

The "boxed" operating conditions are those which apply to the circuit of Figure 4.15. Using the table in Figure 4.8, the corresponding "a" parameters are

| Operating Conditions | $a_{11}$ | $a_{12}$ | $a_{21}$ | $a_{22}$ |
|---|---|---|---|---|
| **Common Emitter** $V_c = -5v$, $I_E = 0.5$ ma | $-4.8 \times 10^{-4}$ | −64 | $-3.69 \times 10^{-7}$ | $-2.67 \times 10^{-2}$ |
| **Common Collector** $V_c = -5v$, $I_E = 5$ ma | 1 | 4.91 | $2.4 \times 10^{-6}$ | $17.6 \times 10^{-3}$ |

Combining B-B's 1, 2, and 3 of Figure 4.17 and neglecting B-B 4 (the feed-back loop)

$$\begin{bmatrix} -4.8 \times 10^{-4}, & -64 \\ -3.7 \times 10^{-7}, & -2.7 \times 10^{-2} \end{bmatrix} \times \begin{bmatrix} 1, & 0 \\ 10^{-4}, & 1 \end{bmatrix} \times \begin{bmatrix} 1, & 4.9 \\ 2.4 \times 10^{-6}, & 17.6 \end{bmatrix}$$

When multiplying several matrices together, the method is to start at the right hand side and multiply the last two matrices in the manner which has been described earlier in this chapter. This gives one combined matrix representing the last two matrices. This combination is then multiplied by the next matrix to the left and so on until the whole product has been reduced to one final matrix combination.

After carrying out this procedure on the open-loop circuit, that is, no feed-back applied (see Figure 4.16), the following "a" matrix is obtained

$$\begin{bmatrix} -70 \times 10^{-4}, & -11{,}400 \times 10^{-4} \\ -31.2 \times 10^{-7}, & -4910 \times 10^{-7} \end{bmatrix}$$

As a quick check on the arithmetic so far the voltage gain will be calculated for a load of 470Ω using the table in Figure 4.14.

$$A_v = \frac{Z_l}{a_{12} + a_{11} Z_l} = \frac{470}{-11{,}400 \times 10^{-4} - 70} \times 10^{-4} \times 470$$

$$A_v = \frac{-47{,}000}{443} \approx -106$$

A negative value of voltage gain is expected since there is a total phase shift of $\pi$ radians over the whole circuit.

From knowledge of the "T" equivalent, a rough value for the gain can be determined. With a load of 470Ω, the emitter-follower stage has an input impedance of approximately

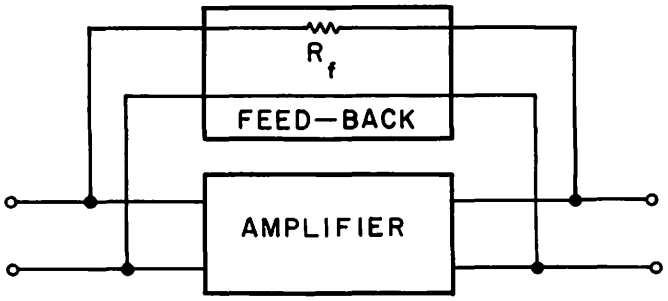
$$h_{21e} \times Z_l \approx 57 \times 470 \approx 27 \text{ K}$$

This 27K in parallel with the 10K resistor forms the load of the first stage. The voltage gain of the first stage is around

$$\frac{h_{21e} Z_l}{h_{11e}} \approx \frac{37.5 \times 7.3 \times 10^3}{2.4 \times 10^3} \approx 114$$

To obtain the over-all voltage gain this figure has to be multiplied by the voltage transfer of the emitter-follower which is very approximately $h_{21b}$. The open-loop voltage gain of the amplifier by this rough method is therefore about $114 \times 0.98 \approx 112$ which differs by only a few percent from the figure arrived at with the matrix equation, namely 106.

One might argue that this degree of accuracy was sufficient for the practical case and why bother with matrices. However, when feed-back is applied the matrix method offers a distinct advantage. Figure 4.17 shows this condition.




**FEEDBACK BLACK-BOX SHOWN IN PARALLEL WITH AMPLIFIER BLACK-BOX**

**Figure 4.17**

It is easily seen that the feed-back black-box is in parallel with the amplifier black-box. The y parameters of each are therefore needed to effect a simple combination.

Using table 4.11, the y parameters of the amplifier are obtained from the "a" parameters. The y parameters for a series impedance (i.e., the feed-back resistor) are

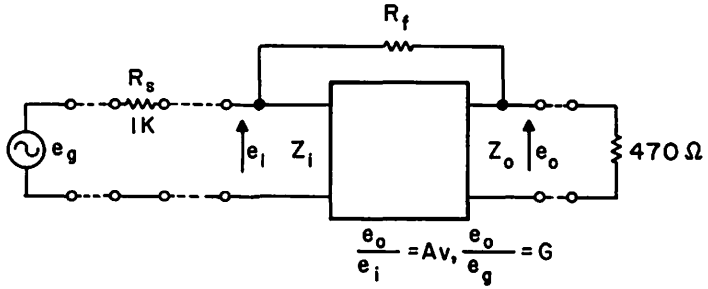
$$\begin{bmatrix} \frac{1}{Z} & -\frac{1}{Z} \\ \frac{1}{Z} & \frac{1}{Z} \end{bmatrix}$$

So, with $R_{fb}$ equal to 10 KΩ, the total y matrix equals

$$\begin{bmatrix} 10^{-4}, & -10^{-4} \\ -10^{-4}, & 10^{-4} \end{bmatrix} + \begin{bmatrix} 4.3 \times 10^{-4}, & -1.05 \times 10^{-7} \\ 0.877, & 6.14 \times 10^{-3} \end{bmatrix} =$$

$$\begin{bmatrix} 5.3 \times 10^{-4}, & -1 \times 10^{-4} \\ 0.877, & 62.4 \times 10^{-4} \end{bmatrix}$$

The voltage gain and the input and output impedances may be calculated with reference to Figure 4.14. $R_s$, the signal source impedance in Figure 4.15 will be chosen as 1K. The equivalent circuit is shown in Figure 4.18.




**EQUIVALENT CIRCUIT OF FIGURE 4.17**

**Figure 4.18**

Figure 4.19 shows the variation of $A_v$, $Z_i$, $Z_o$ for three values of $R_f$: $\infty$*, 10K, and 1K.

| $R_s$ | $R_f$ | $A_v$ | $Z_i$ | $Z_o$ |
|---|---|---|---|---|
| 1 KΩ | ∞* | 106 | 2.3 K | 160 Ω |
| 1 KΩ | 10 K | 105 | 90 Ω | 16 Ω |
| 1 KΩ | 1 K | 95 | 10.5 Ω | 2.7 Ω |

**VARIATON OF $A_v$, $Z_i$, AND $Z_o$ FOR THREE VALUES OF $R_f$**
**Figure 4.19**

*(In assigning an infinite value to $R_f$, it must be assumed that bias for the first stage of the practical amplifier is provided by an auxiliary means since this bias is ordinarily available through the feed-back loop.)

As would be expected $A_v$ is affected by $R_f$ only as far as the feed-back loop loads the output. $Z_i$ and $Z_o$ are significantly affected though, and the reduction of $Z_i$ with $R_f$ affects G, the overall gain, since

$$G = \frac{A_v}{1 + \frac{R_s}{Z_i}}$$

As mentioned previously the matrix parameters may be complex, i.e., frequency dependent, as long as linearity with respect to current and voltage is maintained. The y parameters and the h parameters are often used to analyze high frequency circuits. Figure 4.20 provides useful design equations for this purpose.

With the exception of equation (4hh) all of the equations in Figure 4.20 are valid at any frequency, provided that the values of the h parameters at that particular frequency are used. At the higher frequencies h parameters become complex and the low frequency h parameters are no longer valid. The matched power gain given by equation (4ii) requires that both the input and the output of the amplifier stage be tuned, and the input and output resistances be matched to the generator and load resistance respectively. This situation is seldom met exactly in practice, but it is generally met closely enough to permit accurate results from equation (4ii).

If the voltage feedback ratio, $h_r$, is very small or is balanced out by external feedback the circuit is said to be *unilateral*. This means that no signal transmission can take place from the output of the circuit to the input. Under these conditions the input impedance of the circuit will be equal to $h_i$ and the output impedance will be equal to $1/h_o$. The power gain under matched, unilateral conditions is given by equation (4jj). This power gain is a good figure of merit for the transistor since it is independent of circuit conditions and transistor configuration. It represents the maximum power gain that can be obtained from a transistor under conditions of absolute stability.

## REFERENCE

* Shea, Richard F. et al, "Principles of Transistor Circuits," John Wiley & Sons, Inc. (1953)

INPUT IMPEDANCE $$Z_i = \frac{e_i}{i_i} = h_i - \frac{h_f h_r Z_L}{1+h_o Z_L} \qquad (4bb)$$

MATCHED INPUT IMPEDANCE * $$Z_{im} = a_i \left[D - jC\right] + jb_i \qquad (4cc)$$

OUTPUT ADMITTANCE $$Y_o = \frac{i_o}{e_o} = h_o - \frac{h_f h_r}{h_i + Z_g} \qquad (4dd)$$

MATCHED OUTPUT ADMITTANCE * $$Y_{om} = a_o \left[D - jC\right] + jb_o \qquad (4ee)$$

CURRENT GAIN $$A_i = \frac{i_o}{i_i} = \frac{h_f}{1+h_o Z_L} \qquad (4ff)$$

VOLTAGE GAIN $$A_v = \frac{e_o}{e_i} = \frac{1}{h_r - \frac{h_i}{Z_L}\left(\frac{1+h_o Z_L}{h_f}\right)} \qquad (4gg)$$

OPERATING POWER GAIN (LOW FREQUENCY ONLY, $Z_g = R_g, Z_L = R_L$)

$$G = \frac{\text{POWER INTO LOAD}}{\text{POWER INTO TRANSISTOR}} = A_v A_i = \frac{\left(\frac{h_f}{1+h_o R_L}\right)}{h_r - \frac{h_i}{R_L}\left(\frac{1+h_o R_L}{h_f}\right)} \qquad (4hh)$$

MATCHED POWER GAIN * $$G_m = \frac{a_f^2 + b_f^2}{a_i a_o\left[(1+D)^2 + C^2\right]} \qquad (4ii)$$

MATCHED UNILATERAL POWER GAIN ($h_r = 0$) $$G_{mu} = \frac{a_f^2 + b_f^2}{4 a_i a_o} = \frac{|h_f|^2}{4 a_i a_o} \qquad (4jj)$$

$Z_g = R_g + jX_g$ = OUTPUT IMPEDANCE OF GENERATOR

$Z_L = R_L + jX_L$ = IMPEDANCE OF LOAD

* FOR MATCHED CONDITIONS

$Z_{im} = R_g - jX_g$

$Z_{om} = R_L - jX_L$

$h_i = a_i + jb_i$

$h_r = a_r + jb_r$

$h_f = a_f + jb_f$

$h_o = a_o + jb_o$

$$C = \frac{a_r b_f + a_f b_r}{2 a_i a_o}$$

$$F = \frac{a_r a_f - b_r b_f}{a_i a_o}$$

$$D = \sqrt{1 - F - C^2}$$

TRANSISTOR CIRCUIT EQUATIONS WITH H-PARAMETERS

**Figure 4.20**

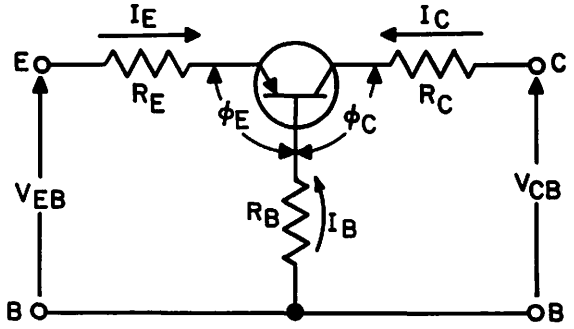
# LARGE SIGNAL CHARACTERISTICS

CHAPTER 5

The large signal or d-c characteristics of junction transistors can be described in many cases by the equations derived by Ebers and Moll.[1] These equations are useful for predicting the behavior of transistors in bias circuits, switching circuits, choppers, d-c amplifiers, etc. Some of the more useful equations are listed below for reference. They apply with a high degree of accuracy to germanium alloy junction transistors operated at low current and voltage levels, but are also useful for analyzing other types of transistors.

## PARAMETERS

The parameters used in the following large signal equations are listed below and indicated in Figure 5.1.




PARAMETERS USED IN LARGE SIGNAL EQUATIONS

**Figure 5.1**

$I_{CO}$ $I_{CBO}$ — Collector leakage current with reverse voltage applied to the collector, and the emitter open circuited ($I_{CO}$ has a positive sign for NPN transistors and a negative sign for PNP transistors).

$I_{EO}$ $I_{EBO}$ — Emitter leakage current with reverse voltage applied to the emitter, and the collector open circuited ($I_{EO}$ has a positive sign for NPN transistors and a negative sign for PNP transistors).

$\alpha_N$ — Normal alpha, the d-c common base forward current transfer ratio from emitter to collector with output short circuited ($\alpha$ has a positive sign for NPN transistors and PNP transistors). In practice, best results are obtained if the collector junction has a few tenths of a volt reverse bias. Since $\alpha$ is a function of emitter current, the value at that particular value of emitter or collector current should be used in the large signal equations.

$\alpha_I$ — Inverted alpha, same as $\alpha_N$ but with emitter and collector interchanged.

$R_B$, $R_E$, $R_C$ — Ohmic resistance internal to the transistor and in series with the base, emitter, and collector leads respectively.

| | |
|---|---|
| $I_B$, $I_E$, $I_C$ | D-C currents in the base, emitter, and collector leads respectively; positive sense of current corresponds to current flow into the terminals. |
| $\phi_C$ | Bias voltage across collector junction, i.e., collector to base voltage exclusive of ohmic drops (across $R_B$, $R_C$); forward bias is considered a positive polarity. |
| $\phi_E$ | Bias voltage across emitter junction, i.e., emitter to base voltage exclusive of ohmic drops (across $R_B$, $R_E$); forward bias is considered a positive polarity. |
| $V_{EB}$, $V_{CB}$, $V_{CE}$ | Terminal voltages: emitter to base, collector to base, and collector to emitter respectively. |
| $\Lambda = \frac{q}{mKT}$ | $1/\Lambda = 26$ millivolts at 25°C for $m = 1$. |
| q | Electronic charge $= 1.60 \times 10^{-19}$ coulomb. |
| K | Boltzmann's constant $= 1.38 \times 10^{-23}$ watt sec/°C. |
| T | Absolute temperature, degrees Kelvin = °C + 273. |
| m | A constant of value between 1 and 2 (m tends to be nearly 1 for germanium transistors and varies between 1 and 2 for silicon transistors).[2] |

$\Lambda$ can be determined from a semi-log plot of the junction forward characteristic (the semi-log scale is used for the current, while the linear scale is used for the voltage). A portion of the plot will be linear, from which $\Lambda$ can be determined

$$\Lambda = \ln\left(\frac{\Delta I}{\Delta V}\right) \tag{5a}$$

where $\Delta V$ is the corresponding change in voltage for a $\Delta I$ change in current on the linear portion of the plot. For both silicon and germanium transistors, the best correlation between theory and practice is obtained if the grounded base configuration is used, and the other junction has a slight reverse bias.

## BASIC EQUATIONS

The basic equations which govern the operation of transistors under all conditions of junction bias are

$$\alpha_N I_{EO} = \alpha_I I_{CO} \tag{5b}$$

$$I_E = -\frac{I_{EO}}{1-\alpha_N\alpha_I}\left(e^{\Lambda\phi_E}-1\right) + \frac{\alpha_I I_{CO}}{1-\alpha_N\alpha_I}\left(e^{\Lambda\phi_C}-1\right) \tag{5c}$$

$$I_C = +\frac{\alpha_N I_{EO}}{1-\alpha_N\alpha_I}\left(e^{\Lambda\phi_E}-1\right) - \frac{I_{CO}}{1-\alpha_N\alpha_I}\left(e^{\Lambda\phi_C}-1\right) \tag{5d}$$

$$I_E + I_B + I_C = 0 \tag{5e}$$

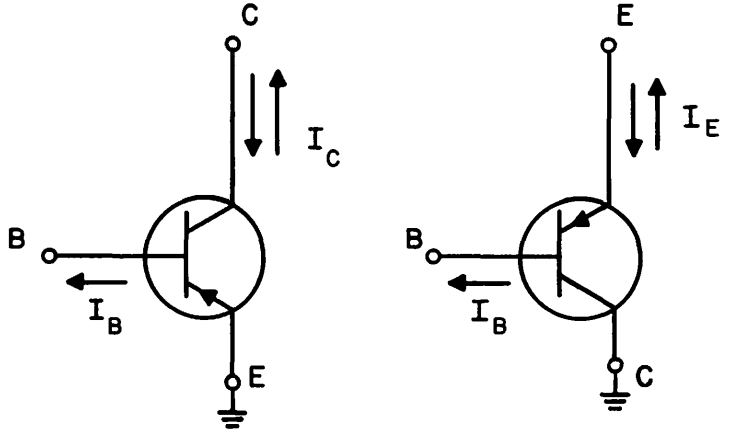
The above equations are written for the direction of current flow shown in Figure 5.1 and the sign of $I_{EO}$ and $I_{CO}$ as given above under Parameters. The three possible areas of transistor operations are: 1) one junction forward biased and one junction reverse biased (active), 2) both junctions forward biased (saturated), 3) both junctions reverse biased (cutoff).

## ACTIVE OPERATION

The transistor behaves as an active device if one junction is forward biased and the other is reverse biased. Under normal operation, the collector is reverse biased so $\phi_C$ in equations (5c) and (5d) is negative. If this bias exceeds a few tenths of a volt, $e^{\Lambda\phi_C} << 1$, and it can be eliminated from the equations. The collector current can then be solved in terms of the leakage currents, current gains, and emitter-base potential, thus giving the large signal behavior of the device.

## SATURATED OPERATION

The transistor can be operated in the normal (grounded emitter) or the inverted (grounded collector) connection as seen in Figure 5.2. The equations which are developed for each respective configuration will be labeled "normal" and "inverted." The directions of base, collector, and emitter current respectively are taken as *into* the transistor. Where a current flows *out* of the transistor, it is to be given a minus sign. When a ($\pm$) sign proceeds the equation, the plus applies to a PNP transistor while the minus applies to an NPN transistor.




(a) Normal (b) Inverted

THE NORMAL AND INVERTED CONNECTIONS

**Figure 5.2**

Under conditions of saturation and neglecting ohmic voltage drops, the voltage drop between collector and emitter is given as

$$\text{(Normal)} \qquad V_{CE} = (\pm)\frac{1}{\Lambda} \ln \frac{\alpha_I \left[1 - \frac{I_C}{I_B}\frac{(1-\alpha_N)}{\alpha_N}\right]}{\left[1 + \frac{I_C}{I_B}(1-\alpha_I)\right]} \tag{5f}$$

$$\text{(Inverted)} \qquad V_{EC} = (\pm)\frac{1}{\Lambda} \ln \frac{\alpha_N \left[1 - \frac{I_E}{I_B}\frac{(1-\alpha_I)}{\alpha_I}\right]}{\left[1 + \frac{I_E}{I_B}(1-\alpha_N)\right]} \tag{5g}$$

Notice that equation (5g) can be obtained from (5f) by replacing $I_C$ by $I_E$, $\alpha_N$ by $\alpha_I$ in the numerator, and $\alpha_I$ by $\alpha_N$ in the denominator. If the ratio of load current to base drive, $\frac{I_C}{I_B}$ or $\frac{I_E}{I_B}$, is very small, equations (5f) and (5g) respectively reduce to

$$\text{(Normal)} \qquad V_{CE} \approx (\pm)\ \frac{1}{\Lambda} \ln \alpha_I \tag{5h}$$

$$\text{(Inverted)} \qquad V_{EC} \approx (\pm)\frac{1}{\Lambda} \ln \alpha_N \tag{5i}$$

The voltage given by (5h) or (5i) is termed "offset voltage" and is an important property in transistor chopper and other low level switching applications. Since $\alpha_I < \alpha_N$ for most transistors, the offset voltage of the inverted connection will be less than that of the normal connection. The offset voltage can be made zero by forcing a current to flow from collector to emitter for a PNP transistor and from emitter to collector for an NPN transistor.

The transistor in either mode of operation will remain saturated as long as the bracketed terms in the numerator or denominator of equations (5f) and (5g) remain larger than one. Thus, the transistor behaves as a "closed switch," and the load current can flow through the transistor from collector to emitter or emitter to collector, depending upon the polarity of the load supply. If either the numerator or denominator bracketed term becomes zero, the log becomes infinite and the transistor comes out of saturation. Since $\alpha_I < \alpha_N$, it can be seen from equations (5f) and (5g), that both the normal and inverted configurations will become unsaturated respectively at lower ratios of $\frac{I_C}{I_B}$ & $\frac{I_E}{I_B}$ if the load current passes from collector to emitter in a PNP transistor and from emitter to collector in an NPN transistor.

By differentiating equation (5f) and (5g) respectively with respect to $I_C$ and $I_E$, the dynamic impedance of the saturated transistor can be found. If $\left(\frac{1-\alpha_N}{\alpha_N}\frac{I_C}{I_B}\right)$ and $\left(\frac{1-\alpha_I}{\alpha_I}\right)\frac{I_E}{I_B}$ are much less than 1, then

$$\text{(Normal)} \qquad r_{dN} \approx \frac{1}{\Lambda}\left(\frac{1-\alpha_I\,\alpha_N}{I_B\,\alpha_I}\right) \tag{5j}$$

$$\text{(Inverted)} \qquad r_{dI} \approx \frac{1}{\Lambda}\left(\frac{1-\alpha_I\,\alpha_N}{I_B\,\alpha_N}\right) \tag{5k}$$

$$\text{and} \qquad \frac{r_{dI}}{r_{dN}} = \frac{\alpha_N}{\alpha_I} \tag{5l}$$

Thus, the dynamic impedance is inversely proportional to the base current. Also, the dynamic impedance of the inverted connection is larger than that of the normal connection since $\alpha_N > \alpha_I$. (This is in contrast to the offset voltage where it is smaller for the inverted mode than for the normal connection).

The body resistances $R_E$ and $R_C$ can be found by respectively plotting $V_{CE}$ and $V_{EC}$ as a function of $I_B$. The collector and emitter are respectively open-circuited, and the voltage is measured with a high impedance millivoltmeter. At high values of base current (1 ma and up for most signal transistors), $V_{CE}$ and $V_{EC}$ become linear functions

of $I_B$. The slope of this linear portion of $V_{CE}$ gives $R_E$ while that of $V_{EC}$ gives $R_C$. This technique applies only to alloy and grown transistors. For mesa and planar transistors, the technique does not apply. The reason for this is that the collector junction overlaps the base lead forming a forward biased diode between the collector and base contact. This diode coupled with the $I_B R_B$ drop between the base contact and emitter edge prevents the transistor from going hard into saturation.[4] For these transistors, $R_E$ and $R_C$ cannot be found indirectly from external measurements. However, at lower base currents (where the internal resistance voltage drops are negligible) equations (5h) and (5i) are valid for these transistors.

## CUTOFF OPERATION

By reverse biasing both emitter and collector, equations (5b), (c), and (d) can be solved for the emitter and collector currents

$$\text{(Normal)} \qquad I_C = \frac{I_{CO}(1 - \alpha_I)}{1 - \alpha_N \alpha_I} \tag{5m}$$

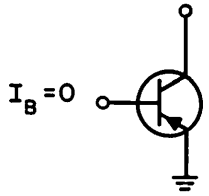
$$\text{(Inverted)} \qquad I_E = \frac{I_{EO}(1 - \alpha_N)}{1 - \alpha_N \alpha_I} \tag{5n}$$

Equations (5m) and (n) indicate that with both junctions reverse biased, the collector current will be less than $I_{CO}$, and the emitter current will be less than $I_{EO}$. Thus, for switching circuits where low leakage currents are desired, the advantage of using the inverted connection can readily be seen.

## USEFUL LARGE SIGNAL RELATIONSHIPS

### COLLECTOR LEAKAGE CURRENT ($I_{CEO}$)

For the direction of current flow shown

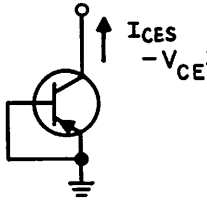



$$I_{CEO} = \frac{I_{CO}}{1 - \alpha_N} \tag{5o}$$

$I_{CEO}$ is the collector leakage current with the base open-circuited and is generally much larger than $I_{CO}$.

### COLLECTOR LEAKAGE CURRENT ($I_{CES}$)

For the direction of current flow shown

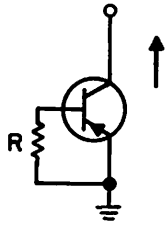



$$I_{CES} = \frac{I_{CO}}{1 - \alpha_N \alpha_I} \tag{5p}$$

$I_{CES}$ is the collector leakage current with the base shorted to the emitter and equals the leakage current the collector diode would have if the emitter junction was not present. Accurate values of $\alpha_N$ and $\alpha_I$ for use in the equations in this section are best obtained by measurement of $I_{CO}$, $I_{CEO}$ and $I_{CES}$ and calculation of $\alpha_N$ and $\alpha_I$ from equations (5o) and (5p). The value of $I_{EO}$ may be calculated from equation (5b).

## COLLECTOR LEAKAGE CURRENT ($I_{CER}$)

For direction of current flow shown

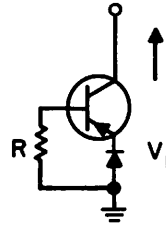



$$I_{CER} = \frac{(1 + A I_{EO} R)\, I_{CO}}{1 - \alpha_N \alpha_I + A R I_{EO}\,(1-\alpha_N)} \qquad (5q)$$

$I_{CER}$ is the collector leakage current measured with the emitter grounded and a resistor R between base and ground. The size of the resistor is generally about 10 K. From equation (5q), it is seen that as R becomes very large, $I_{CER}$ approaches $I_{CEO}$—equation (5o). Similarly, as R approaches zero, $I_{CER}$ approaches $I_{CES}$—equation (5p).

## COLLECTOR LEAKAGE CURRENT—SILICON DIODE IN SERIES WITH EMITTER

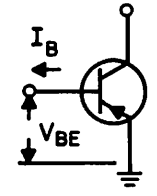
For direction of current flow shown




$$I_C = \frac{(1 + A I_{EO} R - \alpha_I A V_D)\, I_{CO}}{1 - \alpha_N \alpha_I + A R I_{EO}\,(1-\alpha_N)} \qquad (5r)$$

This circuit is useful in some switching applications where a low collector leakage current is required and a positive supply voltage is not available for reverse biasing the base of the transistor. The diode voltage $V_D$ used in the equation is measured at a forward current equal to the $I_{CO}$ of the transistor. This equation holds for values of $I_C$ larger than $I_{CO}$.

## BASE INPUT CHARACTERISTICS




for $I_C = 0$

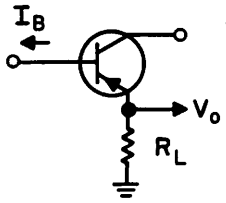
$$V_{BE} = I_B (R_E + R_B) + \frac{1}{A} \ln\left(\frac{I_B}{I_{EO}} + 1\right) \qquad (5s)$$

for $V_{CE} > -.1$ volt

$$V_{BE} = I_B \left(R_B + \frac{R_E}{1 - \alpha_N}\right) + \frac{1}{A} \ln\left[\frac{I_B\,(1-\alpha_N\alpha_I)}{I_{EO}\,(1-\alpha_N)} + 1 + \frac{\alpha_N\,(1-\alpha_I)}{\alpha_I(1-\alpha_N)}\right] \qquad (5t)$$

A comparison of equations (5s) and (5t) indicates that they are approximately equal if $R_B$ is small and $\alpha_N$ is smaller than $\alpha_I$. For this condition, the base input characteristic will be the same whether the collector is reverse biased or open-circuited.

## VOLTAGE COMPARATOR CIRCUIT




for $V_o = V_{cc}$

$$I_B = \frac{V_{cc}}{R_L}\left[1 + \left(\frac{\alpha_N}{\alpha_I}\right)\left(\frac{1-\alpha_I}{1-\alpha_N}\right)\right] \qquad (5u)$$

If an emitter follower is overdriven such that the base current exceeds the emitter current, the emitter voltage can be made exactly equal to the collector voltage. For example, if a square wave with an amplitude greater than $V_{cc}$ is applied to the base of the transistor, the output voltage $V_o$ will be a square wave exactly equal to $V_{cc}$. Equation (5u) gives the base current required for this condition and indicates that the transistor should be used in the inverted connection if the required base current is to be minimized. This circuit is useful in voltage comparators and similar circuits where a precise setting of voltage is necessary.

## REFERENCES


(1) Ebers, J.J., Moll, J.I., "Large – Signal Behavior of Junction Transistors," *Proc. I.R.E.*, Vol. 42, December, 1954.

(2) Pritchard, R.C., "Advances in the Understanding of the P-N Junction Triode," *Proc. I.R.E.*, Vol. 46, June, 1958.

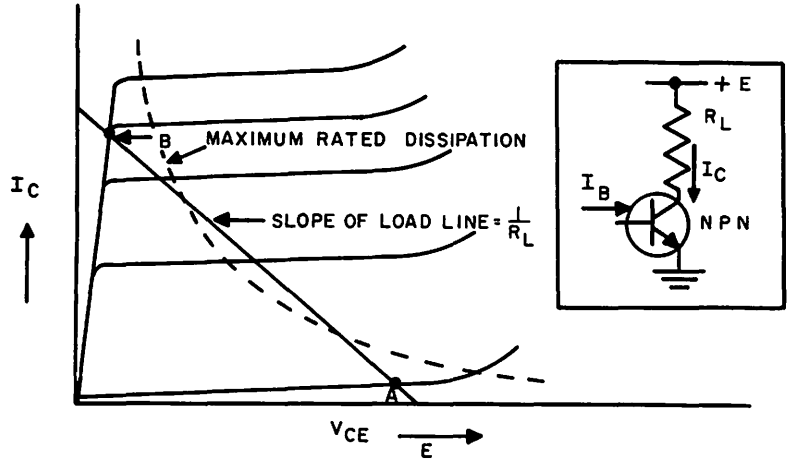
(3) Henkels, H.W., "Germanium and Silicon Rectifiers," *Proc. I.R.E.*, Vol. 46, June, 1958.

(4) Rundenberg, H.G., "On the Effect of Base Resistance and Collector-to-Base Overlap on the Saturation Voltages of Power Transistors," *Proc. I.R.E.*, Vol. 46, pp. 1304-1305, June, 1958.

# SWITCHING CHARACTERISTICS

CHAPTER 6

An ideal switch is characterized by an infinite resistance when it is open, zero resistance when it is closed, and an input by which it can be opened or closed. Transistors can be used as switches. The advantages which transistor switches offer over mechanical switches are that there are no moving or wearing parts, they are easily activated from various electrical inputs, and associated problems such as contact bounce and arcing are essentially eliminated. The common emitter configuration is most often used for transistor switching. The collector and emitter correspond to switch contacts; base to emitter current performs the input function. Common emitter transistor collector characteristics are shown in Figure 6.1 which illustrates a transistor in a switching application. Near the operating point A, the transistor switch is in the open or high resistance state. When $I_B = 0$, $I_C = I_{CO}$ divided by $1-\alpha$. Since $1-\alpha$ is a small number $I_C$ may be several times greater than $I_{CO}$. A higher resistance may be achieved by shorting the base to the emitter. Once the emitter junction is reverse biased by more than .2 volts $I_C$ approaches $I_{CO}$. This achieves the highest resistance from collector to emitter.

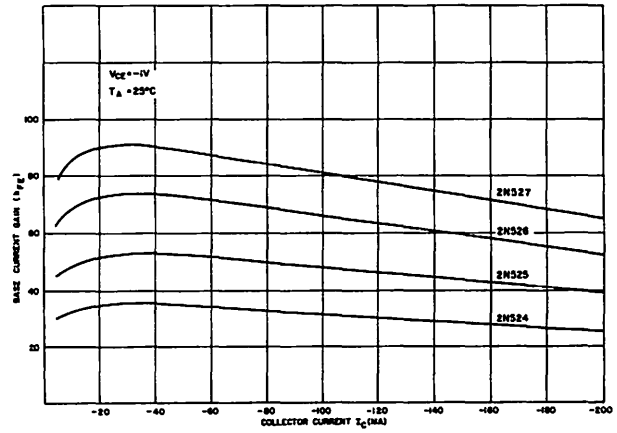



**COLLECTOR CHARACTERISTICS**
**Figure 6.1**

Operating point B corresponds to a closed switch. Ideally the voltage from collector to emitter would be zero. In practice, however, there is always an appreciable voltage across the transistor. The best switches are germanium alloy transistors such as the 2N525 which has about 1 ohm resistance when switched on. Germanium mesa transistors such as the 2N781 have a saturation resistance of 5 ohms or less. Silicon planar epitaxial units such as the 2N2193A have about 1.2 ohms saturation resistance and approach the performance of germanium alloy types. These values, however, are

dependent upon collector and base current levels and are normally specified as a saturation voltage, $V_{CE(SAT)}$, for given current levels. In order that a low resistance be achieved, it is necessary that point B lie below the knee of the characteristic curves. The region below the knee is referred to as the saturation region. Enough base current must be supplied to ensure that this point is reached. It is also important that both the *on* and *off* operating points lie in the region below the maximum rated dissipation to avoid transistor destruction. It is permissible, however, to pass through the high dissipation region very rapidly since peak dissipations of about one watt can be tolerated for a few microseconds with a transistor rated at 150 mw. In calculating the $I_B$ necessary to reach point B, it is necessary to know how $h_{FE}$ varies with $I_C$. Curves such as Figure 6.2 are provided for switching transistors. Knowing $h_{FE}$ from the curve gives $I_{B\,min}$ since $I_{B\,min} = \frac{I_C}{h_{FE}}$. Generally $I_B$ is made two or three times greater than $I_{B\,min}$ to allow for variations in $h_{FE}$ with temperature or aging and, as will be pointed out later, to improve some of the transient characteristics. The maximum rated collector voltage should never be exceeded since destructive heating may occur once a transistor breaks down. Inductive loads can generate injurious voltage transients. These can be avoided by connecting a diode across the inductance to absorb the transient as shown in Figure 6.3.

Even with the diode connected, large peak power transients can occur unless the transistor is switched off rapidly. If the transistor is switched off slowly, as soon as the collector comes out of saturation the collector voltage will rise to the supply voltage as the inductor attempts to maintain a constant current. At this instant, transistor dissipation is the product of supply voltage and maximum load current. Specific circuit components determine whether this dissipation is excessive.

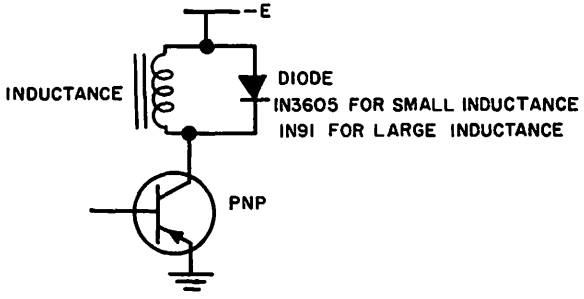



**D.C. BASE CURRENT GAIN ($h_{FE}$) VS. COLLECTOR CURRENT**

**Figure 6.2**

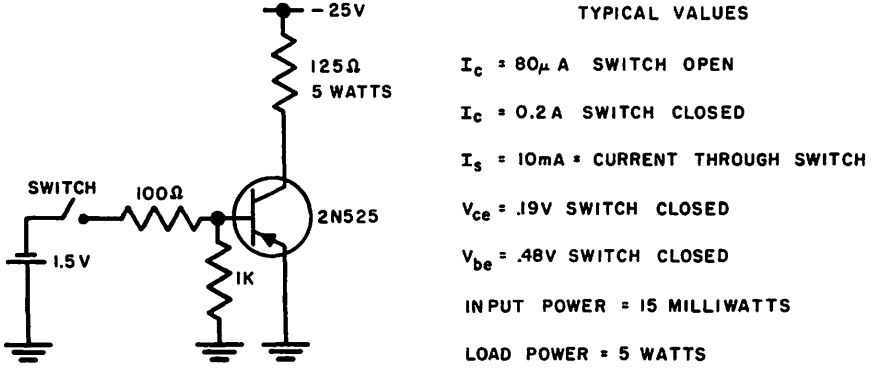
Lighted incandescent lamps have about 10 times their off resistance, consequently, $I_B$ must be increased appreciably to avoid overheating the switching transistor when lighting a lamp.

A typical switching circuit is shown in Figure 6.4. The requirement is to switch a 200 ma current in a 25 volt circuit, delivering 5 watts to the load resistor. The mechanical switch contacts are to carry a low current and be operated at a low voltage to minimize arcing. The circuit shown uses a 2N525. The 1K resistor from the base to ground reduces the leakage current when the switch is open. Typical values are indicated in Figure 6.4.




**DIODE USED TO PROTECT TRANSISTOR FROM INDUCTIVE VOLTAGE TRANSIENTS**

**Figure 6.3**




**TYPICAL TRANSISTOR SWITCH APPLICATION**

**Figure 6.4**

## STEADY STATE CHARACTERISTICS

Four items – leakage current, current gain, dissipation, and saturation – which have already been briefly mentioned, must be considered in determining the steady state characteristics of switching transistors. At high junction temperatures, $I_{co}$ can become a problem. In the off condition, both the emitter and collector junctions are generally reverse-biased. As a rule, the bias source has an appreciable resistance permitting a voltage to be developed across the resistance by $I_{co}$. The voltage can reduce the reverse bias to a point where the base becomes forward biased and conduction

occurs. Conduction can be avoided by reducing the bias source resistance, by increasing the reverse bias voltage, or by reducing $I_{CO}$ through a heat sink or a lower dissipation circuit design.

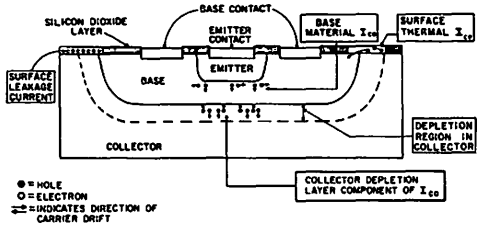
The $I_{CO}$ of a transistor is generated in four ways. One component originates in the semiconductor material in the base region of the transistor. At any temperature, there are a number of interatomic energy bonds which will spontaneously break into hole-electron pairs. If a voltage is applied, holes and electrons drift in opposite directions and can be seen as the $I_{CO}$ current. If no voltage is present, the holes and electrons eventually recombine. The number of bonds that will break can be predicted theoretically to double about every 10°C in germanium transistors and every 6°C in silicon. Theory also indicates that the number of bonds broken will not depend on voltage over a considerable voltage range. At low voltages, $I_{CO}$ appears to decrease because the drift field is too small to extract all hole-electron pairs before they recombine. At very high voltages, breakdown occurs.

A second component of $I_{CO}$ is generated at the surface of the transistor by surface energy states. The energy levels established at the center of a semiconductor junction cannot end abruptly at the surface. The laws of physics demand that the energy levels adjust to compensate for the presence of the surface. By storing charges on the surface, compensation is accomplished. These charges can generate an $I_{CO}$ component; in fact, in the processes designed to give the most stable $I_{CO}$, the surface energy levels contribute much $I_{CO}$ current. This current behaves much like the base region component with respect to voltage and temperature changes. It is described as the surface thermal component in Figure 6.5.

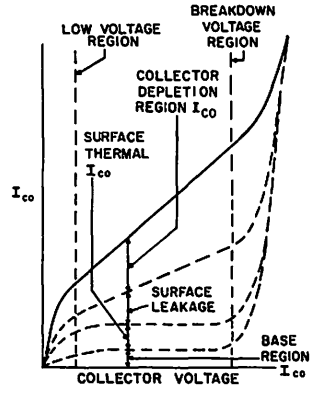
A third component of $I_{CO}$ is generated at the surface of the transistor by leakage across the junction. This component can be the result of impurities, moisture, or surface imperfections. It behaves like a resistor in that it is relatively independent of temperature but varies markedly with voltage.

The fourth component of $I_{CO}$ is generated in the collector depletion region. This component is the result of hole-electron pair formation similar to that described as the first $I_{CO}$ component. As the voltage across the collector junction is increased, the depletion region will extend into the base and collector regions. The hole-electron pairs generated in the base portion of the depletion region are accounted for by the first $I_{CO}$ component discussed, but those generated in the collector portion of the depletion region are not included. The number of pairs generated in the collector portion of the depletion region and, thus, the $I_{CO}$ from this region depend on the volume of the depletion region in the collector. Inasmuch as this volume is a function of collector and base resistivity, of junction area, and of junction voltage, the fourth component of $I_{CO}$ is voltage dependent. In an alloy transistor, this component of $I_{CO}$ is negligible since the collector depletion layer extends only slightly into the collector region due to the high base resistivity and low collector resistivity. In a mesa or planar structure where the collector region is not too heavily doped the depletion region extends into the collector, and this fourth $I_{CO}$ component may be appreciable. Since the mechanism of $I_{CO}$ generation here is hole-electron pair formation, this component will be temperature sensitive as well as voltage dependent.

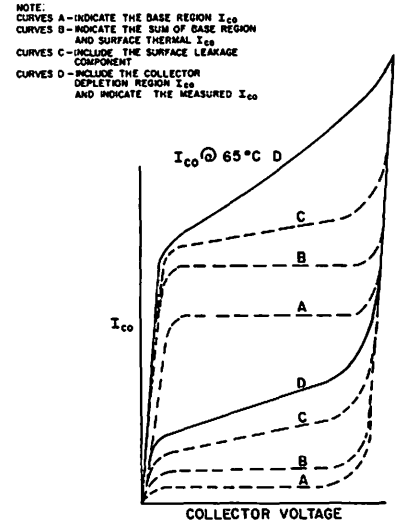
Figure 6.5(A) shows the regions which contribute to the four components. Figure 6.5(B) illustrates how the components vary with voltage. It is seen that while there is no way to measure the base region and surface energy state components separately, a low voltage $I_{CO}$ consists almost entirely of these two components. Thus, the surface leakage contribution to a high voltage $I_{CO}$ can be readily determined by subtracting out the low voltage value of $I_{CO}$, if the collector depletion layer contribution is small.




**CROSS SECTION OF NPN PLANAR PASSIVATED TRANSISTOR SHOWING REGIONS GENERATING $I_{CO}$**
**(A)**




**VARIATION OF $I_{CO}$ COMPONENTS WITH COLLECTOR VOLTAGE**
**(B)**




**VARIATION OF $I_{CO}$ COMPONENTS WITH TEMPERATURE**
**(C)**

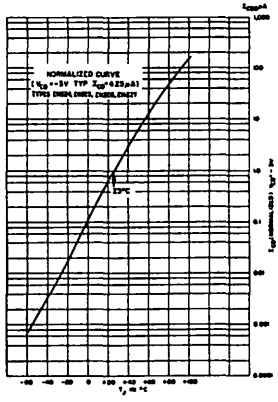
**Figure 6.5**

Figure 6.5(C) shows the variation of $I_{CO}$ with temperature. Note that while the surface thermal component, collector depletion region component and base component of $I_{CO}$ have increased markedly, the surface leakage component is unchanged. For this reason, as temperature is changed the high voltage $I_{CO}$ will change by a smaller percentage than the low voltage $I_{CO}$.

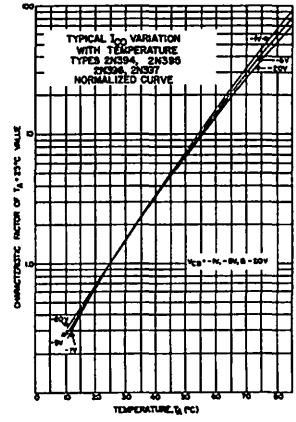
Figure 6.6 shows the variation of $I_{CO}$ with temperature and voltage for a number of transistor types. Note that the curves for the 2N396 agree with the principles above and show a leakage current less than one microampere.

The variation of current gain at high temperatures is also significant. Since $h_{FE}$ is defined as $I_C/I_B$, $h_{FE}$ depends on $I_{CO}$ since $I_C \approx h_{fe}(I_B + I_{CO})$. If $I_B = 0$ i.e., if the base

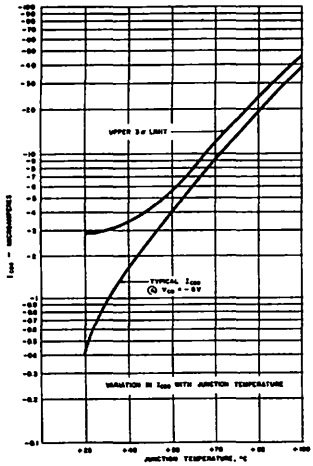
is open circuited, a collector current still flows, $I_C = h_{fe} I_{CO}$. Thus, $h_{FE}$ is infinite when $I_B = 0$. As base current is applied, the ratio $I_C/I_B$ becomes more meaningful. If $h_{FE}$ is measured for a sufficiently low $I_C$, then at a high temperature $h_{fe}I_{CO}$ will become equal to $I_C$. At this temperature $h_{FE}$ becomes infinite since no $I_B$ is required to maintain $I_C$. The AC current gain $h_{fe}$, however, is relatively independent of $I_{CO}$ and generally increases about 2:1 from −55°C to +85°C. Figure 6.7 illustrates this fact.



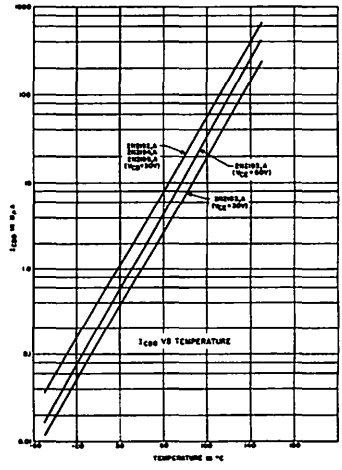
**COLLECTOR CUTOFF CURRENT VS. TEMPERATURE NORMALIZED TO 25°C (INTERMEDIATE GRIDS ARE AT 2, 4, 6, 8)**
**(A)**




**TYPICAL $I_{CO}$ VARIATION WITH TEMPERATURE**
**(B)**




**$I_{CBO}$ VS. JUNCTION TEMPERATURE FOR 2N994**
**(C)**



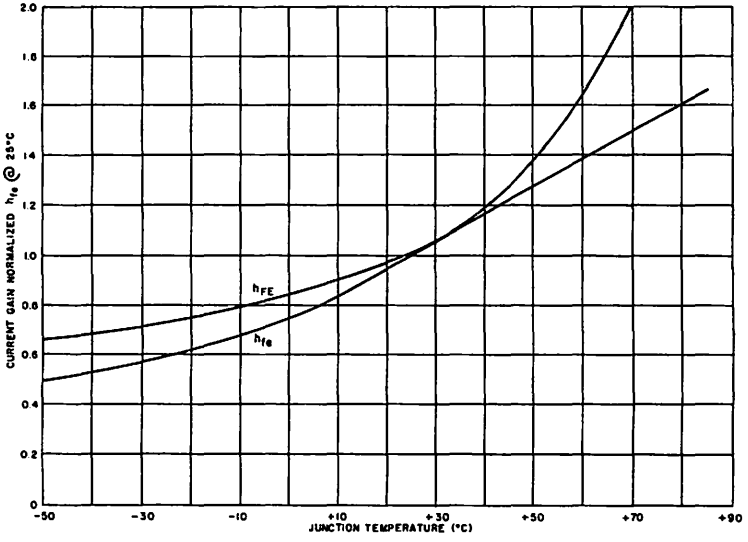

**$I_{CBO}$ VS. TEMPERATURE FOR 2N2192A, 2N2194A, AND 2N2195A**
**(D)**

**Figure 6.6**

The different electrical properties of the base, emitter, and collector regions tend to disappear at high temperatures with the result that transistor action ceases. This temperature usually exceeds 85°C and 150°C in germanium and silicon transistors, respectively.

When a transistor is used at high junction temperatures, it is possible for regenerative heating to occur which will result in thermal run-away and possible destruction of the transistor. For the maximum overall reliability, circuits should be designed to preclude the possibility of thermal run-away under the worst operating conditions. The subject of thermal run-away is discussed in detail in Chapter 7.

A major problem encountered in the operation of transistors at low temperatures is the reduction in both the a-c and d-c current gain. Figure 6.7 shows the variation of $h_{FE}$ with temperature for the 2N525 and indicates that at −50°C the value of $h_{FE}$ drops to about 65% of its value at 25°C. Most germanium and silicon transistors show approximately this variation of $h_{FE}$ and $h_{fe}$ with temperature. In the design of switching circuits the decrease of $h_{FE}$ and the increase of $V_{BE}$ at the lower temperatures must be taken into account to guarantee reliable circuit operation.




**CURRENT GAIN VS. TEMPERATURE NORMALIZED TO 25°C**

**Figure 6.7**

As with most electrical components, the transistor's range of operating conditions is limited by its power dissipation capabilities.

Because the transistor is capable of a very low $V_{CE}$ when it is in saturation it is possible to use load lines which exceed the maximum rated dissipation during the switching transient, but do not exceed it in the steady state. Such load lines can be used safely if the junction temperature does not rise to the runaway temperature during the switching transient. If the transient is faster than the thermal time constant of the junction, the transistor case may be considered to be an infinite heatsink. The junction temperature rise can then be calculated on the basis of the infinite heatsink

derating factor. Since the thermal mass of the junctions is not considered, the calculation is conservative.

In some applications there may be a transient over-voltage applied to transistors when power is turned on or when circuit failure occurs. If the transistor is manufactured to high reliability standards, the maximum voltages may be exceeded provided the dissipation is kept within specifications. While quality alloy transistors and grown junction transistors can tolerate operation in the breakdown region, low quality alloy transistors with irregular junctions should not be used above the maximum voltage ratings. Many mesa and planar transistors exhibit negative resistance after breakdown. Precautions should be taken to avoid this region or limit dissipation.

Quality transistors can withstand much abuse. 2N396 transistors in an avalanche mode oscillator have been operated at peak currents of one ampere. 2N914 transistors in the avalanche mode have generated an 8 ampere pulse with no apparent degradation. Standard production units however should be operated within ratings to ensure consistent circuit performance and long life.

It is generally desirable to heatsink a transistor to lower its junction temperature since life expectancy as well as performance decreases at high temperatures. Heat sinks also minimize thermal fatigue problems, if any exist.

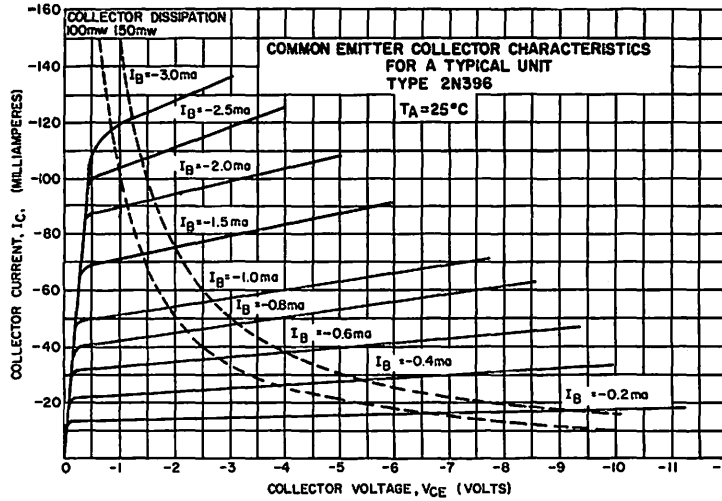



**Figure 6.8(A)**

A transistor is said to be in saturation when both junctions are forward biased. Looking at the common emitter collector characteristics shown in Figure 6.8(A) the saturation region is approximately the region below the knee of the curves, since $h_{FE}$ usually falls rapidly when the collector is forward biased. Since all the characteristic curves tend to become superimposed in the saturation region, the slope of the curves is called the *saturation resistance*. If the transistor is unsymmetrical electrically – and most transistors are unsymmetrical – then the characteristics will not be directed towards the zero coordinates but will be displaced a few millivolts from zero. For ease of measurement, generally the characteristics are assumed to converge on zero so that the saturation resistance is $r_{CE\,(SAT)} = \dfrac{I_C}{V_{CE\,(SAT)}}$.

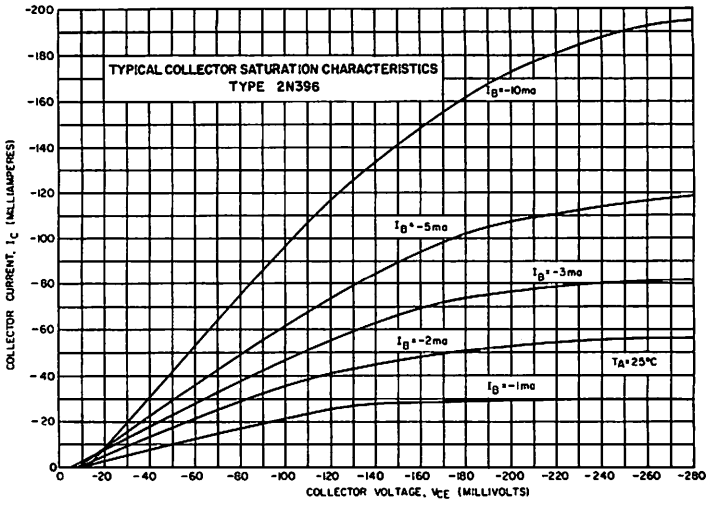



**Figure 6.8(B)**

While the characteristic curves appear superimposed, an expanded scale shows that $V_{CE\,(SAT)}$ depends on $I_B$ for any given $I_C$. The greater $I_B$ is made, the lower $V_{CE\,(SAT)}$ becomes until $I_B$ is so large that it develops an appreciable voltage across the ohmic emitter resistance and in this way increases $V_{CE\,(SAT)}$. In most cases the saturation voltage, $V_{CE\,(SAT)}$, is specified rather than the saturation resistance. Figure 6.8(B) showing the collector characteristics in the saturation region, illustrates the small voltage off-set due to asymmetry and the dependence of $r_{CE\,(SAT)}$ on $I_B$. Note also that $r_{CE\,(SAT)}$ is a low resistance to both AC and DC.

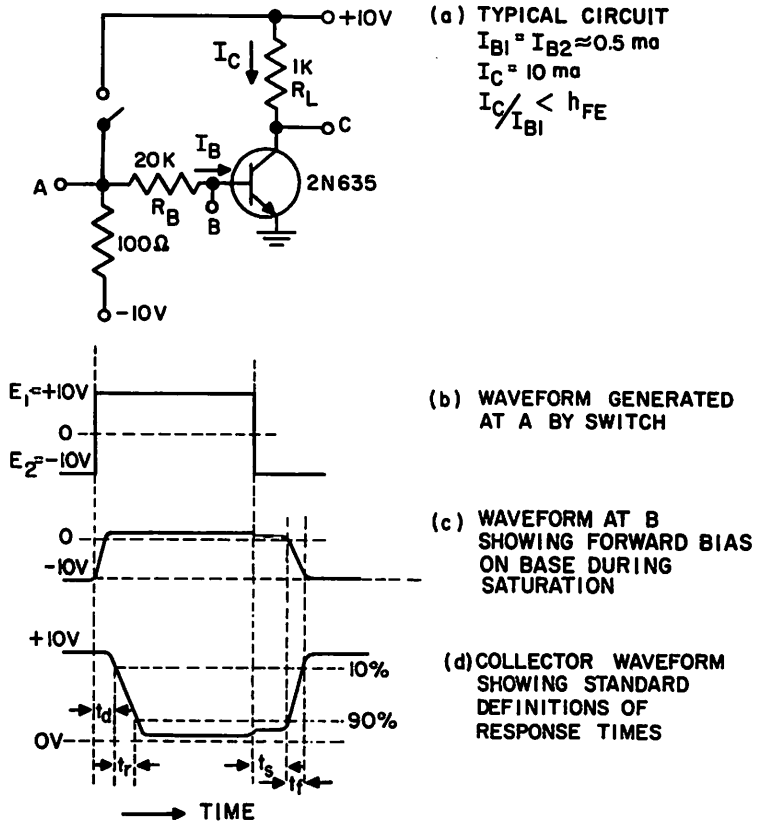
In accordance with theory the collector saturation voltage, $V_{CE\,(SAT)}$, decreases linearly with temperature for most transistors. In the case of alloy transistors, this is a result of the increase of $I_{CO}$ with temperature which increases the effective base charge at high temperatures. However, transistors which have an appreciable ohmic resistance in series with the collector or silicon transistors which have a low $I_{CO}$, generally exhibit a positive temperature coefficient for $V_{CE\,(SAT)}$.

The base to emitter voltage, $V_{BE}$, has a negative temperature coefficient which is about 2.0 millivolts per degree Centrigrade for both silicon and germanium transistors. Figure 7.1 shows the emitter to base characteristics of the 2N525 at several different temperatures. The series base resistance and emitter resistance ($r_b'$, $r_e'$) have a positive temperature coefficient so that the IR drops across these resistances can offset the normal variation of $V_{BE}$ at high values of base current.

The increase in $V_{CE\,(SAT)}$ and the decrease in $V_{BE}$ at high temperatures can lead to instability in DCTL circuits such as shown in Figure 6.21 and result in operation closer to saturation in circuits such as those shown in Figure 6.23.

## TRANSIENT RESPONSE CHARACTERISTICS

The speed with which a transistor switch responds to an input signal depends on the load impedance, the gain expected from the transistor, the operating conditions just prior to application of the input signal, as well as on the transistor's inherent characteristics.




**TRANSIENT RESPONSE**

**Figure 6.9**

Consider the simple circuit of Figure 6.9(A). Closing and opening the switch to generate a pulse as shown in Figure 6.9(B), gives the other waveforms shown. When the switch closes, current flows through the 20K resistor to turn on the transistor. However there is a delay before collector current can begin to flow since the 20K must discharge the emitter capacitance which was charged to —10 volts prior to closing the switch. Also, the collector capacitance which was charged to —20 volts prior to closing the switch must be discharged to —10 volts.

Time must also be allowed for the emitter current to diffuse across the base region. A third factor adding to the delay time is the fact that at low emitter current densities current gain and frequency response decrease. The total delay from all causes is called the "delay time" and is measured conventionally from the beginning of the input pulse to the 10% point on the collector waveform as shown in Figure 6.9(D). Delay time can be decreased by reducing the off bias voltage, and by reducing the base drive resistor in order to reduce the charging time constant. At high emitter current densities, delay time becomes negligible. Figure 6.10 shows typical delay times for the 2N396 transistor.

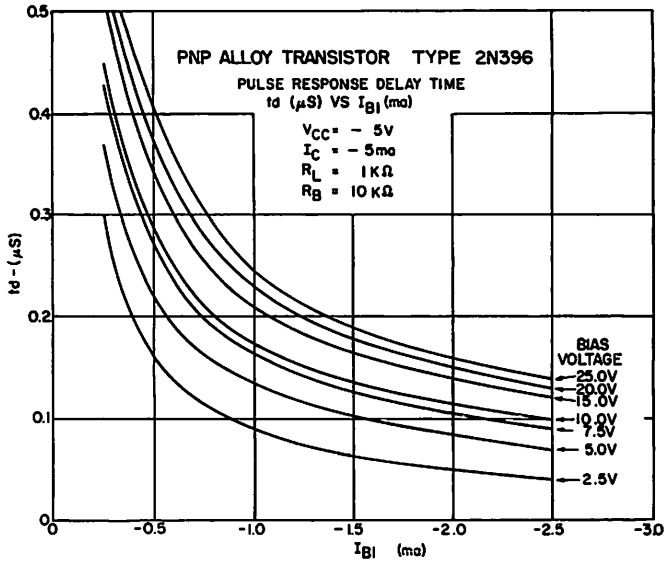



**Figure 6.10**

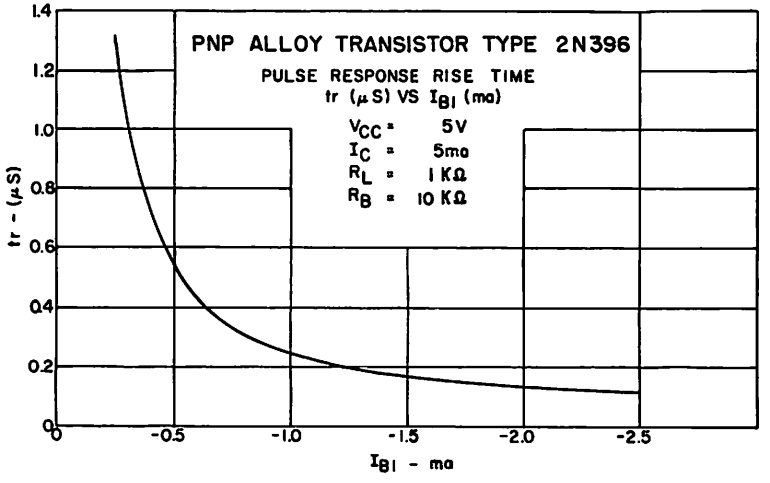
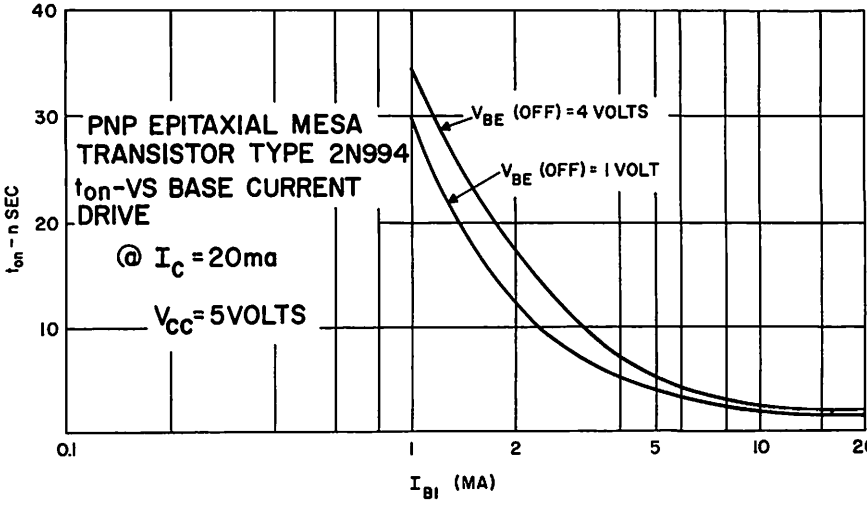



**Figure 6.11(A)**

The "rise time" refers to the turn-on of collector current. By basing the definition of rise time on current rather than voltage it becomes the same for NPN and PNP transistors. The collector voltage change may be of either polarity depending on the transistor type. However, since the voltage across the collector load resistor is a measure of collector current, it is customary to discuss the response time in terms of the collector voltage. If all other circuit parameters are kept constant, the rise time will decrease as the drive current is increased as shown in Figure 6.11(A). Turn-on time (delay time plus rise time) is shown for the 2N994, a germanium epitaxial mesa in Figure 6.11(B).

Storage time is the delay a transistor exhibits before its collector current starts to turn off. In Figure 6.9, $R_B$ and $R_L$ are chosen so that $R_L$ rather than $h_{FE}$ will limit the collector current. The front edge of the collector waveform, Figure 6.9(D), shows the delay time, $t_d$, followed by the nearly linear rise time, $t_r$. When the collector voltage falls below the base voltage, the base to collector diode becomes forward biased with the result that the collector begins emitting. By definition, the transistor is said to be *in saturation* when this occurs. This condition results in a stored charge of carriers in the base region and in some cases in the collector region.

Since the flow of current is controlled by the carrier distribution in the base, it is impossible to decrease the collector current until the stored carriers are removed. When the switch is open in Figure 6.9, the voltage at A drops immediately to −10 volts. The base voltage at B however cannot go negative since the transistor is kept *on* by the stored carriers. The resulting voltage across $R_B$ causes the carriers to flow out of the base to produce a current $I_{B2}$. As soon as the stored carriers are swept out, the transistor starts to turn off with the base voltage dropping to −10 volts and the base current decreasing to zero. The higher $I_{B1}$ is, the greater the stored charge; the higher $I_{B2}$ is, the faster charge is swept out. Figure 6.12 shows the dependence of storage time on $I_{B1}$ and $I_{B2}$ for the 2N396 transistor.




**$t_{ON}$ VS. BASE CURRENT DRIVE FOR 2N994**

**Figure 6.11(B)**

The "fall time," $t_f$, of a transistor is analogous to the rise time in that the transistor traverses the active region during this time. As normally defined, fall time is the time for the transistor to switch from 90% ON to 10% ON as shown in Figure 6.9(D). Figure 6.13(A) shows typical fall time measurements for a 2N396. Turn off time (storage plus fall time) for the 2N994 is shown in Figure 6.13(B).

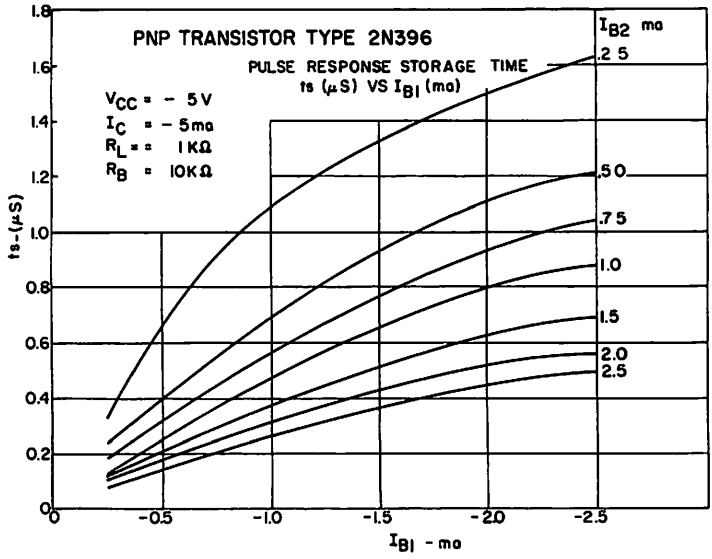



**Figure 6.12**

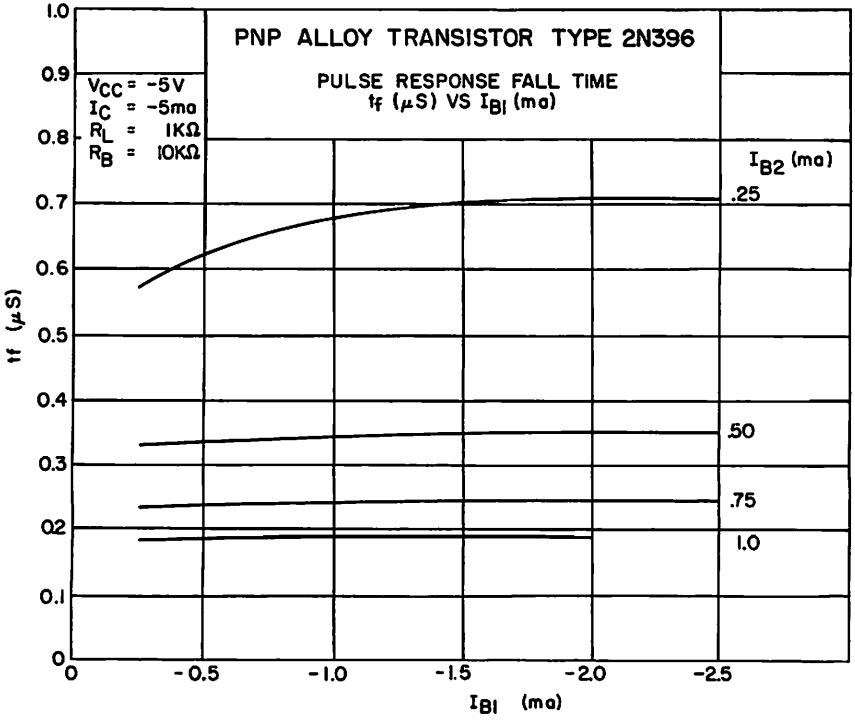



**Figure 6.13(A)**

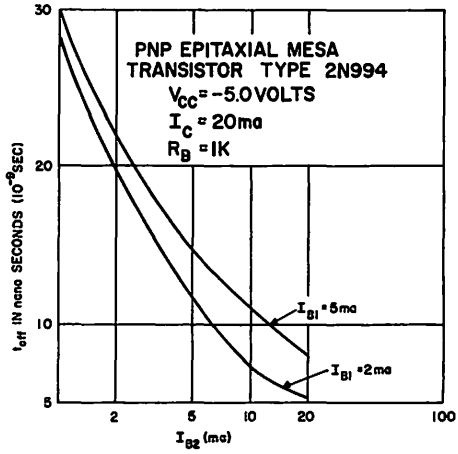
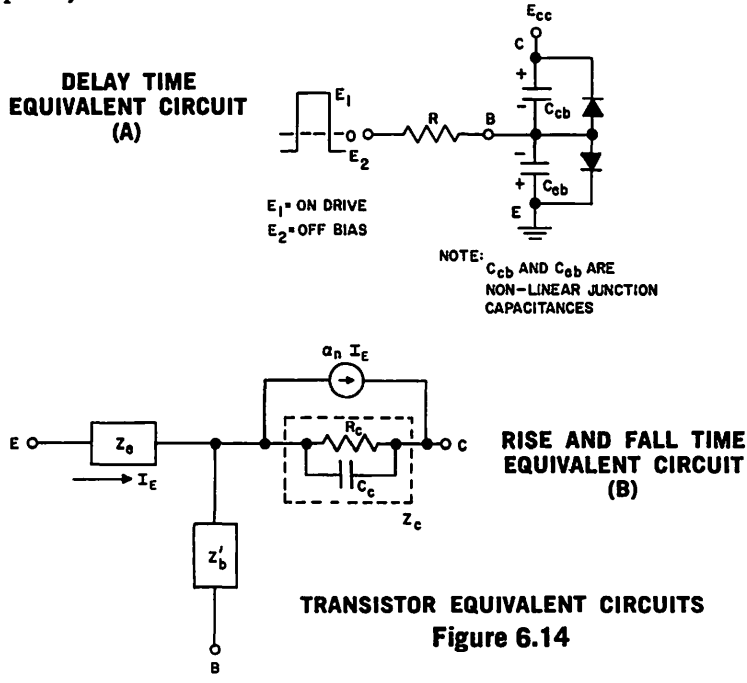



**Figure 6.13 (B)**

## TRANSIENT RESPONSE PREDICTION

A number of methods exist which enable one to predict the speed of response of a given transistor in a given circuit. Three fundamental methods are: the equivalent circuit approach, charge control analysis, and the diffusion equation solution. The equivalent circuit method normally uses the equivalent circuits shown in Figure 6.14. NPN polarity is used in the circuits.




**TRANSISTOR EQUIVALENT CIRCUITS**

**Figure 6.14**

The $\alpha_n$, the common base current gain at a frequency f, is defined as

$$\alpha_n = \frac{\alpha_N}{1 + j\frac{f}{f_\alpha}} \tag{6a}$$

where $\alpha_N$ = low frequency common-base current gain

$f_\alpha$ = alpha cutoff frequency

Since both junctions are forward biased during storage time, the inverse characteristics of the transistor are involved in storage prediction. The inverse characteristics are obtained by interchanging the collector and emitter connections in any test circuit. They are identified by the subscript I following the parameter, e.g., $h_{FEI}$ is the *inverse* DC beta. In the equivalent circuit approach, the storage time is analyzed by considering both junctions as emitting junctions. The common base current gain in the normal condition is given in equation (6a). In the inverse mode of operation,

$$\alpha_I = \frac{\alpha_I}{1 + j\frac{f}{f_{\alpha I}}} \tag{6b}$$

where

$\alpha_I$ = low frequency inverse common base current gain.

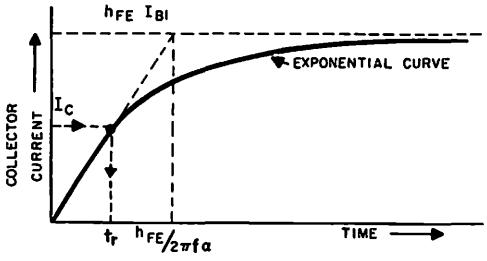
$f_{\alpha I}$ = inverse $\alpha$ cutoff frequency.

Using equivalent circuits, the storage time is defined as the time required for the collector to become back-biased – i.e., to stop emitting. As will be shown shortly, this is also the same as requiring that excess base charge be removed.

From the equivalent circuit, the transient times can be approximated. For delay time, the effects of the collector capacitance can be neglected if $E_{CC}$ is much greater than $E_2$. If $E_1$ and R (in Figure 6.14(A)) approximate a current source, then

$$t_d = \frac{C_{eb}(E_2) \times E_2}{I_{B1}} \tag{6c}$$

$C_{eb}(E_2)$ is the average effective capacitance of the emitter junction between $E_2$ volts reverse bias and the forward biased condition. A method of approximating this capacitance will be discussed later in this section in conjunction with the charge control parameters. In the following graphs results of the equivalent circuit approach are shown for the common emitter configuration. Figure 6.15 gives the rise time information.

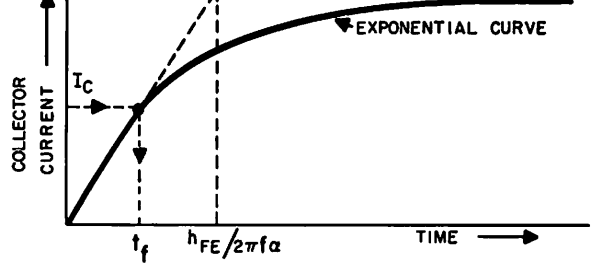



**GRAPHICAL ANALYSIS OF RISE TIME**

**Figure 6.15**

If the load resistor $R_L$ in Figure 6.9(a) is small enough that a current $h_{FE}\ I_{B1}$, through it will not drive the transistor into saturation, the collector current will rise exponentially to $h_{FE}I_{B1}$ with a time constant, $h_{FE}/2\pi f_\alpha$. However, if $R_L$ limits the current to less than $h_{FE}I_{B1}$ the same exponential response will apply, except that the curve will be terminated at $I_{CS} = \frac{V_{CC}}{R_L}$, the saturation current. Figure 6.15 illustrates the case for $I_{CS} \approx h_{FE}I_{B1}/2$. Note that the waveform will no longer appear exponential but rather almost linear. This curve can be used to demonstrate the roles of the circuit and the transistor in determining rise time. For a given transistor it is seen that increasing $h_{FE}I_{B1}/I_C$ will decrease rise time by having $I_C$ intersect the curve closer to the origin. Since the approximate equation assumes that $h_{FE}$ and $f_\alpha$ are the same for all operating points and that the collector capacitance effects are negligible, the calculated results will not fit experimental data where these assumptions are invalid. Figure 6.11(A) showed that the rise time halves as the drive current doubles, just as the expression for $t_r$ suggests, since in this case capacitance effects were small; however, the calculated value for $t_r$ using the approximate expression is in error by more than 50%. This shows that even though the calculations may be in error, if the response time is specified for a circuit, it is possible to judge fairly accurately how it will change with circuit modifications using the above equations.

Collector current fall time can be analyzed in much the same manner as rise time. Figure 6.16 indicates the exponential curve of amplitude $I_C + h_{FE}I_{B2}$, and a time constant, $h_{FE}/2\pi f_\alpha$. Fall time is given by the time it takes the exponential to reach $I_{CS}$.




$$t_f = \frac{1+2\pi f_\alpha R_L C_{cb}}{2\pi f_\alpha (1-\alpha_N)} \ln \frac{h_{FE} I_{B2} + I_{CS}}{h_{FC} I_{B2}}$$

$$t_f \simeq \frac{1}{2\pi f_\alpha} \frac{h_{FE} I_{CS}}{h_{FE} I_{B2} + I_{CS}} \quad \text{IF } 2\pi f_\alpha R_L C_{cb} << 1 \text{ AND } h_{FE} I_{B2} > 3 I_{CS}$$

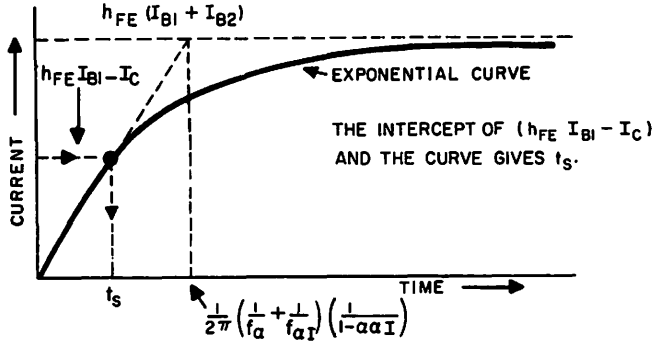
**GRAPHICAL ANALYSIS OF FALL TIME**

**Figure 6.16**

In the approximate expression in Figure 6.16, $t_f$ will be approximately equal to $\frac{1}{2\pi f_\alpha} \times \frac{I_{CS}}{I_{B2}}$ if $h_{FE}$ is very large compared to $I_{CS}/I_{B2}$.

Figure 6.17 shows a curve which is useful for calculating storage time graphically. The maximum value is $h_{FE}$ ($I_{B1} + I_{B2}$), where $I_{B2}$ is given the same sign as $I_{B1}$, ignoring

the fact it flows in the opposite direction. The time constant of the curve involves the forward and inverse current gain and frequency cut-off. The storage time corresponds to the time required to reach the current $h_{FE}I_{B1} - I_C$. It can be seen that for a given frequency response, high $h_{FE}$ gives long storage time. The storage time also decreases as $I_{B2}$ is increased or $I_{B1}$ is decreased.




$$t_S = \frac{1}{2\pi}\left(\frac{1}{f_\alpha}+\frac{1}{f_{\alpha I}}\right)\left(\frac{1}{1-\alpha_N\alpha_I}\right)\ln\left[\frac{h_{FE}(I_{B1}+I_{B2})}{h_{FE}I_{B2}+I_{CS}}\right]$$

$$t \simeq \frac{1}{2\pi I_{B2}}\left(\frac{1}{f_\alpha}+\frac{1}{f_{\alpha I}}\right)\left(\frac{1}{1-\alpha_N\alpha_I}\right)\left(I_{B1}-\frac{I_C}{h_{FE}}\right) \text{ IF } h_{FE}I_{B1} > 3I_{CS}$$

**GRAPHICAL ANALYSIS OF STORAGE TIME**

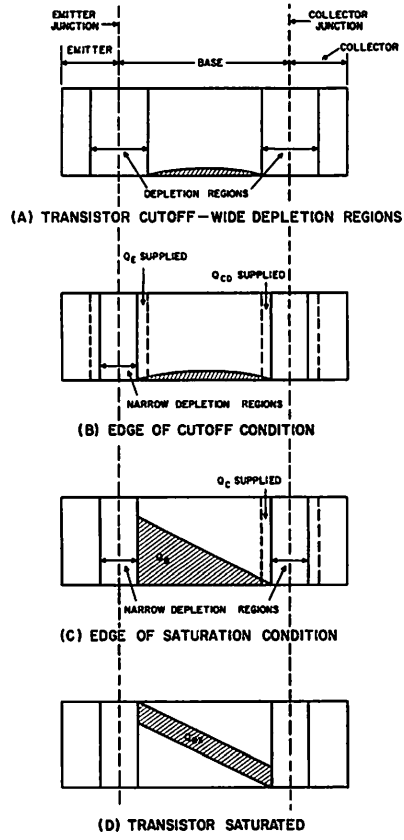
**Figure 6.17**

The time constant for a very unsymmetrical transistor is approximately $\frac{h_{FEI}+1}{2\pi f_{\alpha I}}$. It is seen that the generally specified normal $h_{FE}$ and $f_\alpha$ are of little use in determining storage time. For a symmetrical transistor, the time constant is approximately $\frac{h_{FE}+1}{2\pi f_\alpha}$. It is possible for a symmetrical transistor to have a longer storage time than an unsymmetrical transistor with the same $h_{FE}$ and $f_\alpha$.

Using the charge control approach, the transistor is viewed from a more fundamental vantage point. The actual charge requirements of various regions within the device are determined, and the transient times are found by calculating the time required to supply the various charge components. The emitter and collector junctions of a transistor when in the cutoff condition are reversed biased; in this condition only leakage currents flow across the junctions, the base charge is negligible and the junction depletion layers are wide because of the reverse bias applied as shown in Figure 6.18(A). In Figure 6.9(A), this condition exists in the transistor when the switch is open; $V_{BE}$ is equal to −10 volts and $V_{CB}$ is equal to 20 volts. Immediately after the switch is closed, no collector current flows since the emitter junction is reverse biased, thus the initial base current which flows supplies charge to the emitter and collector junction depletion layers and soon causes the emitter junction to become forward biased and begin emitting as shown in Figure 6.18(B). The quantity of charge which has been supplied to the emitter junction depletion region is called $Q_E$ and is a function of the reverse bias voltage which was applied to the junction prior to the application of the turn-on signal. The charge supplied to the collector depletion region during this time is denoted $Q_{CD}$ and is a function of the reverse bias on the emitter,

and the collector supply voltage being switched. Looking again at Figure 6.9(A), the condition illustrated in Figure 6.18(B) exists when $V_{BE}$ equals about .3 volts and $V_{CB}$ equals about 10 volts.

With the emitter junction now forward biased, the transistor enters the active region. Collector current begins to flow and the voltage at the collector begins to drop because of the presence of the collector load resistor, $R_L$, shown in Figure 6.9(A). During this time a gradient of charge is established in the base region of the transistor. The slope of this charge gradient is proportional to the collector current which is flowing. If the base current supplied is greater than the rate of recombination of charge in the base region, the gradient will continue to rise until an equilibrium condition is reached. If equilibrium is reached before the collector junction is forward biased, the transistor will not saturate. Since the recombination rate of charge in the base is $I_C/h_{FE}$ (or $I_{B1}$), the collector current will rise to $h_{FE}$ $I_{B1}$ if the device does not saturate. If, on the other hand, the collector current causes the collector-base junction to become forward biased before equilibrium is reached, the device will saturate. The existing condition within the transistor at the edge of saturation is depicted in Figure 6.18(C). The time required to move from the edge of cutoff to the




**CHARGE DISTRIBUTION IN TRANSISTOR DURING SWITCHING**

**Figure 6.18**

edge of saturation is the rise time. Charge quantities involved are the base gradient of charge $Q_B$, which is a function of collector current flowing, and $Q_C$, which is a function of $V_{CB}$. $Q_C$ is the charge required to cause the collector junction to narrow and becomes forward biased. Since measurement of $Q_B$ and $Q_C$ is frequently accomplished by measuring the two quantities together and then separating them as shown in Chapter 15, the sum of $Q_B$ and $Q_C$ is frequently used and is called $Q_B$*. At the edge of saturation the $V_{BE}$ is about .3 volt and $V_{CB}$ is 0 volts if the bulk resistance of the collector body is neglected. Since equilibrium is not established with respect to the base current, charge in excess to that required to saturate the transistor is introduced into the base region. The base gradient of charge remains constant since the collector current is at a maximum for the circuit; the excess charge, $Q_{BX}$, is a function of the current which is permitted to flow into the base in excess of that required to saturate the transistor. This current is called $I_{BX}$. Distribution of $Q_{BX}$ in the transistor is shown in Figure 6.18(D).

In the alloy type transistor, essentially all of the stored charge is in the base region. In devices where the collector bulk region has high minority carrier lifetime, excess carriers can also be stored in the collector. These carriers reach the collector from the base since the collector junction is now forward biased and base majority carriers are free to flow into the collector region during saturation. These stored carriers have no effect in turn-on time. Storage time, however, is the time required to remove these stored carriers as well as those stored in the base. Both the mesa and planar devices exhibit collector minority carrier storage. The epitaxial process used in General Electric transistors 2N781, 2N914, 2N994 and the 2N2193 minimizes collector storage while not adversely effecting collector breakdown voltage or other desirable characteristics of the transistor. Incidentally, it may be possible to meet the electrical specification of a given registration without using epitaxial techniques. Component manufacturer's data should be consulted for process information.

From the various charge quantities introduced, a number of time constants can be described that relate the charge quantities to the currents flowing; these time constants are defined in equations (6d).

$$\tau_a = \frac{Q_B}{I_{BS}}$$

$$\tau_c = \frac{Q_B}{I_{CS}} \qquad (6d)$$

$$\tau_b = \frac{Q_{BX}}{I_{BX}}$$

$\tau_a$ is called the *active region lifetime,* $\tau_c$ is called the *collector time constant,* and $\tau_b$ is the *effective lifetime in the saturated region.* In some literature $\tau_b$ has been called $\tau_s$. Where collector minority carrier storage exists the measurement method for $\tau_b$ shown in Chapter 15 does not only measure $Q_{BX}/I_{BX}$ but includes much of the collector stored charge; as such, this parameter is still a valuable tool in rating the storage characteristics of various transistors since a low $\tau_b$ value indicates a low storage time. The time constants defined are *constant* over large regions of device usage and are normally specified as device constants.

To determine the transient response using the charge approach, the required charge for the time in question is divided by the current available to supply that charge; thus, the basic equations are as given in Equation (6e).

$$
\begin{aligned}
t_d &= \frac{Q_E + Q_{CD}}{I_{B1}} \\
t_r &= \frac{Q_B + Q_C}{I_{B1}} = \frac{\tau_c I_c + Q_C}{I_{B1}} \\
t_s &= \frac{Q_{BX}}{I_{B2}} = \tau_b \frac{I_{BX}}{I_{B2}} \\
t_f &= \frac{Q_B + Q_C}{I_{B2}} = \frac{\tau_c I_c + Q_C}{I_{B2}}
\end{aligned}
\tag{6e}
$$

The simplicity of these equations is readily seen. Their accuracy is dependent upon the assumption made in the equations that $I_{B1}$ and $I_{B2}$ truly are constant. Refinements in these equations arise from the fact that some of the charge in the base recombines on its own and must be accounted for in determining transient speed. These refinements are seen primarily in equations (6f) for rise and fall time.

$$
\begin{aligned}
t_r &= \frac{Q_B + Q_C}{I_{B1} - .5\, I_{BS}} \\
t_f &= \frac{Q_B + Q_C}{I_{B1} + .5\, I_{BS}}
\end{aligned}
\tag{6f}
$$

Equations (6e) and (6f) assume that the current $I_{B1}$ is sufficient to drive the transistor well into saturation. If $I_{B1}$ is three times greater than $I_{BS}$, these equations are valid. For the cases where the drive-on is not large compared to $I_{BS}$, but nevertheless is greater than $I_{BS}$, equations (6g) are more accurate expressions.

$$
\begin{aligned}
t_r &= \left[\tau_a + \frac{h_{FE}\, R_L\, Q_C}{V_{CC}}\right] \ln\left(\frac{I_{B1}}{I_{B1} - I_{BS}}\right) \\
t_s &= \tau_b \ln \frac{I_{B1} + I_{B2}}{I_{B2} + I_{BS}} \\
t_f &= \left[\tau_a + \frac{h_{FE}\, R_L\, Q_C}{V_{cc}}\right] \ln\left(\frac{I_{B2} + I_{BS}}{I_{B2}}\right)
\end{aligned}
\tag{6g}
$$

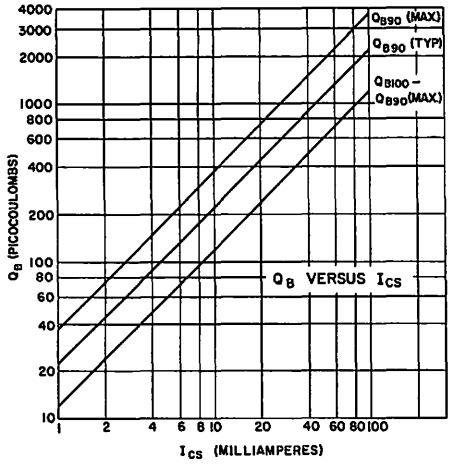
The lack of simplicity of these equations is also readily seen. If the drive-on current is not sufficient to drive the transistor into saturation the collector current will rise to $h_{FE}\, I_B$ with a time constant slightly greater than $\tau_a$ as shown in (6g). Fall time is also determined by using the time constant of the $t_f$ expression in (6g), but the magnitude attempts to reach $h_{FE}\, I_{B2}$ in the reverse direction before it is interrupted at $I_c = 0$. Thus, the turn-off time from the non-saturated state is

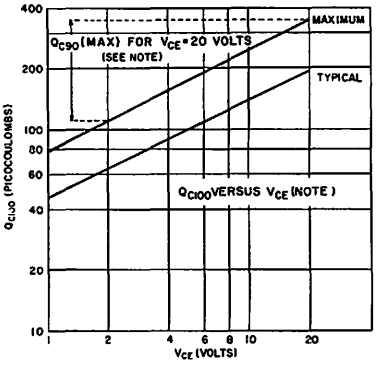
$$
t_f = \left[\tau_a + \frac{h_{FE}\, R_L\, Q_C}{V_{cc}}\right] \ln\left(\frac{I_{B2} + I_{B1}}{I_{B2}}\right)
$$

The charge control parameters as they appear on the 2N396A alloy device are shown in Figure 6.19(A). On the specification, transient times are defined from 10% to 90% points to make their measurements easier as shown in Figure 6.9(D). This definition, however, demands that the equations be slightly modified to accommodate these new definitions of transient times. The modified form is shown in Figure 6.19(A) with the 2N396A specification. Figure 6.19(B) shows the charge graphs for the 2N994.

Frequently, it is convenient to know some of the relationships between charge control parameters and small signal parameters. Convenient approximate interrelationships are shown in equations (6h).

$$
\begin{aligned}
Q_B &= I_B\, \tau_a = I_B \cdot \frac{h_{FE}}{2\pi f_\alpha} \\
Q_B &= I_c\, \tau_c = I_c \cdot \frac{1}{2\pi f_\alpha} \text{ or } I_c \cdot \frac{1}{2\pi f_T} \\
\frac{\tau_a}{\tau_c} &= h_{FE}
\end{aligned}
\tag{6h}
$$




SPECIFICATION $T_A$ = 25° C)

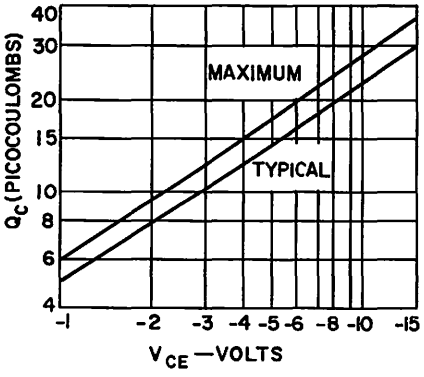
| | 2N396A MIN. | TYP. | MAX. | |
|---|---|---|---|---|
| $\tau_a$, ACTIVE REGION LIFETIME | 1.1 | 1.8 | | μs |
| $\tau_b$, SATURATED REGION LIFETIME | | .65 | 1.2 | μs |
| $\overline{C_{BE}}$, AVERAGE EMITTER JUNCTION CAPACITANCE | | 12 | 17 | pf |

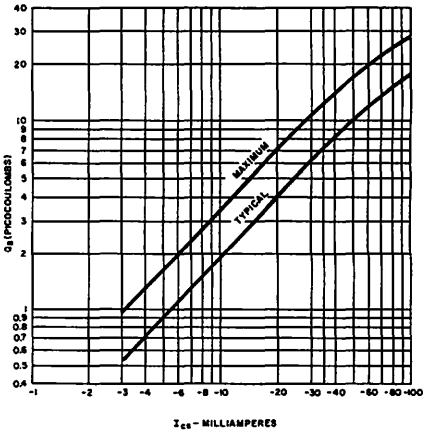
$$t_d = \frac{V_{BE\,(OFF)}\,\overline{C_{BE}}}{I_{B1}} + 1/9 \times \frac{Q_{B90}+Q_{C90}}{I_{B1}-.5I_{BS}} \qquad t_r = 8/9 \times \frac{Q_{B90}+Q_{C90}}{I_{B1}-.5I_{BS}} \qquad t_s = \tau_b \ln\left(\frac{I_{B1}+I_{B2}}{I_{BS}+I_{B2}}\right) +$$

$$\frac{(Q_{B100}-Q_{B90})+(Q_{C100}-Q_{B90})}{+I_{B2}+.5I_{BS}} \qquad t_f = 8/9 \times \frac{Q_{B90}+Q_{C90}}{+I_{B2}+.5I_{BS}}$$

NOTE: $Q_{C90} = Q_{C100}$ AT $V_{CE}$ MINUS $Q_{C100}$ AT .1 $V_{CE}$ AS ILLUSTRATED FOR $V_{CE}$ = 20 VOLTS IN THE $Q_{C100}$ VS. $V_{CE}$ PLOT.

**2N396A SWITCHING SPECIFICATION**
**(A)**




**2N994 CHARGE SPECIFICATION**
**(B)**

**Figure 6.19**

Expressions for the emitter and collector depletion layer charge can be approximated from small signal capacitance measurements on the respective junctions. If $C_{ob}$ is known at some reverse bias $V_{CB}$ with $I_E = 0$, the $Q_C$ can be approximated if it is known whether the device has alloy, grown, or diffused junctions. If the device is an alloy transistor, then

$$C_{ob} = k\, V_{CB}^{-1/2} \tag{6i}$$

where k is a proportionality constant. The approximate depletion layer charge required for the alloy junction voltage to move from $V_{CB1}$ to $V_{CB2}$ is found from equations 6j and 6k or Table 6.1.

$$Q_C = \int_{V_{CB1}}^{V_{CB2}} C_{ob}\, dV = \int_{V_{CB1}}^{V_{CB2}} kV^{-1/2}\, dV \tag{6j}$$

$$Q_C = 2\, k\, V_{CB}^{1/2} \Big|_{V_{CB1}}^{V_{CB2}} = 2\, k\, (V_{CB2}^{1/2} - V_{CB1}^{1/2}) \tag{6k}$$

The value of k is found from the small signal capacitance measurement and the expression given in equation (6i); that is, the junction constant k is found for the collector junction of an alloy transistor by multiplying the measured $C_{ob}$ by $(V_{CB})^{1/2}$ where $V_{CB}$ is the measurement voltage. Table 6.1 gives these formulae for other structures. For grown junctions, the capacitance is proportional to $V_{CB}^{-1/3}$ while for diffused junctions — mesa and planar structures — an approximate value of $V_{CB}^{-0.4}$ is frequently used. The diffused junction capacitance may, however, be proportional to voltage functions anywhere from $V_{CB}^{-1/3}$ to $V_{CB}^{-1/2}$ and will vary with voltage level. Table 6.1 indicates some of the results from these considerations.

| Parameter | Alloy | Grown | Diffused |
|---|---|---|---|
| $C_{ob}$ | $k_c\, V_{BC}^{-1/2}$ | $k_c\, V_{CB}^{-1/3}$ | $k_c\, V_{CB}^{-0.4}$ |
| $C_{ib}$ | $k_e\, V_{EB}^{-1/2}$ | $k_e\, V_{EB}^{-1/3}$ | $k_e\, V_{EB}^{-0.4}$ |
| $Q_C$ | $2k_c\, V_{CB}^{1/2} \Big\vert_{V_{CB1}}^{V_{CB2}}$ | $1.5k_c\, V_{CB}^{2/3} \Big\vert_{V_{CB1}}^{V_{CB2}}$ | $1.6k_c\, V_{CB}^{0.6} \Big\vert_{V_{CB1}}^{V_{CB2}}$ |
| $Q_E$ | $2k_c\, V_{EB}^{1/2} \Big\vert_{V_{EB1}}^{V_{EB2}}$ | $1.5k_e\, V_{CB}^{2/3} \Big\vert_{V_{EB1}}^{V_{EB2}}$ | $1.6k_e\, V_{EB}^{0.6} \Big\vert_{V_{EB1}}^{V_{EB2}}$ |
| $k_c$* | $C_{ob}\, V_{CB}^{1/2}$ | $C_{ob}\, V_{CB}^{1/3}$ | $C_{ob}\, V_{CB}^{0.4}$ |
| $k_e$* | $C_{ib}\, V_{EB}^{1/2}$ | $C_{ib}\, V_{EB}^{1/3}$ | $C_{ib}\, V_{EB}^{0.4}$ |

*The $V_{CB}$ or $V_{EB}$ in these expressions is the measurement voltage for $C_{ob}$ or $C_{ib}$ respectively.

## Table 6.1

### APPROXIMATE VALUES OF $Q_C$ AND $Q_E$ FROM $C_{ob}$ AND $C_{ib}$

An instance where Table 6.1 would be of value is in determining the charge requirements for delay time. From equations (6d), it is seen that the delay time charge is $Q_E + Q_{CD}$. If the reverse bias on an alloy transistor is $V_2$ and the supply voltage is $V_{cc}$, then

$$Q_E = 2k_e V_{EB}^{1/2}\Big|_0^{V_2} = 2k_e V_2^{1/2}$$

$$Q_{CD} = 2k_c V_{CB}^{1/2}\Big|_{V_{cc}}^{V_2 + V_{cc}} = 2k_c\left[(V_2 + V_{cc})^{1/2} - V_{cc}^{1/2}\right]$$

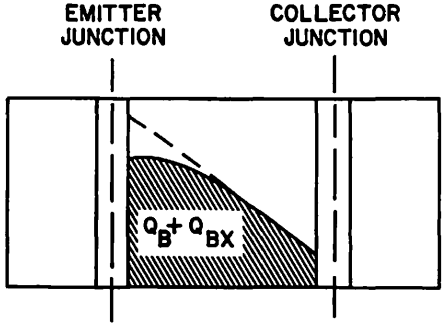
or

$$Q_E + Q_{CD} = 2k_e V_2^{1/2} + 2k_c\left[(V_2 + V_{cc})^{1/2} - V_{cc}^{1/2}\right]$$

On the 2N396A specification shown in Figure 6.19, the $Q_{CD}$ value would be taken from the $Q_{C100}$ graph by finding $Q_C$ at $V_2 + V_{cc}$ and subtracting $Q_C$ at $V_{cc}$ from it. $\overline{C_{BE}}$ is specified as the average base-emitter junction capacitance and is essentially equivalent to the capacitance at 1 volt reverse bias. The $C_{BE}$ value is thus numerically equal to $k_e$. Using these charge parameters, one can rapidly determine response characteristics. Even if the input is not a current source, the charge requirements of the device are useful. For example, the speed-up capacitor in RCTL (Resistance Capacitor Transistor Logic) circuits can be estimated.

Also, since the charge graphs as shown in Figure 6.19 illustrate the effects of collector current and voltage separately, a designer can readily estimate the effects of supply voltage or load current variation on the transient response of a circuit. It is interesting to note, for example, that at high current levels in the 2N396A specification the depletion layer charge, $Q_C$, is only a small fraction of $Q_B$, whereas on a mesa device like the 2N781 or 2N994, the collector depletion charge $Q_C$ is a large fraction of the total base charge ($Q_B + Q_C$) at almost all operating points of interest, as shown in Figure 6.19 for the 2N396A and 2N994. These observations would argue that for alloy transistors the supply voltage level which is being used need not be as critically selected as for mesa units, and that the mesa's ability to switch rapidly is shown more readily at low collector supply voltages.

Solution of the diffusion equation for transient speed of a transistor is beyond the scope of this manual. Two important results of this analysis should be stated however. First, any prediction using equations given in this section to predict a response time approaching $1/(25\ f_\alpha)$ should not be accepted since approximations made are not valid at these speeds. Secondly, as $I_{B2}$ becomes larger, the error in storage and fall time equations increases since the minority carrier density in the base, shortly after the application of the turn-off pulse, is not as shown in Figure 6.18(D), but is more like that shown in Figure 6.20

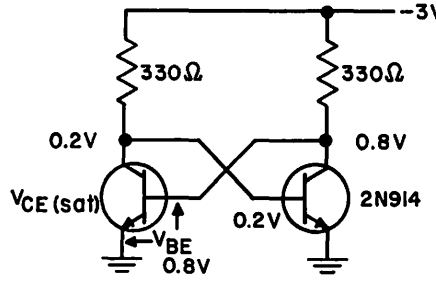



**BASE CHARGE DISTRIBUTION WITH LARGE $I_{B2}$**

**Figure 6.20**

## CIRCUIT TECHNIQUES TO AUGMENT SWITCHING CHARACTERISTICS

Some circuits have been designed making specific use of saturation. The direct coupled transistor logic (DCTL) flip-flop shown in Figure 6.21 utilizes saturation. In saturation $V_{CE\,(SAT)}$ can be so low that if this voltage is applied between the base and emitter of another transistor, as in this flip-flop, there is insufficient forward bias to cause this transistor to conduct appreciably. The extreme simplicity of the circuit




**DIRECT COUPLED TRANSISTOR LOGIC (DCTL) FLIP-FLOP**
**Figure 6.21**

is self evident and is responsible for its popularity. However, special requirements are placed on the transistors. The following are among the circuit characteristics:

First, the emitter junction is never reverse biased permitting excessive current to flow in the off transistor at temperatures above 40°C in germanium. In silicon, however, operation to 150°C has proved feasible.

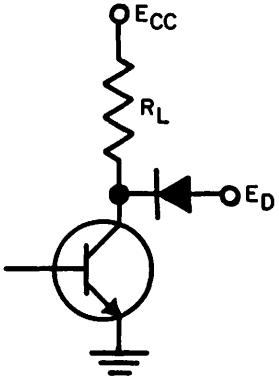
Second, saturation is responsible for a storage time delay slowing up circuit speed. In the section on transient response we see the importance of drawing current out of the base region to increase speed. In DCTL this current results from the difference between $V_{CE\,(SAT)}$ and $V_{BE}$ of a conducting transistor. To increase the current, $V_{CE\,(SAT)}$ should be small and $r_b'$ should be small. However, if one collector is to drive more than one base, $r_b'$ should be relatively large to permit uniform current sharing between bases since large base current unbalance will cause large variations in transient response resulting in circuit design complexity. High base recombination rates and epitaxial collectors to minimize collector storage result in short storage times in spite of $r_b'$.

Third, since $V_{CE\,(SAT)}$ and $V_{BE}$ differ by less than .3 volt in germanium, stray voltage signals of this amplitude can cause faulty performance. While stray signals can be minimized by careful circuit layout, this leads to equipment design complexity. Silicon transistors with a 0.6 volt difference between $V_{CE\,(SAT)}$ and $V_{BE}$ are less prone to being turned on by stray voltages but are still susceptible to turn-off signals. This is somewhat compensated for in transistors with long storage time delay since they will remain on by virtue of the stored charge during short turn-off stray signals. This leads to conflicting transistor requirements – long storage time for freedom from noise, short storage time for circuit speed.

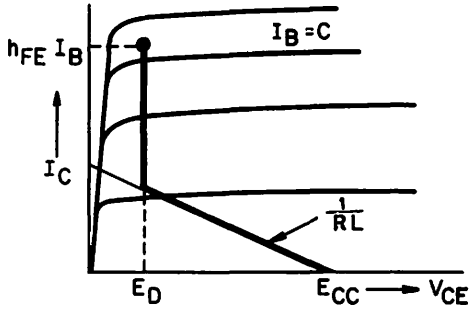
Another application of saturation is in saturated flip-flops of conventional configuration. Since $V_{CE\,(SAT)}$ is generally very much less than other circuit voltages, saturating the transistors permits the assumption that all three electrodes are nearly at the same potential making circuit voltages independent of transistor characteristics. This yields good temperature stability and good interchangeability. The stable voltage levels are

useful in generating precise pulse widths with monostable flip-flops. The section on flip-flop design indicates the ease with which saturated circuits can be designed.

In general, the advantages of saturated switch design are: (a) simplicity of circuit design, (b) well defined voltage levels, (c) fewer parts required than in non-saturating circuits, (d) low transistor dissipation when conducting, and (e) immunity to short stray voltage signals. Against this must be weighed the probable reduction in circuit speed since higher trigger power is required to turn off a saturated transistor than one unsaturated.




DIODE COLLECTOR CLAMPING CIRCUIT TO AVOID SATURATION




COLLECTOR CHARACTERISTICS SHOWING LOAD LINE AND OPERATING POINTS

**COLLECTOR VOLTAGE CLAMP**

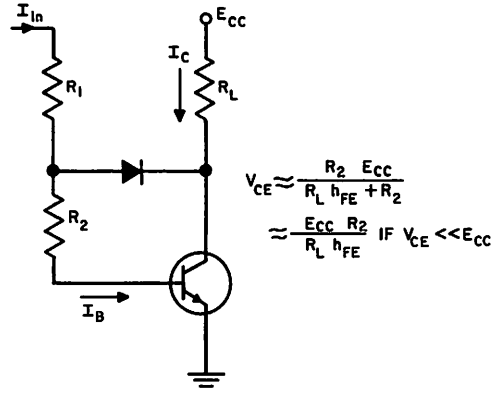
**Figure 6.22**

A number of techniques are used to avoid saturation. The simplest is shown in Figure 6.22. The diode clamps the collector voltage so that it cannot fall below the base voltage to forward bias the collector junction. Response time is not improved appreciably over the saturated case since $I_C$ is not clamped but rises to $h_{FE}I_B$. Typical variations of $I_B$ and $h_{FE}$ with temperature and life, for a standard transistor, may vary $I_C$ by as much as 10:1. Care should be taken to ensure that the diode prevents saturation with the highest $I_C$. When the transistor is turned off $I_C$ must fall below the value given by $(E_{CC} - E_D)/R_L$ before any change in collector voltage is observed. The time required can be determined from the fall time equations in the section on transient response. The diode can also have a long recovery time from the high currents it has to handle. This can further increase the delay in turning off. Diodes such as the 1N3604 or 1N3606 have recovery times compatible with high speed planar epitaxial transistors.

A much better way of avoiding saturation is to control $I_B$ in such a way that $I_C$ is just short of the saturation level. This can be achieved with the circuit of Figure 6.23(A). The diode is connected between a tap on the base drive resistor and the collector. When the collector falls below the voltage at the tap, the diode conducts diverting base current into the collector and preventing any further increase in $I_C$. The voltage drop across $R_2$ is approximately $I_CR_2/h_{FE}$ since the current in $R_2$ is $I_B$. Since the voltage drop across the diode is approximately the same as the input voltage to the transistor, $V_{CE}$ is approximately $I_CR_2/h_{FE}$. It is seen that if the load decreases ($I_C$ is reduced) or $h_{FE}$ becomes very high, $V_{CE}$ decreases towards saturation. Where the

change in $h_{FE}$ is known and the load is relatively fixed, this circuit prevents saturation.

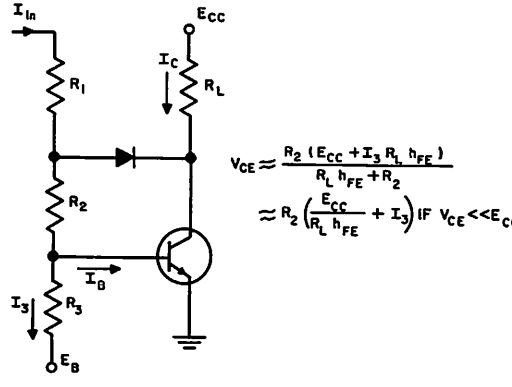
To avoid the dependence of $V_{CE}$ on $I_C$ and $h_{FE}$, $R_3$ may be added as in Figure 6.23(B). By returning $R_3$ to a bias voltage, an additional current is drawn through $R_2$. Now $V_{CE}$ is approximately $(\frac{I_C}{h_{FE}} + I_3)\, R_2$. $I_3$ can be chosen to give a suitable minimum $V_{CE}$.




**COLLECTOR CURRENT CLAMP WITHOUT BIAS SUPPLY**

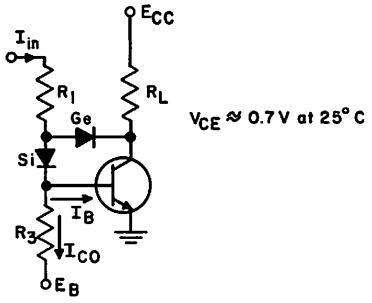
**Figure 6.23(A)**

The power consumed by $R_3$ can be avoided by using the circuit of Figure 6.23(C), provided a short lifetime transistor is used. Otherwise fall times may be excessively long. $R_3$ is chosen to reverse bias the emitter at the maximum $I_{CO}$. The silicon diode replaces $R_2$. Since the silicon diode has a forward voltage drop of approximately .7 volts over a considerable range of current, it acts as a constant voltage source making $V_{CE}$ approximately .7 volts. If considerable base drive is used, it may be necessary to use a high conductance germanium diode to avoid momentary saturation as the voltage drop across the diode increases to handle the large base drive current.




**COLLECTOR CURRENT USING BIAS SUPPLY**

**Figure 6.23(B)**




**COLLECTOR CURRENT CLAMP USING SILICON AND GERMANIUM DIODES**

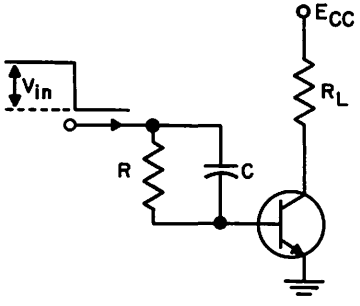
**Figure 6.23(C)**

In applying the same technique to silicon transistors with low saturation resistance, it is possible to use a single germanium diode between the collector and base. While this permits $V_{CE}$ to fall below $V_{BE}$, the collector diode remains essentially non-conducting since the .7 volt forward voltage necessary for conduction cannot be reached with the germanium diode in the circuit.

Diode requirements are not stringent. The silicon diode need never be back biased, consequently, any diode will be satisfactory. The germanium diode will have to withstand the maximum circuit $V_{CE}$, conduct the maximum base drive with a low forward voltage, and switch rapidly under the conditions imposed by the circuit, but these requirements are generally easily met.

Care should be taken to include the diode leakage currents in designing these circuits for high temperatures. All the circuits of Figure 6.23 permit large base drive currents to enhance switching speed, yet they limit both $I_B$ and $I_C$ just before saturation is reached. In this way, the transistor dissipation is made low and uniform among transistors of differing characteristics.

It is quite possible to design flip-flops which will be non-saturating without the use of clamping diodes by proper choice of components. The resulting flip-flop is simpler than that using diodes but it does not permit as large a load variation before malfunction occurs. Design procedure for an unclamped non-saturating flip-flop can be found in *Transistor Circuit Engineering* by R. F. Shea, et al (John Wiley & Sons, Inc).




**STORED CHARGE NEUTRALIZATION BY CAPACITOR**

**Figure 6.24**

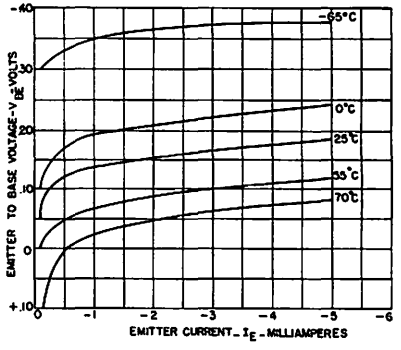
Another circuit which is successful in minimizing storage time is shown in Figure 6.24. If the input is driven from a voltage source, it is seen that if the input voltage and capacitor are appropriately chosen, the capacitor charge can be used to neutralize the stored charge, in this way avoiding the storage time delay. In practical circuits, the RC time constant in the base necessary for this action limits the maximum pulse repetition rate.

# BIASING

CHAPTER 7

One of the basic problems involved in the design of transistor amplifiers is establishing and maintaining the proper collector to emitter voltage and emitter current (called the biasing conditions) in the circuit. These biasing conditions must be maintained despite varations in ambient temperature and variations of gain and leakage current between transistors of the same type. The factors which must be taken into account in the design of bias circuits would include:

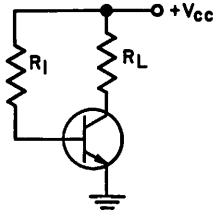
1. The specified maximum and minimum values of current gain ($h_{FE}$) at the operating point for the type of transistor used.
2. The variation of $h_{FE}$ with temperature. This will determine the maximum and minimum values of $h_{FE}$ over the desired temperature range of operation. The variation of $h_{FE}$ with temperature is shown in Figure 6.7 for the 2N525 transistor.
3. The variation of collector leakage current ($I_{CO}$) with temperature. For most transistors, $I_{CO}$ increases at approximately 6.5-8%/°C and doubles with a temperature change of 9-11°C. In the design of bias circuits, the minimum value of $I_{CO}$ is assumed to be zero and the maximum value of $I_{CO}$ is obtained from the specifications and from a curve such as Figure 6.6. If silicon transistors are used, it is best to use the specified high temperature $I_{CO}$ for estimating the maximum $I_{CO}$.
4. The variation of base to emitter voltage drop ($V_{BE}$) with temperature. Under normal bias conditions, $V_{BE}$ is about 0.2 volts for germanium transistors and 0.7 volts for silicon transistors and has a temperature coefficient of about —2.5 millivolts per °C. Figure 7.1 shows the variation of $V_{BE}$ with collector current at several different temperatures for the 2N525. Note that for some conditions of high temperature it is necessary to reverse bias the base to get a low value of collector current.
5. The tolerance of the resistors used in the bias networks and the tolerance of the supply voltages.



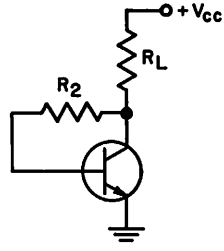

**INPUT CHARACTERISTICS OF 2N525 ($V_{CE}$ = 1V)**

**Figure 7.1**

Two of the simpler types of bias circuits are shown in Figures 7.2 and 7.3. These circuits can be used only in cases where a wide range of collector voltage can be tolerated (for Figure 7.2 at least as great as the specified range of $h_{FE}$) and where $h_{FE}^{max}$ times $I_{CO}^{max}$ is less than the maximum desired bias current. Neither circuit can be used with transistors which do not have specifications for maximum and minimum $h_{FE}$ unless the bias resistors are selected individually for each transistor. The circuit of Figure 7.3 provides up to twice the stability in collector current with changes in $h_{FE}$ or $I_{CO}$ than the circuit of Figure 7.2. However, the circuit of Figure 7.3 has a-c feedback through the bias network which reduces the gain and input impedance slightly. This feedback can be reduced by using two series resistors in place of $R_2$ and connecting a capacitor between their common point and ground.




$$I_C = h_{FE}\left(\frac{V_{CC}}{R_1} + I_{CO}\right)$$

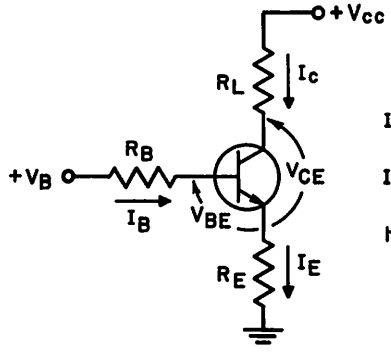



$$I_C = \frac{h_{FE}(V_{CC} + I_{CO}R_2)}{R_2 + h_{FE}R_L}$$

TRANSISTOR BIAS CIRCUITS

**Figure 7.2** **Figure 7.3**

In cases where more stability is desired than is provided by the circuits of Figure 7.2 or 7.3, it is necessary to use a resistor in series with the emitter of the transistor as shown in Figure 7.4. There are several variations of this circuit, all of which may be obtained by the general design procedure outlined below. The currents shown in Figure 7.4 are those which would be measured if an ammeter were inserted in that circuit; thus, for example, the value of $I_B$ in the figure includes $I_{CO}$.




$$I_C = \alpha I_E + I_{CO}$$

$$I_C = h_{FE} I_B + (h_{FE} + 1) I_{CO}$$

$$h_{FE} = \frac{\alpha}{1-\alpha}$$

BASIC TRANSISTOR BIAS CIRCUIT

**Figure 7.4**

For the circuit of Figure 7.4, the following equations apply:

$$I_E = (h_{FE} + 1)(I_B + I_{CO}) \tag{7a}$$

$$V_B = \left[\frac{R_B}{(h_{FE} + 1)} + R_E\right] I_E + V_{BE} - I_{CO}R_B \tag{7b}$$

Considering bias conditions at the temperature extremes, at the minimum temperature, $I_E$ will have its minimum value and the worst conditions would occur for $h_{FE} = h_{FE}^{min}$, $V_{BE} = V_{BE}^{max}$, $I_{CO} = 0$ or

$$\text{at lowest temperature:} \quad V_B = \left[\frac{R_B}{h_{FE}^{min} + 1} + R_E\right] I_E^{min} + V_{BE}^{max} \tag{7c}$$

and at the highest temperature of operation $I_E$ will have its maximum value and the worst conditions would occur for $h_{FE} = h_{FE}^{max}$, $V_{BE} = V_{BE}^{min}$, $I_{CO} = I_{CO}^{max}$.

$$\text{at highest temperature:} \quad V_B = \left[\frac{R_B}{h_{FE}^{max} + 1} + R_E\right] I_E^{max} + V_{BE}^{min} - I_{CO}^{max} R_B. \tag{7d}$$

from these two equations the value of $R_B$ can be calculated by equating the two expressions:

$$R_B = \frac{(I_E^{max} - I_E^{min})R_E + V_{BE}^{min} - V_{BE}^{max}}{I_{CO}^{max} - \frac{I_E^{max}}{h_{FE}^{max} + 1} + \frac{I_E^{min}}{h_{FE}^{min} + 1}} \tag{7e}$$

As an example, consider the following bias circuit design:

1. Select the transistor type to be used (2N525)
2. Determine the required range of temperature

   0°C to + 55°C
3. Select the supply voltage and load resistance

   $V_{CC} = 20$ volts; $R_L = 7.5K$
4. Determine $I_{CO}^{max}$:

   From the electrical specifications the upper limit of $I_{CO}$ is 10 $\mu$a at 25°C and from Figure 6.6 $I_{CO}$ will increase by a factor of 10 at 55°C, thus $I_{CO}^{max} = 10 \times 10 = 100$ $\mu$a.
5. Determine the values of $h_{FE}^{min}$ and $h_{FE}^{max}$

   From the electrical specifications, the range of $h_{FE}$ at 25°C is 34 to 65. From Figure 6.7 $h_{FE}$ can change by a factor of 0.75 at 0°C and by a factor of 1.3 at +55°C.

   Thus $h_{FE}^{min} = 0.75 \times 34 = 25$ and $h_{FE}^{max} = 1.3 \times 65 = 85$.
6. Determine the allowable range of $I_E$:

   In general, the variation of the circuit performance with emitter current determines the allowable range of emitter current. In some cases the allowable range of emitter current is determined by the peak signal voltage required across $R_L$.

   Assume that the minimum current is .67 ma which gives a minimum voltage of 5 volts across $R_L$ and the maximum emitter current is 1.47 ma which gives a maximum voltage of 11 volts across $R_L$. The allowable range of emitter current must be modified to take into account the tolerance of the bias resistors. That is, if the allowable range of emitter current is .67 ma to 1.47 ma, the circuit must be designed for some narrower range of emitter current to allow for resistor tolerances.

Assuming a bias network using three 5% resistors, then

$I_E^{min} = (1 + 3 \times .05)\ (0.67) = 0.77$ ma and

$I_E^{max} = (1 - 3 \times .05)\ (1.47) = 1.25$ ma

7. Estimate the values of $V_{BE}^{min}$ and $V_{BE}^{max}$

   From Figure 5.1 $V_{BE}^{min}$ at 55°C and $I_E = 1.47$ ma is about 0.08 volt, $V_{BE}^{max}$ at 0°C and $I_E = 0.67$ ma is about 0.17 volt.

8. Calculate the value of $R_B$ from equation (7e).

   $R_B = 4.17\ R_E - 0.78K$

9. Using the equation from (8), choose a suitable value of $R_B$ and $R_E$. This involves a compromise since low values of $R_E$ require a low value of $R_B$ which shunts the input of the stage and reduces the gain. A high value of $R_E$ reduces the collector to emitter bias voltage which limits the peak signal voltage across $R_L$.

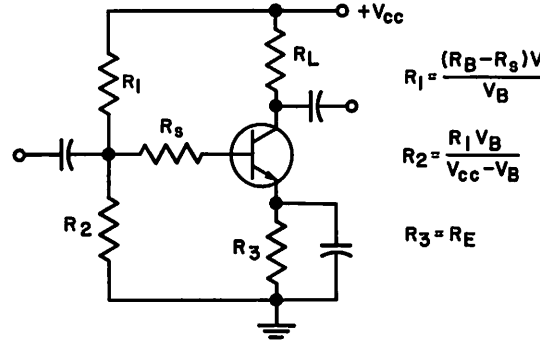
   Choose $R_E = 2.7K$ for which $R_B = 10.4K$. This gives a minimum collector to emitter voltage of $20 - (2.7 + 7.5)\ 1.47 = 5$ volts.

10. Calculate $V_B$ using equation (7c).

    $V_B = 2.56$ volts

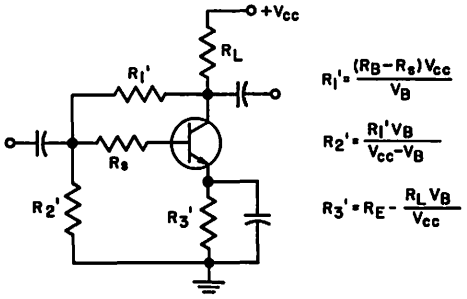
11. If the bias circuits of either Figures 7.5 or 7.6 are to be used, the values of the bias resistors can be calculated from the values of $R_B$, $R_E$ and $V_B$ obtained in the preceding design by the use of the conversion equations which are given. In these figures $R_S$ represents a series resistance which would be present if transformer coupling were used in which case $R_S$ would be the d-c resistance of transformer secondary. In cases where capacitor coupling is used $R_S$ will usually be equal to zero. A comparison of Figures 7.5 and 7.6 indicates that the circuit of Figure 7.6 is superior in that for a given bias stability, it allows a lower value of the emitter resistor or larger values of the base resistors than the circuit of Figure 7.5. On the other hand, the circuit of Figure 7.6 gives a-c feedback through the bias circuits which may be a disadvantage in some cases, as was mentioned earlier in connection with Figure 7.3.

    For the circuit of Figure 7.5, assume $R_S = 0$. Then $R_3 = R_E = 2.7K$, $R_1 = 77K$ or, choosing the next lowest standard value, $R_1 = 68K$. Using this value, calculate $R_2 = 10K$. For the circuit of Figure 7.6 as before $R'_1 = 68K$ and $R'_2 = 10K$. Resistor $R'_3$ is calculated as 1.73K or, using the next highest standard value, $R'_3 = 1.8K$.




**VOLTAGE DIVIDER TYPE BIAS CIRCUIT**

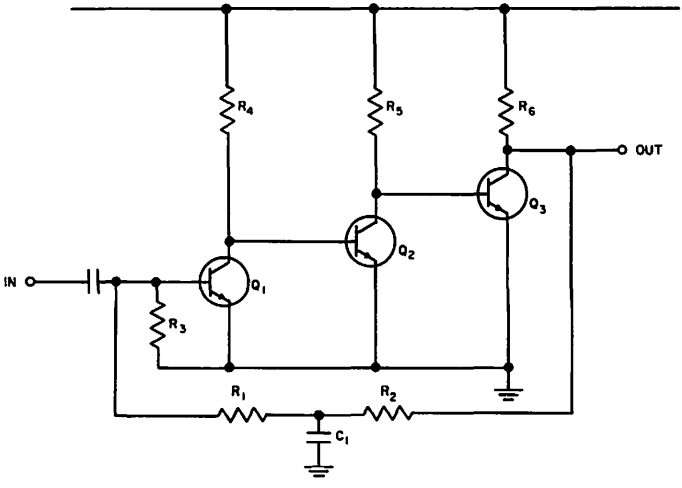
**Figure 7.5**




**VOLTAGE DIVIDER TYPE BIAS CIRCUIT WITH FEEDBACK**

**Figure 7.6**

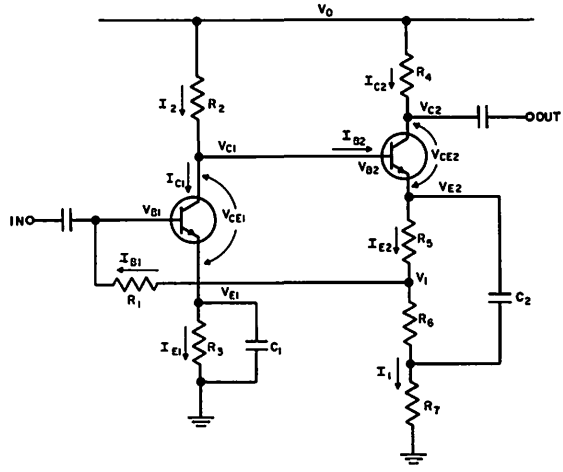
Frequently, in biasing an amplifier, it becomes necessary to use techniques by which higher input impedance or better stability are obtained than afforded by the circuits already shown. Many different schemes have been used to accomplish these purposes and the degree of complexity of any one method depends largely upon the factors listed earlier in this chapter. In any design, however, considerations similar to those in the example shown above must govern the circuit values chosen. Some bias methods used are shown in Figure 7.7 through Figure 7.9. In Figure 7.7 a three stage direct coupled amplifier is shown. The second and third stages of this amplifier are biased by the preceding stages. In the direct coupled amplifier, the stability is improved if all transistors in the amplifier are similar since the changes in bias in adjacent transistors tend to compensate for one another. Further stability is gained in this configuration by the addition of the feedback loop represented by $R_1$, $R_2$, and $C_1$. $C_1$ is added to eliminate a.c. feedback.




**COMMON EMITTER DIRECT COUPLED AMPLIFIER**

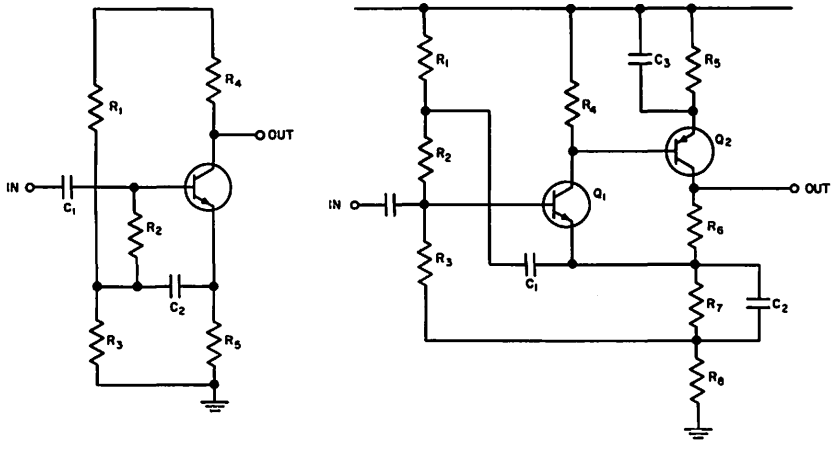
**Figure 7.7**

In Figures 7.8 and 7.9, biasing techniques are used which will improve the input impedance of the amplifier being designed. In Figure 7.8, the a.c. feedback through $R_1$ is essentially eliminated by the existence of $C_2$. $R_1$ can therefore be quite small in order to obtain good temperature stability for the amplifier. In Figure 7.9 bootstrapping techniques are used. Here the a.c. and d.c. feedback are quite large. Temperature stability and input impedance can be optimized but the gain of the circuit is sacrificed for increased input impedance.




**DIRECT COUPLED AMPLIFIER**

**Figure 7.8**




**BOOTSTRAPPED AMPLIFIERS**

**Figure 7.9**

As an example of the biasing considerations for a direct coupled amplifier, the circuit shown in Figure 7.8 is considered. Only d.c. conditions are of interest, therefore resistors $R_6$ and $R_7$ will be considered together and called $R_6$ in the analysis. Node equations can be written for this bias scheme

$$I_2 = I_{C1} + I_{B2} \tag{7f}$$

$$I_{B1} + I_{C1} = I_{E1} \tag{7g}$$

$$I_{B2} + I_{C2} = I_{E2} \tag{7h}$$

$$I_{E2} = I_{B1} + I_1 \tag{7i}$$

Again, these currents are those which one would measure in the lines in which they flow. In addition to these equations, two more equations can be written which depend upon the transistor's action.

$$I_{C1} = h_{FE1} I_{B1} + (h_{FE1} + 1) I_{CO1} \tag{7j}$$

$$I_{C2} = h_{FE2} I_{B2} + (h_{FE2} + 1) I_{CO2} \tag{7k}$$

The relationships between the voltages, resistors, and currents in the circuit are

$$I_2 = \frac{V_0 - V_{C1}}{R_2} \tag{7l}$$

$$I_{B1} = \frac{V_1 - V_{B1}}{R_1} \tag{7m}$$

$$I_{E1} = \frac{V_{E1}}{R_3} \tag{7n}$$

$$I_{C2} = \frac{V_0 - V_{C2}}{R_4} \tag{7o}$$

$$I_{E2} = \frac{V_{E2} - V_1}{R_5} \tag{7p}$$

$$I_1 = \frac{V_1}{R_6} \tag{7q}$$

Substituting these voltage and resistor values into the node equations, and eliminating $I_{C1}$ and $I_{B2}$ by use of the transistor equations (7j) and (7k), the following results

$$\frac{V_0 - V_{C1}}{R_2} = h_{FE1}\left(\frac{V_1 - V_{B1}}{R_1}\right) + (h_{FE1} + 1) I_{CO1} + \frac{V_0 - V_{C2}}{h_{FE2} R_4} - \left(\frac{h_{FE2} + 1}{h_{FE2}}\right) I_{CO2} \tag{7r}$$

$$(1 + h_{FE1})\left(\frac{V_1 - V_{B1}}{R_1} + I_{CO1}\right) = \frac{V_{E1}}{R_3} \tag{7s}$$

$$\left(\frac{V_0 - V_{C2}}{R_4} - I_{CO2}\right)\left(1 + h_{FE2}\right) = h_{FE2}\left(\frac{V_{E2} - V_1}{R_5}\right) \tag{7t}$$

$$\frac{V_{E2} - V_1}{R_5} = \frac{V_1 - V_{B1}}{R_1} + \frac{V_1}{R_6} \tag{7u}$$

To these equations, other transistor voltage relationships can be written

$$V_{E1} + V_{CE1} = V_{C1} \tag{7v}$$

$$V_{E2} + V_{CE2} = V_{C2} \tag{7w}$$

$$V_{E1} + V_{BE1} = V_{B1} \tag{7x}$$

$$V_{E2} + V_{BE2} = V_{B2} = V_{C1} \tag{7y}$$

There are now eight independent equations (7r) through (7y), relating the voltage and resistance values of the circuit. The circuit requirements of the particular design now govern the remainder of the design procedure. All of the above equations are true at all temperature extremes. The stability problem arises since the values of $I_{CO}$ and $h_{FE}$ change as a function of temperature. As these values change, the voltage and

current relationships within the circuit must also change so that equations (7r) through (7y) are satisfied. In practical design, for example, the specifications for the amplifier normally demand that the output be capable of a specific voltage excursion. This peak to peak allowable swing at the collector of the output transistor can theoretically equal the supply voltage, if the bias voltage, $V_{C2}$, is exactly $V_0/2$. Maintaining $V_{C2}$ exactly over the range of $h_{FE}$ and $I_{CO}$ is essentially impossible, and thus the output voltage excursion must be somewhat less than the supply voltage so that limiting does not occur on the output waveform as the bias level changes. At the lowest temeperature of interest, the emitter currents will be a minimum and the worst conditions would occur for $h_{FE} = h_{FE}^{min}$, $V_{BE}^{max}$, and $I_{CO} = 0$. At high temperature, the emitter currents will have a maximum value, and the worst case is encountered for $h_{FE} = h_{FE}^{max}$, $V_{BE} = V_{BE}^{min}$, and $I_{CO} = I_{CO}.^{max}$

The choosing of resistor values throughout the circuit is normally accomplished by considering circuit requirements in conjunction with transistor operating conditions. Equations (7f) through (7q) may also be of value in selecting resistors. A perfectly general biasing scheme is difficult to describe since individual circuit requirements play an important role in every amplifier. Some considerations are mentioned earlier in this chapter and also in Chapter 14. A general method of checking the values of resistance chosen could be worked out by solving equations (7r) through (7y) for $V_{C2}$ by eliminating all voltages except $V_0$, $V_{BE1}$, and $V_{BE2}$. The resulting equation will be of the form

$$V_{C2} = \frac{K_1 V_0 + K_2 V_{BE1} + K_3 V_{BE2} + K_4 I_{CO1} + K_5 I_{CO2}}{K_6} \tag{7z}$$

If no approximations are made, these constants can be quite lengthy. For the case of Figure 7.18 the constants are

$$K_1 = \frac{(1 + h_{FE2}) R_6}{R_4}\left[R_3\left(1 + \frac{R_A}{R_6}\right) + R_A + h_{FE1} R_2\right] - R_A\left(h_{FE2} - \frac{R_2}{R_4}\right) \tag{7aa}$$

$$K_2 = -h_{FE2}(h_{FE1} R_2 - R_6) \tag{7bb}$$

$$K_3 = h_{FE2} R_A \tag{7cc}$$

$$K_4 = h_{FE2}(1 + h_{FE1})(R_B + R_1 R_2) \tag{7dd}$$

$$K_5 = -(1 + h_{FE2})\left[(1 + h_{FE1})(R_3 R_5 + R_B) + (R_1 R_2 + R_C)\right] \tag{7ee}$$

$$K_6 = \frac{(1 + h_{FE2}) R_6}{R_4}\left[R_3\left(1 + \frac{R_A}{R_6}\right) + R_A + h_{FE1} R_2\right] + \frac{(R_A + R_6) R_2}{R_4} \tag{7ff}$$

where,

$$R_A = R_1 + (1 + h_{FE1}) R_3 \tag{7gg}$$

$$R_B = R_2 R_3 + R_2 R_6 + R_3 R_6 \tag{7hh}$$

$$R_C = R_1 R_5 + R_1 R_6 + R_5 R_6 \tag{7ii}$$

By calculating the value of $V_{C2}$ using the worst case values for $h_{FE}$, $V_{BE}$, and $I_{CO}$ at the temperature extremes the variation in $V_{C2}$ with temperature can be checked. Though this procedure is tedious, one is able to determine the stability of any given amplifier using steps similar to those outlined for the circuit of Figure 7.18.

Because of the circuit configuration used in this example, other types of bias schemes can also be analyzed by setting some of the resistor values at zero. Two different bias schemes would call for the following resistor changes: $R_5 = 0$; or $R_6 = 0$, and $R_1$ represents resistance seen at the base by the first transistor.

## THERMAL RUNAWAY

When a transistor is used at high junction temperatures (high ambient temperatures and/or high power dissipation) it is possible for regenerative heating to occur which will result in thermal run-away and possible destruction of the transistor. In any circuit the junction temperature ($T_J$) is determined by the total power dissipation in the transistor (P), the ambient temperature ($T_A$), and the thermal resistance (K).

$$T_J = T_A + KP \tag{7jj}$$

If the ambient temperature is increased, the junction temperature would increase an equal amount provided that the power dissipation was constant. However, since both $h_{FE}$ and $I_{CO}$ increase with temperature, the collector current can increase with increasing temperature which in turn can result in increased power dissipation. Thermal run-away will occur when the rate of increase of junction temperature with respect to the power dissipation is greater than the thermal resistance ($\Delta T_J/\Delta P > K$).

Thermal run-away is generally to be avoided since it can result in failure of the circuit and possibly in destruction of the transistor. By suitable circuit design it is possible to ensure either that the transistor can not run away under any conditions or that the transistor can not run away below some specified ambient temperature. A different circuit analysis is required depending on whether the transistor is used in a linear amplifier or in a switching circuit.

In switching circuits such as those described in Chapter 6, it is common to operate the transistor either in saturation (low collector to emitter voltage) or in cutoff (base to emitter reverse biased). The dissipation of a transistor in saturation does not change appreciably with temperature and therefore run-away conditions are not possible. On the other hand, the dissipation of a transistor in cutoff depends on $I_{CO}$ and therefore can increase rapidly at higher temperatures. If the circuit is designed to ensure that the emitter to base junction is reverse biased at all temperatures (as for the circuit of Figure 7.10) the following analysis can be used:

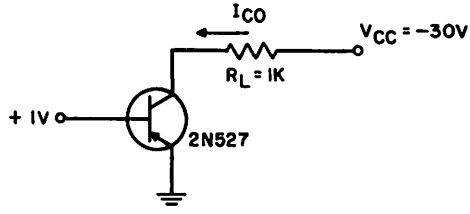



**Figure 7.10**

The transistor power dissipation will be,

$$P = I_{CO}V_{CE} = I_{CO}(V_{CC} - I_{CO}R_L) = I_{CO}\,V_{CC} - I_{CO}^2\,R_L \tag{7kk}$$

The rate of change of power dissipation with temperature will be,

$$\frac{dP}{dT} = \frac{dP}{dI_{CO}} \cdot \frac{dI_{CO}}{dT} = (V_{CC} - 2I_{CO}R_L)\,\delta I_{CO} \tag{7ll}$$

where $\delta \cong 0.08$ is the fractional increase in $I_{CO}$ with temperature. The condition for run-away occurs when $dP/dT = 1/K$ or,

$$(V_{CC} - 2I_{COM}R_L)\,\delta I_{COM} = 1/K \tag{7mm}$$

where $I_{COM}$ is the value of $I_{CO}$ at the run-away point. Solving for $I_{COM}$ gives,

$$I_{COM} = \frac{V_{CC} \pm \sqrt{(V_{CC})^2 - (8R_L)/(\delta K)}}{4R_L} \tag{7nn}$$

In this equation the solution using the negative sign gives the value of $I_{COM}$, while the solution using the positive sign gives the value of $I_{CO}$ after run-away has occurred. It is seen from the equation that the value of $I_{CO}$ after run-away can never be greater than $V_{CC}/2R_L$ so that the collector voltage after run-away can never be less than one half of the supply voltage $V_{CC}$. If the term under the square root sign in the above equation is zero or negative, thermal run-away cannot occur under any conditions. Also, if thermal run-away does occur it must occur when the collector voltage is greater than $0.75V_{CC}$. since when the term under the square root sign is zero, $I_{COM}$ $R_L$ equals .25 $V_{CC}$. As $R_L$ goes to 0, the solution for $I_{COM}$ using the negative sign is indeterminant, i.e., equal to 0/0. In this case Equation (7mm) is used and

$$I_{COM} = \frac{1}{\delta K V_{CC}} \tag{7oo}$$

Since no $R_L$ exists, the current after thermal runaway is theoretically infinite, and the transistor will be destroyed unless some other current limiting is provided. Once the value of $I_{COM}$ is determined from Equation (7nn) or (7oo) the corresponding junction temperature can be determined from a graph such as Figure 6.6. The heating due to $I_{COM}$ is found by substituting $I_{COM}$ for $I_{CO}$ in Equation (7kk). Finally, the ambient temperature at which run-away occurs can be calculated from Equation (7jj).

In circuits which have appreciable resistance in the base circuit such as the circuit of Figure 7.11 the base to emitter junction will be reverse biased only over a limited temperature range. When the temperature is increased to the point where the base to emitter junction ceases to be reverse biased emitter current will flow and the dissipation will increase rapidly. The solution for this case is given by:

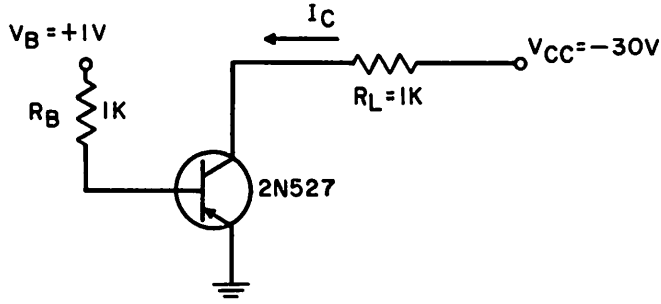



**Figure 7.11**

$$I_{COM} = \frac{(V_{CC} - 2R_L h_{fe} I_x) \pm \sqrt{(V_{CC} - 2R_L h_{fe} I_x)^2 - (8R_L)/(\delta K)}}{4R_L h_{fe}} \tag{7pp}$$

where $I_x = V_B/R_B$. When $R_L$ approaches 0.

$$I_{COM} = \frac{1}{h_{FE}\, \delta\, K\, V_{CC}} \tag{7qq}$$

In the analysis of run-away in linear amplifiers it is convenient to classify linear amplifiers into preamplifiers and power amplifiers. Preamplifiers are operated at low signal levels and consequently the bias voltage and current are very low particularly in stages where good noise performance is important. In capacitor coupled stages a large collector resistance is used to increase gain and a large emitter resistance is used to improve bias stability. Accordingly, thermal run-away conditions are seldom met in preamplifier circuits.

In contrast, power amplifiers invariably require transistors to operate at power levels which are near the run-away condition. The conditions are aggravated by the use of biasing networks of marginal stability which are required for power efficiency and by the use of transformer coupling to the load which reduces the effective collector series resistance. Since thermal run-away in power stages is likely to result in destruction of the transistors, it is wise to use worst case design principles to ensure that thermal run-away cannot occur. The worst case conditions are with $h_{fe} \rightarrow \infty$, $V_{BE} = 0$, $R_L = 0$, and $I_{CO} = I_{CO}^{max}$. If these conditions are applied to a transistor in the general bias circuit shown in Figure 7.12 the total transistor dissipation is given by:

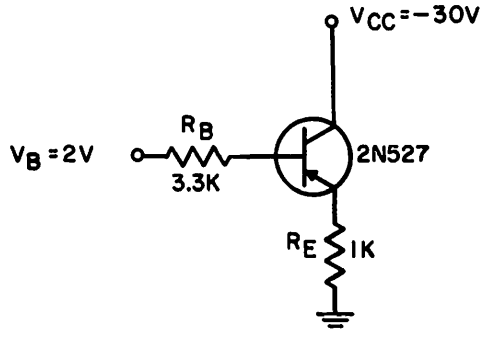



**Figure 7.12**

$$P = V_{CE}I_C = (V_{CC} - V_B - I_{CO}R_B)\left(I_{CO} + \frac{V_B + I_{CO}R_B}{R_E}\right) \qquad (7rr)$$

Equating dP/dT with 1/K and solving for $I_{COM}$ as before,

$$I_{COM} = \frac{(V_{CC} - R_1V_B) \pm \sqrt{(V_{CC} - R_1V_B)^2 - (R_2)/(\delta K)}}{4R_B} \qquad (7ss)$$

where

$$R_1 = \frac{R_E + 2R_B}{R_E + R_B} \qquad R_2 = \frac{8R_ER_B}{R_E + R_B}$$

As before, the solution of Equation (7ss) using the negative sign gives the value of $I_{COM}$, while the solution using the positive sign gives the final value of $I_C$ after run-away has occurred. If the quantity under the square root sign is zero or negative, run-away cannot occur under any conditions.

In class-B power amplifiers the maximum transistor power dissipation occurs when the power output is at 40% of its maximum value at which point the power dissipation in each transistor is 20% of the maximum power output. In class-A power amplifiers on the other hand, the maximum transistor dissipation occurs when there is no applied signal. The maximum power dissipation is obtained by substituting $I_{COM}$ in Equation (7rr) and the maximum junction temperature is obtained from Equation (7jj).

In the design of power amplifiers the usual procedure is to design the circuit to meet the requirements for gain, power output, distortion, and bias stability as described in the other sections of this manual. The circuit is then analyzed to determine the conditions under which run-away can occur to determine if these conditions meet the operating requirements. As a practical example, consider the analysis of the class-A output stage of the receiver shown in Figure 10.12. The transistor is the 2N241A for

which K = 250°C/watt and $I_{co}^{max}$ = 16$\mu$a at 25°C and 25 volts. Calculating the circuit values corresponding to Figure 7.12 and Equation (7ss):

$$V_{cc} = 9\text{ v}, \quad R_E = 100\ \Omega$$

$$V_B = \frac{(1000)(9)}{1000 + 4700} = 1.58\text{ v} \qquad R_B = \frac{(1000)(4700)}{1000 + 4700} = 825\ \Omega$$

$$R_1 = \frac{100 + 2(825)}{100 + 825} = 1.89 \qquad R_2 = \frac{8(100)(825)}{100 + 825} = 713\ \Omega$$

Calculating $I_{COM}$ from Equation (7ss)

$$I_{COM} = \frac{6 \pm \sqrt{0.47}}{3300} = 1.61\text{ ma or } 2.02\text{ ma}$$

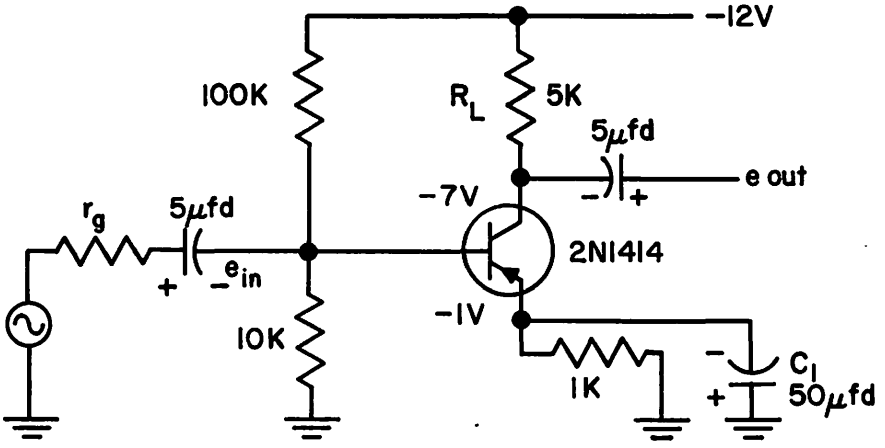
Since the quantity under the square root is positive, thermal run-away can occur. The two solutions give the value of $I_{COM}$ (1.61 ma) and the value of $I_{co}$ after run-away has occurred (2.02 ma). The fact that these two currents are very nearly equal indicates that the change in power dissipation when run-away occurs will not be very large. Using the value $I_{COM}/I_{co}^{max}$ = 100 the junction temperature at run-away from Figure 6.6(A) is about 92°C. The dissipation at run-away, calculated from Equation (7rr), is about 187 milliwatts. The rise in junction temperature due to this power dissipation is (0.25) (187) = 46.7°C. The ambient temperature at run-away is then calculated to be 92 — 46.7 = 45.3°C. The above value of maximum transistor power dissipation is calculated under the assumption that the series collector resistance is zero. In the circuit under consideration the transformer primary will have a small d-c resistance ($R_T$) which will reduce the transistor power dissipation by approximately $(I_C)^2R_T$ where $I_C$ is given by the second term in Equation (7rr). Assuming that the d-c resistance of the transformer is 20 ohms the reduction in power dissipation for the case just considered will be 18.8 milliwatts and the ambient temperature at run-away will be increased to 50.0°C.

# AUDIO AMPLIFIERS

CHAPTER 8

## SINGLE STAGE AUDIO AMPLIFIER

Figure 8.1 shows a typical single stage audio amplifier using a 2N1414 PNP transistor.




SINGLE STAGE AUDIO AMPLIFIER

**Figure 8.1**

With the resistance values shown, the bias conditions on the transistor are 1 ma of collector current and six volts from collector to emitter. At frequencies at which $C_1$ provides good by-passing, the input resistance is given by the formula: $R_{in} = (1 + h_{fe})\, h_{ib}$. At 1 ma for a design center 2N1414, the input resistance would be $45 \times 29$ or about 1300 ohms.

The a-c voltage gain $\frac{e_{out}}{e_{in}}$ is approximately equal to $\frac{R_L}{h_{ib}}$ For the circuit shown, this would be $\frac{5000}{29}$ or approximately 172.

The frequency at which the voltage gain is down 3 db from the 1 Kc value depends on $r_g$. This frequency is given approximately by the formula

$$\text{low } f_{3db} \approx \frac{1 + h_{fe}}{6.28\,(r_g C_1)}$$

## TWO STAGE R-C COUPLED AMPLIFIER

The circuit of a two stage R-C coupled amplifier is shown by Figure 8.2. The input impedance is the same as the single stage amplifier and would be approximately 1300 ohms.

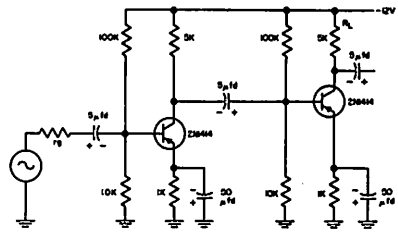


Figure 8.2

The load resistance for the first stage is now the input impedance of the second stage. The voltage gain is given approximately by the formula

$$A_V \approx h_{fe} \frac{R_L}{h_{ib}}$$

More exact formulas for the performance of audio amplifiers may be found in Chapter 4 on small signal characteristics.

## CLASS B PUSH-PULL OUTPUT STAGES

In the majority of applications, the output power is specified so a design will usually begin at this point. The circuit of a typical push-pull Class B output stage is shown in Figure 8.3.

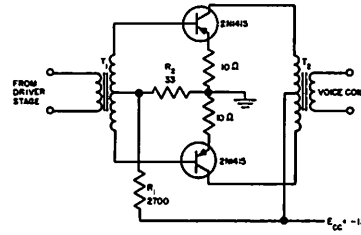



Figure 8.3

The voltage divider consisting of R1 and R2 gives a slight forward bias of about .14 volts on the transistors to prevent cross-over distortion. The 10 ohm resistors in the emitter leads stabilize the transistors so they will not go into thermal runaway when the ambient temperature is less than 55°C. Typical collector characteristics with a load line are shown below

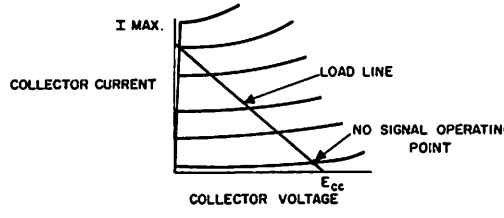



Figure 8.4

It can be shown that the maximum a-c output power without clipping using a push-pull stage is given by the formula

$$P_{out} = \frac{I_{max} \quad V_{CE}}{2}$$ where $V_{CE}$ = collector to emitter voltage at no signal.

Since the load resistance is equal to $R_L = \frac{V_{CE}}{I_{max}}$

and the collector to collector impedance is four times the load resistance per collector, the output power is given by the formula

$$P_o = -\frac{2\,V_{CE}^2}{R_{c\text{-}c}} \tag{8a}$$

Thus, for a specified output power and collector voltage the collector to collector load resistance can be determined. For output powers in the order of 50 mw to 850 mw, the load impedance is so low that it is essentially a short circuit compared to the output impedance of the transistors. Thus, unlike small signal amplifiers, no attempt is made to match the output impedance of transistors in power output stages.
The power gain is given by the formula:

$$\text{Power Gain} = \frac{P_{out}}{P_{in}} = \frac{I_o^2 \quad R_L}{I_{in}^2 \quad R_{in}}$$

Since $\frac{I_o}{I_{in}}$ is equal to the current gain, Beta, for small load resistance, the power gain formula can be written as

$$P.G. = \beta^2 \frac{R_{c\text{-}c}}{R_{b\text{-}b}} \tag{8b}$$

where $R_{c\text{-}c}$ = collector to collector load resistance.
$R_{b\text{-}b}$ = base to base input resistance.
$\beta$ = grounded emitter current gain.

Since the load resistance is determined by the required maximum undistorted output power, the power gain can be written in terms of the maximum output power by combining equations (8a) and (8b) to give

$$P.G. = \frac{2\beta^2\,V_{CE}^2}{R_{b\text{-}b}\,P_{out}} \tag{8c}$$

## CLASS A OUTPUT STAGES

A Class A output stage is biased as shown on the collector characteristics below

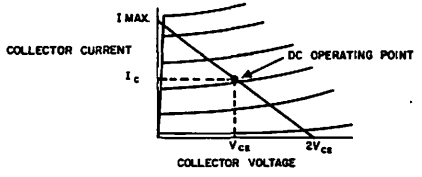



**Figure 8.5**

The operating point is chosen so that the output signal can swing equally in the positive and negative direction. The maximum output power without clipping is equal to

$$P_{out} = \frac{V_{CE} \quad I_c}{2}$$

The load resistance is then given by the formula

$$R_L = \frac{V_{CE}}{I_c}$$

Combining these two equations, the load resistance can be expressed in terms of the collector voltage and power output by the formula below

$$R_L = \frac{V_{CE}^2}{2\,P_o} \tag{8d}$$

For output powers of 20 mw and above, the load resistance is very small compared to the transistor output impedance and the current gain of the transistor is essentially the short circuit current gain Beta. Thus for a Class A output stage the power gain is given by the formula

$$P.G. = \frac{\beta^2 R_L}{R_{in}} = \frac{\beta^2 V_{CE}^2}{2\,R_{in}\,P_o} \tag{8e}$$

## CLASS A DRIVER STAGES

For a required output power of 400 mw, the typical gain for a 12 volt push-pull output stage would be in the order of 27 db. Thus the input power to the output stage would be about 1 to 2 mw. The load resistance of a Class A driver stage is then determined by the power that must be furnished to the output stage and this load resistance is given by equation (8d). For output powers in the order of a few milliwatts, the load resistance is not negligible in comparison to the output impedance of the transistors, therefore, more exact equations must be used to determine the power gain of a Class A driver stage. From four-terminal network theory, after making appropriate approximations, it can be shown that the voltage gain is given by the formula

$$A_V = \frac{R_L}{h_{ib} + Z_e} \tag{8f}$$

where $h_{ib}$ = grounded base input impedance.

$Z_e$ = external circuit impedance in series with emitter.

The current gain is given by the formula

$$A_I = \frac{\alpha}{1 - \alpha + R_L\,h_{ob}} \tag{8g}$$

where $h_{ob}$ = grounded base output conductance.

The power gain is the product of the current gain and the voltage gain, thus unlike the formula for high power output stages, there is no simple relationship between required output power and power gain for a Class A driver amplifier.

## DESIGN CHARTS

Figures 8.6 through 8.15 are design charts for determination of transformer impedances and typical power gains for Class A driver stages, Class A output stages, and Class B push-pull stages. The transformer-power output charts take into account a transformer efficiency of 75% and therefore may be read directly in terms of power delivered to the loudspeaker. Power gain charts show the ratio of output power in the collector circuit to input power in the base circuit and therefore do not include transformer losses. Since the output transformer loss is included in the one chart and the design procedure used below includes the driver transformer loss, it can be seen that the major losses are accounted for.

The charts can best be understood by working through a typical example. Assume a 300 mw output is desired from a 12v amplifier consisting of a driver and push-pull output pair. Also the signal source has an available power output of 30 mμw

($30 \times 10^{-9}$ watts). Overall power gain required then is

$$\text{P.G.} = \frac{P_{out}}{P_{in}} = \frac{300 \text{ mw}}{30 \text{ m}\mu\text{w}} = \frac{300 \times 10^{-3}}{30 \times 10^{-9}} = 10 \times 10^{6}$$

or 70 db.

To obtain 300 mw in the loudspeaker, the output pair must develop 300 mw plus the transformer loss.

$$P_{\text{collector to collector}} = \frac{P_{out}}{\text{transformer eff.}} = \frac{300 \text{ mw}}{.75} = 400 \text{ mw}$$

From Figure 8.11, a pair of 2N1415's in Class B push-pull has a power gain of approximately 28 db at 400 mw. This is a numerical gain of 650 so the input power required by the output stage is

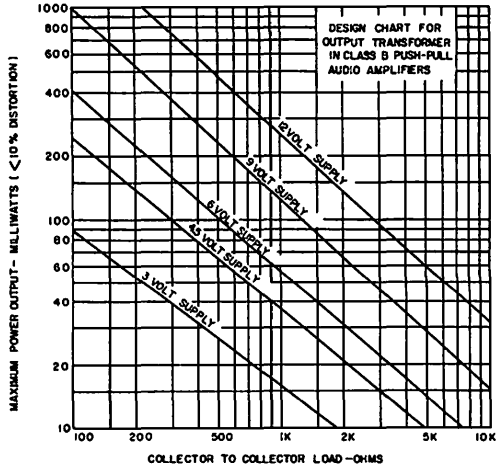
$$P_{in} = \frac{P_{out}}{\text{Gain}} = \frac{400 \text{ mw}}{650} = .62 \text{ mw}$$

If the driver transformer is 75% efficient, the driver must produce

$$P_{driver} = \frac{\text{P into output stage}}{75\%} = \frac{.62 \text{ mw}}{.75} = .82 \text{ mw}$$

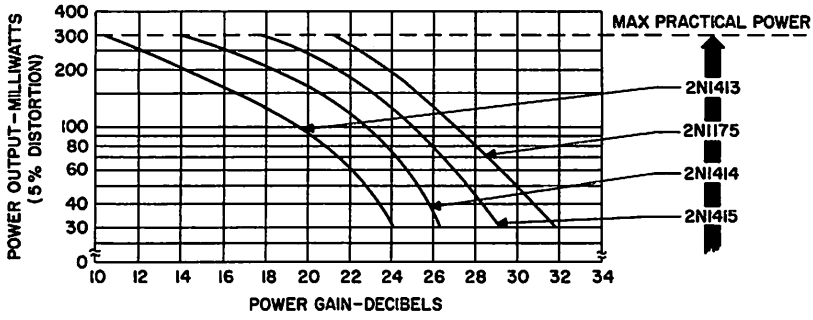
The remaining power gain to be obtained from the driver is 70 db — 28 db = 42 db. From Figure 8.15 the 2N322 has a power gain of 42.5 db at a power output of .82 mw.

The output transformer primary impedance is obtained from Figure 8.6 on the 12 volt supply line at 400 mw output, and is 600 ohms maximum collector to collector load resistance. Therefore a more standard 500 ohm CT output transformer may be used with secondary impedance to match the load. From Figure 8.12 the driver transformer primary impedance is 40,000 ohms, but as low as a 20,000 ohm transformer can be used and still have 42 db gain. The secondary must be center-tapped with a total impedance of 800 to 5000 ohms. When this procedure is used for commercial designs, it must be remembered that it represents full battery voltage, typical power gain and input impedance, and therefore does not account for end-limit points. Figure 8.17 is a circuit that uses the above design calculations.



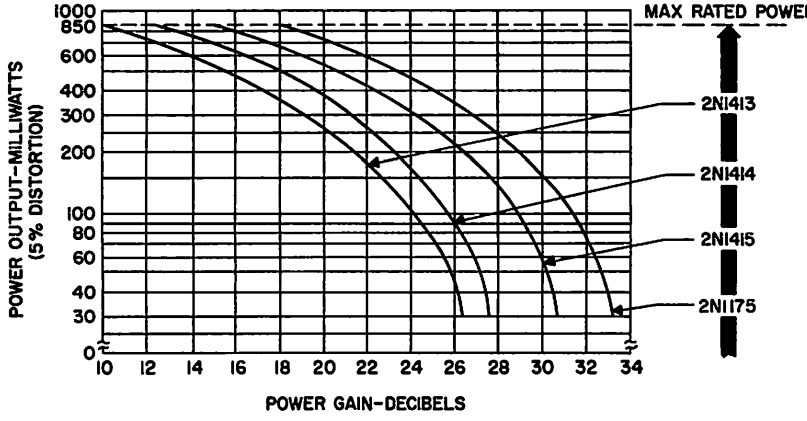

**DESIGN CHART FOR OUTPUT TRANSFORMER IN CLASS B PUSH-PULL AUDIO AMPLIFIERS**

**Figure 8.6**



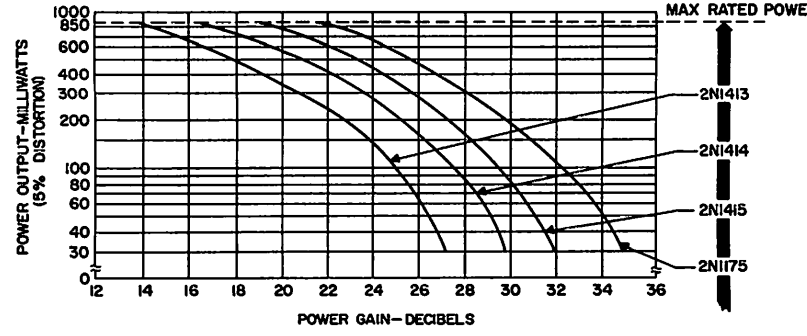

**TYPICAL POWER GAIN FOR CLASS B PUSH-PULL AMPLIFIERS, 3.0 VOLT SUPPLY**

**Figure 8.7**



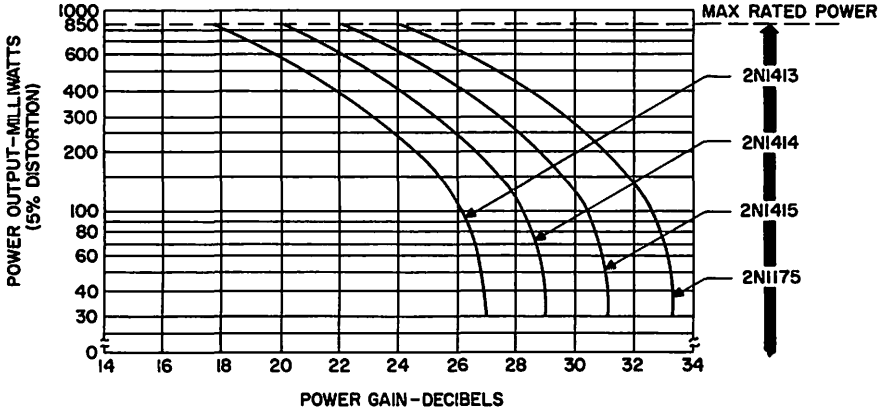

**TYPICAL POWER GAIN FOR CLASS B PUSH-PULL AMPLIFIERS, 4.5 VOLT SUPPLY**

**Figure 8.8**



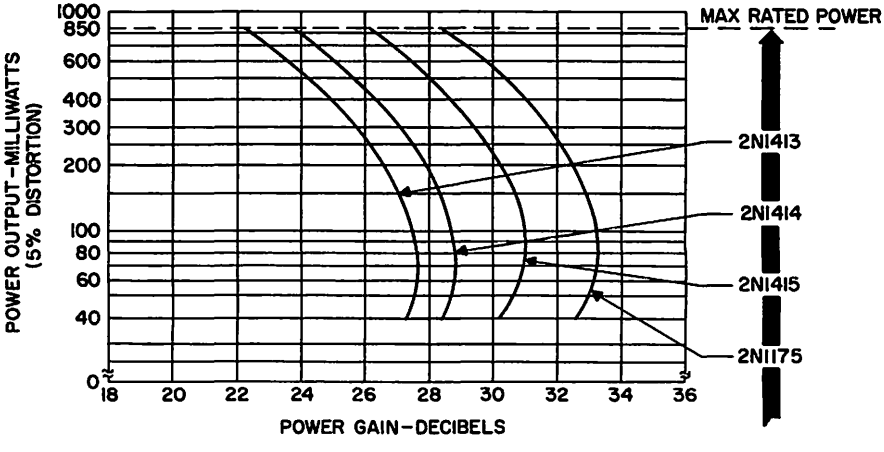

**TYPICAL POWER GAIN FOR CLASS B PUSH-PULL AMPLIFIERS, 6 VOLT SUPPLY**

**Figure 8.9**



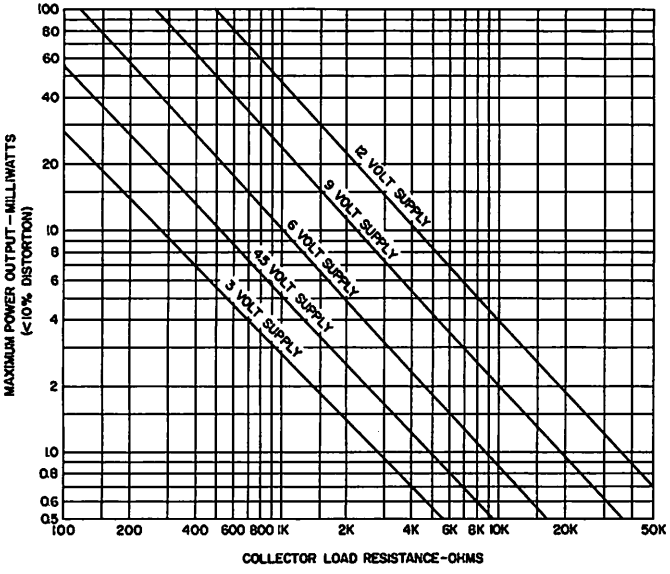

**TYPICAL POWER GAIN FOR CLASS B PUSH-PULL AMPLIFIERS, 9 VOLT SUPPLY**

**Figure 8.10**



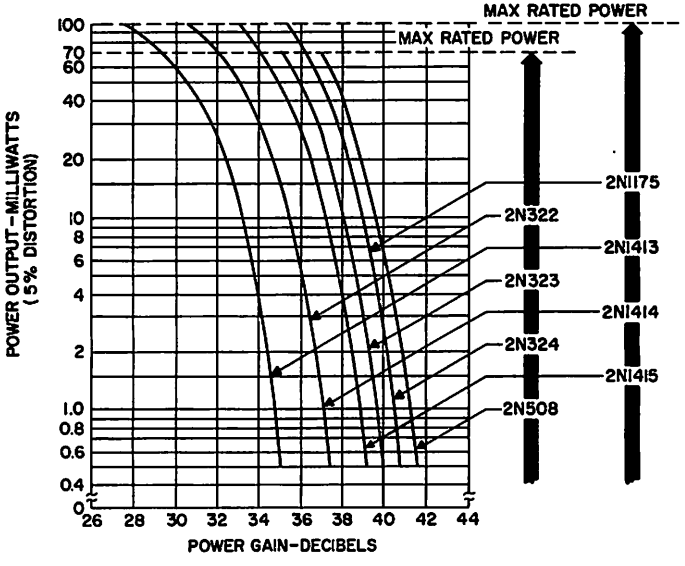

**TYPICAL POWER GAIN FOR CLASS B PUSH-PULL AMPLIFIERS, 12 VOLT SUPPLY**

**Figure 8.11**



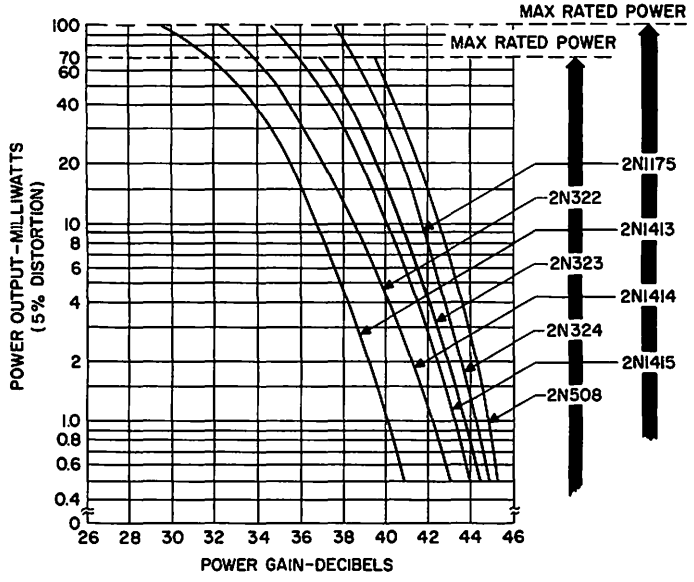

**DESIGN CHART FOR OUTPUT TRANSFORMER IN CLASS A SINGLE-ENDED AMPLIFIER**

**Figure 8.12**



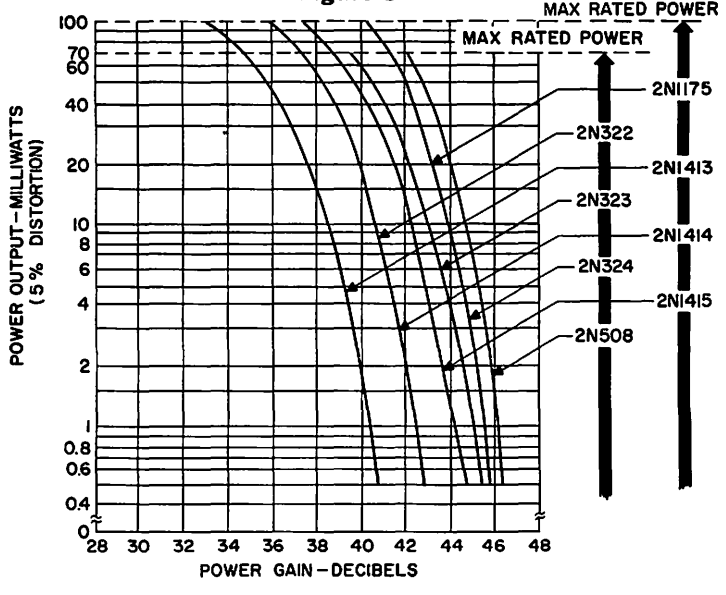

**TYPICAL POWER GAIN FOR CLASS A SINGLE-ENDED AMPLIFIERS, 6 VOLT SUPPLY**

**Figure 8.13**




**TYPICAL POWER GAIN FOR CLASS A SINGLE-ENDED AMPLIFIERS, 9 VOLT SUPPLY**

**Figure 8.14**




**TYPICAL POWER GAIN FOR CLASS A SINGLE-ENDED AMPLIFIERS, 12 VOLT SUPPLY**

**Figure 8.15**

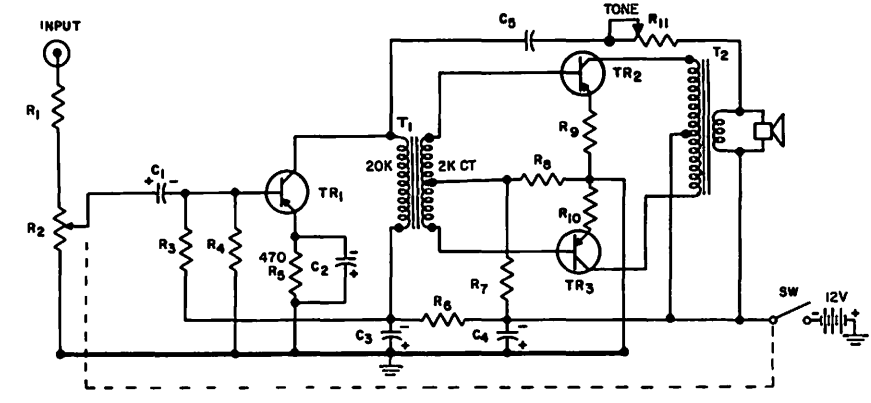
TRANSISTORS LISTED IN THE TOP ROW ARE PREFERRED TYPES AND SHOULD BE USED IN ALL NEW DESIGNS. THEY CAN BE SUBSTITUTED FOR TYPES LISTED BELOW THEM IN THE SAME COLUMN.

| * 2N322 | * 2N323 | * 2N324 | * 2N508 | 2N1413 | 2N1414 | 2N1415 | 2N1175 |
|---|---|---|---|---|---|---|---|
| 2N190 | 2N191 | 2N192 | 2N265 | 2N187A<br>2N189<br>2N319 | 2N188A<br>2N190<br>2N320<br>2N322 | 2N241A<br>2N191<br>2N321<br>2N323 | 2N192<br>2N324 |

* THESE TYPES CAN NOT BE SUBSTITUTED IF APPLICATION REQUIRES $V_{CER} > 16$ VOLTS

PREFERRED TYPES AND SUBSTITUTION CHART

**Figure 8.16**




$R_1$ —— 220,000 OHM
$R_2$ —— VOLUME CONTROL 10,000 OHM 1/2 W AUDIO TAPER
$R_3$ —— 190,000 OHM
$R_4$ —— 10,000 OHM
$R_5$ —— 470 OHM
$R_6$ —— 220 OHM
$R_7$ —— 2700 OHM
$R_8$ —— 33 OHM
$R_9$, $R_{10}$ —— 10 OHM
$R_{11}$ —— 25K LINEAR

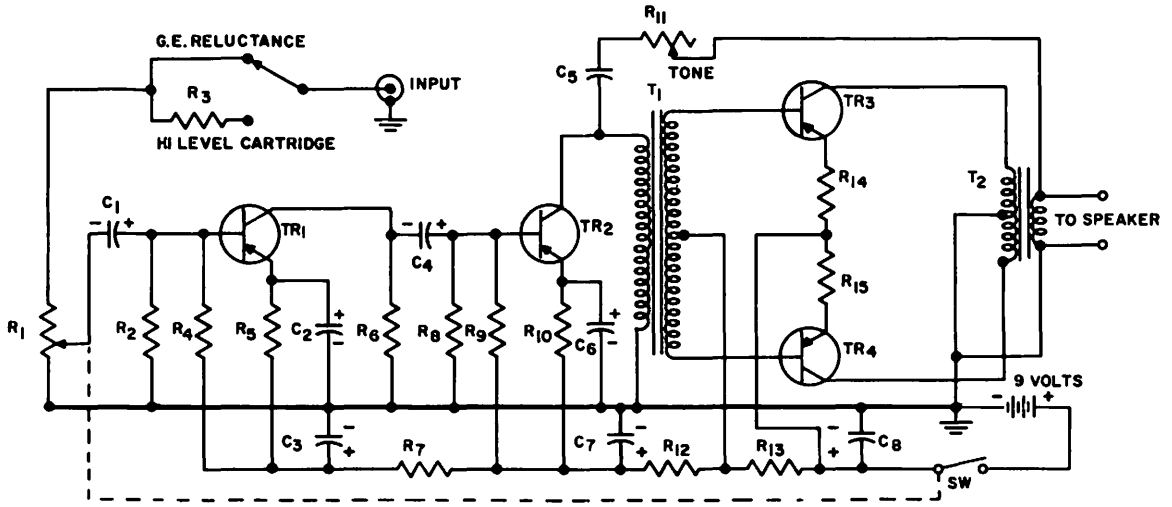
$C_1$ —— 6 μfd, 12V
$C_2$ —— 100 μfd, 3V
$C_3$, $C_4$ —— 50 μfd, 12V
$C_5$ —— .01 μfd
$TR_1$ —— GE. 2N322
$TR_2$, $TR_3$ —— GE. 2N415
$T_1$ —— 20K/2K CT
$T_2$ —— 500 Ω CT/ V.C.

MAXIMUM POWER OUT AT 10% HARMONIC DISTORTION—300 MW
FOR USE WITH MAGNETIC CARTRIDGE OMIT $R_1$

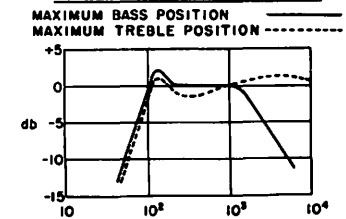
ALL RESISTORS 1/2 W

12 VOLT PHONO AMPLIFIER

**Figure 8.17**




FREQUENCY RESPONSE
OF FOUR TRANSISTOR AMPLIFIER



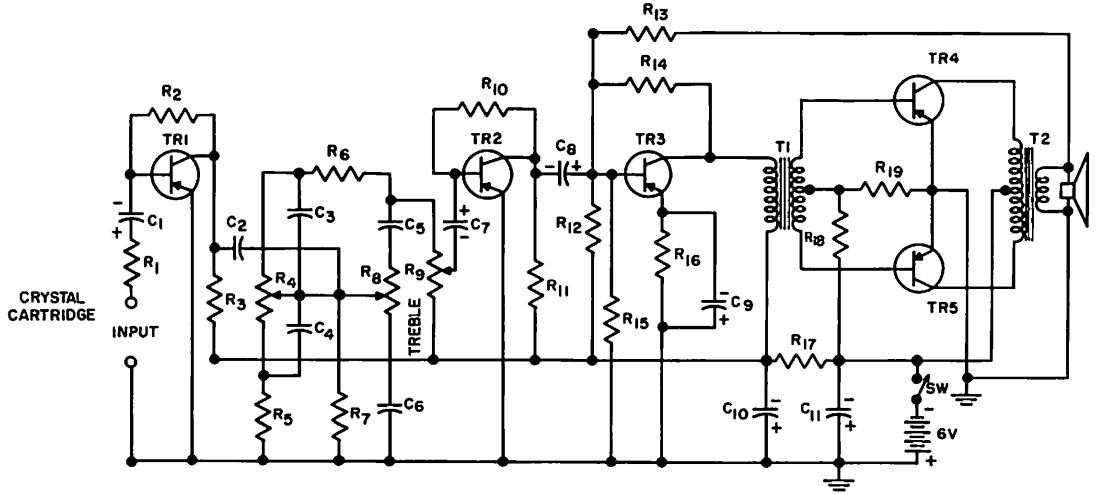

AMPLIFIER LOADED WITH 3.2 Ω VOICE COIL SPEAKER RESONANCE @ 130 CPS

$R_1$ — 5000 OHM VOLUME CONTROL 1/2 W AUDIO TAPER
$R_2$ — 150,000 OHM
$R_3$ — 470,000 OHM
$R_4$ — 10,000 OHM
$R_6, R_9$ — 4700 OHM
$R_7$ — 1000 OHM
$R_8$ — 33,000 OHM
$R_{11}$ — 25,000 OHM LINEAR
$R_{12}$ — 220 OHM
$R_5, R_{10}$ — 470 OHM
$R_{13}$ — 47 OHM
$R_{14}, R_{15}$ — 8.2 OHM
$C_1, C_3, C_7, C_8$ — 50μfd, 12V
$C_2, C_6$ — 50μfd, 3V
$C_4$ — 15μfd, 12V
$C_5$ — .02μfd
$TR_1, TR_2$ — G.E. 2N323
$TR_3, TR_4$ — G.E 2N1415
$T_1$ — 5K/3K CT
$T_2$ — 200Ω C.T./V.C.

MAXIMUM POWER OUT AT 10% HARMONIC DISTORTION — 400 MW
DISTORTION AT 100 MILLIWATTS
AT 100 C/S — 5%
AT 1000 C/S — 2%
AT 5000 C/S — 5%

ALL RESISTORS 1/2 W

**9 VOLT PHONO AMPLIFIER**
**Figure 8.18**




**6 VOLT PHONO AMPLIFIER**

**Figure 8.19**

# HIGH FIDELITY CIRCUITS

CHAPTER 9

Transistors are ideally suited for high fidelity amplifiers since there is no problem with microphonics or hum pick-up from filaments as there is with tubes. Transistors are inherently low impedance devices and thus offer better matching to magnetic pick-ups and loudspeakers for more efficient power transfer.

Transistor circuits with negative feedback can give the wide frequency response and low distortion required for high fidelity equipment. In general, the distortion reduction is about equal to the gain reduction for the circuit to which negative feedback is applied. The input and output impedances of amplifiers with feedback are either increased or decreased, depending on the form of feedback used. Voltage feedback, over one or several transistor stages, from the collector decreases the output impedance of that stage; whereas current feedback from the emitter increases the output impedance of that stage. If either of these networks are fed back to a transistor base the input impedance is decreased, but if the feedback is to the emitter then the impedance is increased. The feedback can be applied to the emitter for effective operation with a low generator impedance, whereas the feedback to the base is effective with a high impedance (constant current) source. If the source impedance was low in the latter case then most of the feedback current would flow into the source and not into the feedback amplifier. The feedback connections must be chosen to give a feedback signal that is out-of-phase with the input signal if applied to the base, or in-phase if it is applied to the emitter of a common emitter stage.

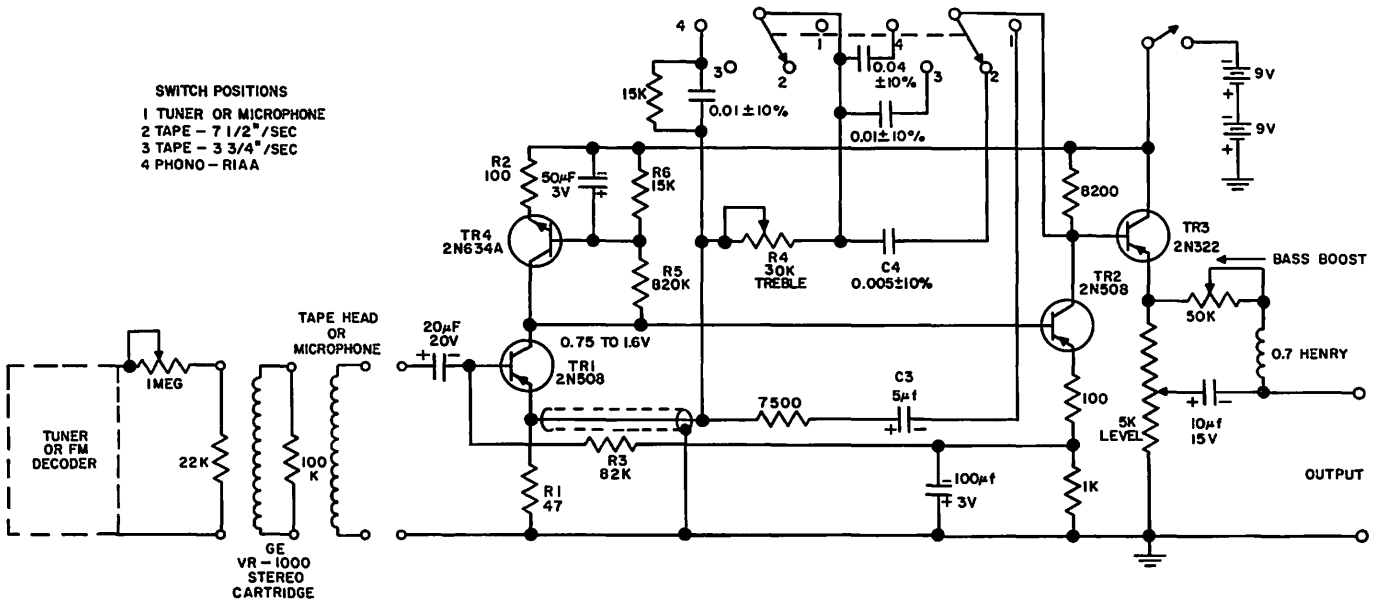
Care must be used in applying feedback around more than two transistor stages to prevent high frequency instability. This instability results when the phase shift through the transistor amplifiers is sufficient to change the feedback from negative to positive. The frequency response of the feedback loop is sometimes limited to stabilize the circuit. At the present time, the amount of feedback that can be applied to some audio power transistors is limited because of the poor frequency response in the common emitter and common collector connections. The common collector connection offers the advantage of local voltage feedback that is inherent with this connection. Local feedback (one stage only) can be used on high phase shift amplifiers to increase the frequency response and decrease distortion.

## PREAMPLIFIERS

Preamplifiers have two major functions: (1) increasing the signal level from a pick-up device to about 1 volt rms, and (2) providing compensation if required to equalize the input signal for a constant output with frequency.

The circuit of Figure 9.1 meets these requirements when the pick-up device is a magnetic phono cartridge (monaural or stereo), or a tape head. The total harmonic or I.M. (inter-modulation) distortion of the preamp is less than ½% at reference level output (1 volt).

This preamp will accommodate most magnetic pick-up impedances. The input impedance to the preamp increases with frequency because of the frequency selective negative feedback to the emitter of TR1. The impedance of the magnetic pick-ups will also increase with frequency but are below that of the preamp.



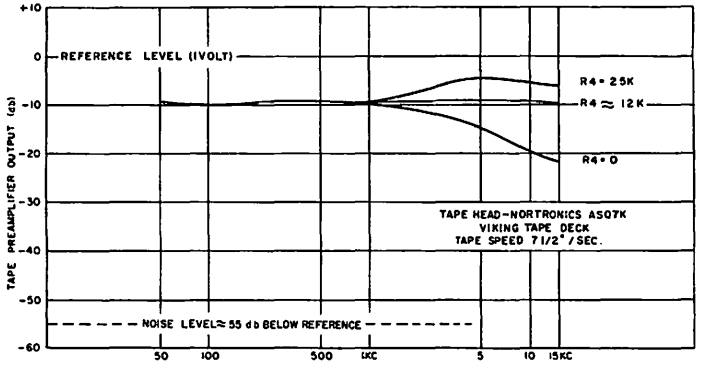

**PHONO-TAPE PREAMPLIFIER**

**Figure 9.1**

The first two stages of this circuit have a feedback bias arrangement with R3 feeding bias current to the base of TR1 that is directly proportional to the emitter current of TR2. The output stage is well stabilized with a 5K emitter resistance. TR4 is used to stabilize the circuit bias conditions from 25° to 55°C (130°F) ambient and also with variations in $h_{FE}$ for TR1 and TR2. Thus TR4 is not used as a signal amplifier, but as a collector load resistor for TR1. Its resistance will decrease with either increasing ambient temperature or increasing collector current from TR1. The increasing collector current of TR1 may be a result of either higher ambient temperature or higher $h_{FE}$ transistors. The collector to emitter resistance of TR4 will also decrease due to the leakage current ($I_{CO}$) of TR4 itself with increasing ambient temperature. The stabilizing circuit (R2, R5, and R6) for TR4 was selected so that TR4 (as the collector load for TR1) would have the desired temperature characteristic to stabilize the collector voltage of TR1, with increasing ambient temperature up to 130°F. The collector voltage of TR1 is the base bias voltage for TR2, and TR2 biases TR1 as indicated above.

TR4, in addition to its role as a temperature sensitive resistance, acts as a current sensitive resistance and thus automatically adjusts its resistance for $h_{FE}$ variations of TR1 and TR2 to maintain the collector voltage at TR1 between .75 and 1.6 volts.

The AC negative feedback from the collector of TR2 to the emitter of TR1 is frequency selective to compensate for the standard NAB recording characteristic for tape or the standard RIAA for phonograph records. The flat response from a standard NAB recorded tape occurs with the Treble Control (R4) near mid-position or 12K ohms (see Figure 9.2). There is about 5 db of treble boost with the Control at 25K and approximately 12 db of treble cut with R4 = 0. Mid-position of the Treble Control also gives flat response from a standard RIAA recording. This treble equalization permits adjustment for variations in program material, pick-ups, and loudspeakers.




**TAPE PREAMPLIFIER RESPONSE FROM NAB RECORDING**
**Figure 9.2**

The RIAA feedback network (with Treble Control at mid-position) has a net feedback resistance of 7.5K to decrease the gain because of the higher level input. This resistance has a .01 $\mu$f capacitor in parallel for decreasing the amplifier gain at the higher frequencies in accordance with RIAA requirements. This eliminates the need to load a reluctance pick-up with the proper resistance for high frequency compensation. If it is desirable to build the preamplifier for phonograph use only, the compensating feedback network would consist only of a .04 $\mu$f feedback capacitor in series with a 7.5K resistor (or a 10K Treble Control) which has a .01 $\mu$f capacitor in parallel.

The manufacturer of a piezoelectric pickup often has a recommended network for converting his pick-up to a velocity device, so that it may be fed into an input jack intended for a magnetic pickup.

The voltage feedback from the collector of TR2 decreases at lower frequencies because of the increasing reactance of the feedback capacitor in series with the Treble Control. In switch position #1 the capacitor C3 is large enough to make the voltage feedback, and thus the gain, constant across the audio spectrum. This flat preamp response can be used with a tuner, F.M. decoder or microphone. The input impedance to the preamp in #1 switch position is about 25K ohms, and 15 millivolts input level gives 1 volt output. When used with an F.M. tuner or decoder the standard 75 micro-second de-emphasis can be accomplished in this preamp by shunting the 7500 ohm feedback resistor with .01 micro-farads.

In switch position #3 with the Treble equalization at 30K, the equalized response is flat from 50 cycles to 7½ Kc with an NAB recording at 3¾"/second. The S/N (signal-to-noise ratio) is 50 db.

The reference level for S/N measurements in tape recording is the maximum level at which a 400 cycle signal can be recorded at 2% harmonic distortion. In vacuum tube circuitry there is a problem in maintaining high S/N at audio frequencies because of the lower signal transfer from a magnetic pickup (tape, phono, or microphone) to the tube grid. The lower input impedance of the transistor more nearly matches the source for a better signal transfer and thus improved S/N.

A good S/N can be realized with a tape head inductance between .2 and 1 henry. The .4 henry tape head gave a very flat response with this preamp (see Figure 9.2) and a S/N of approximately 55 db. One has to be careful of the physical position of the tape head or the noise output will increase considerably due to pick-up of stray fields. For good S/N it is important that the tape head have good shielding and hum bucking. The S/N is improved by the 100 ohm resistor in the emitter of TR2 which reflects a higher input impedance for this stage and thus TR1 has increased gain.

The preamp in the #2 (Tape at 7½"/sec.) position requires about 1.5 mv input signal at 1 Kc for 1 volt output. Therefore a tape head with a 1 Kc reference level output of 1.5 to 3 mv is desirable.

The emitter-follower output stage of the preamp gives a low impedance output for a cable run to a power amplifier (transistor or tube) and acts as a buffer so that any preamp loading will not affect the equalization characteristic.

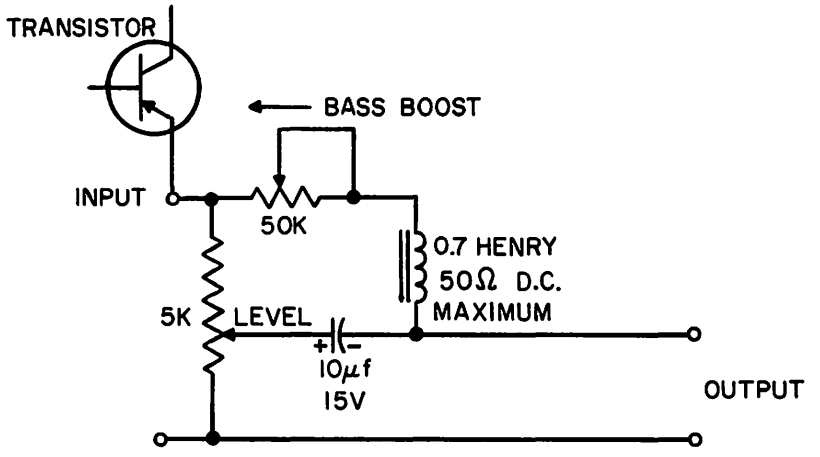
The Treble Control should have a linear taper and the Level Control an audio taper. Two 9 volt batteries will give good life in this application since the total supply drain is approximately 4 ma DC. This 18 volts may also be obtained by suitable decoupling from a higher voltage supply with an 18 volt zener.

This is a high gain circuit and thus care should be used in layout to prevent regenerative feedback to the input. Also, a switching circuit at the input will increase the possibilities for hum pick-up and thus decrease the S/N.

## BASS BOOST CIRCUIT

The bass boost circuit of Figure 9.3 operates on the output of the preamp (Figure 9.1). With this addition, the operator has the necessary treble and bass control to compensate for listening levels, or deficiencies in program material, pick-up, speakers, etc. This bass boost circuit gives the operator independent control of the level, or amount of bass boost desired, or the level control can be used as a loudness control.

It is usually desirable to have some method of boosting the level of the lower




BASS BOOST CIRCUIT

**Figure 9.3**

portion of the audio spectrum as the overall sound level is decreased. This is to compensate for the non-linear response of the human ear as shown in the Fletcher-Munson curves that are often referred to in the audio industry. The ear requires a higher level for the low frequency sound to be audible as the frequency is decreased and also as the overall spectrum level is decreased.

Figure 9.4 shows the frequency characteristics of this bass boost circuit. With the level control set for zero attenuation at the output there is no bass boost available, but as the output level is attenuated, the available bass boost increases.

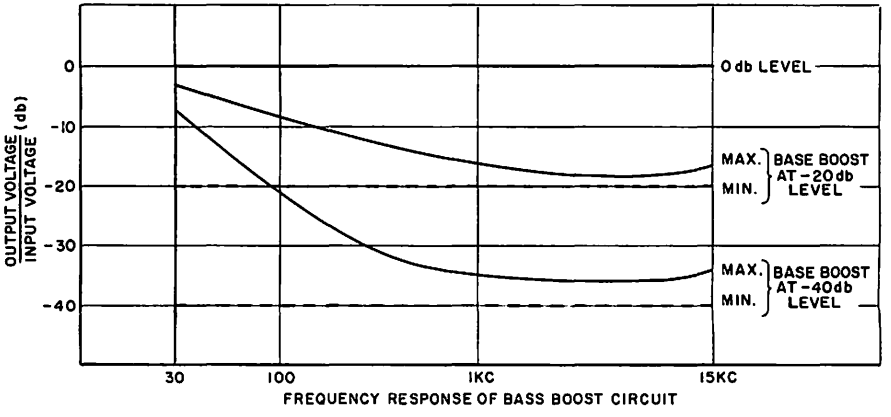



**Figure 9.4**

Figure 9.4 shows the frequency response (lower dashed curve) when the output is attenuated 40 db and the Bass Boost Control is set for minimum (50K ohms). The solid curve immediately above represents the frequency response when the Bass Boost Control is set at maximum (zero ohms). Thus a frequency of 30 cycles can have anything

from zero to 27 db of boost with respect to 1 KC, depending on the adjustment of the Bass Boost Control.

The Fletcher-Munson contours of equal loudness level show most of the contour changes involve a boost of the bass frequencies at the lower levels of intensity. Therefore, this circuit combination fulfills the requirements of level control, bass boost and loudness control. The Bass Boost Control may be a standard 50K potentiometer with a linear taper. The desired inductance may be obtained by using the green and yellow leads on the secondary of Argonne transistor transformer #AR-128 (Lafayette Radio Catalog).

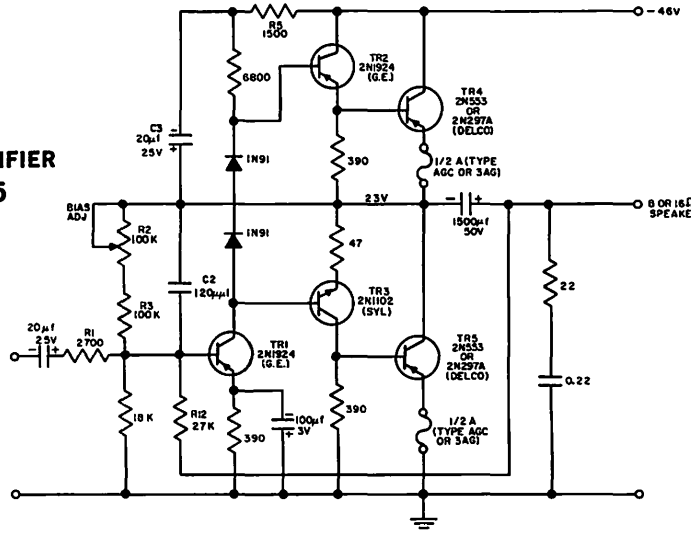
## POWER AMPLIFIERS

It is difficult to attain faithful reproduction of a square wave signal with a transformer amplifier. A high quality transformer is required and it must be physically large to have a good response at the low frequencies. Thus, a great deal of effort has gone into developing transformerless push-pull amplifiers using vacuum tubes. Practical circuits, however, use many power tubes in parallel to provide the high currents necessary for direct-coupling to a low impedance load such as loudspeakers.

The advent of power transistors has sparked new interest in the development of transformerless circuits since the transistors are basically low voltage, high current devices. The emitter follower stage, in particular, offers the most interesting possibilities since it has low inherent distortion and low output impedance.

Figure 9.5 is a direct-coupled power amplifier with excellent low frequency response, and also has the advantage of D.C. feedback for temperature stabilization of all stages. This feedback system stabilizes the voltage division across the power output transistors TR4 and TR5 which operate in a single-ended Class B push-pull arrangement. TR2 and TR3 also operate Class B in the Darlington connection to increase the current gain. Using an NPN for TR3 gives the required phase inversion for driving TR5 and also has the advantage of push-pull emitter follower operation from the output of TR1 to the load. Emitter follower operation has lower inherent distortion and low output impedance because of the 100% voltage feedback.

**10-WATT AMPLIFIER**
**Figure 9.5**



TR4 and TR5 have a small forward bias of 10 to 20 ma to minimize cross-over distortion and it also operates the output transistors in a more favorable beta range. This bias is set by the voltage drop across the 390 ohm resistors that shunt the input to TR4 and TR5. TR2 and TR3 are biased at about 1 ma (to minimize crossover distortion) with the voltage drop across the two 1N91 germanium diodes. The junction diodes have a temperature characteristic similar to the emitter-base junction of a transistor. Therefore, the two diodes also give compensation for the temperature variation of the emitter-base resistance of TR2, TR4 and TR3. These resistances decrease with increasing temperature, thus the decrease in forward voltage drop of approximately 2 millivolts/degree centigrade for each of the diodes provides temperature compensation.

The 47Ω resistor in the emitter of TR3 aids the stabilization of this transistor stage and also decreases distortion through local feedback.

TR1 is a Class A driver with an emitter current of about 3 ma. Negative feedback to the base of TR1 lowers the input impedance of this stage and thus requires a source impedance that is higher so the feedback current will flow into the amplifier rather than into the source generator. The resistor R1 limits the minimum value of source impedance. The bias adjust R2 is set for one-half the supply voltage across TR5.

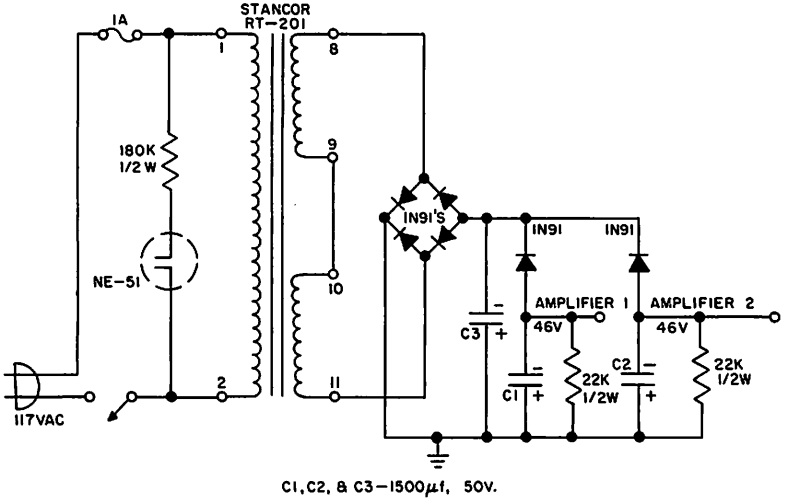
About 11 db of positive feedback is applied by way of C3 across R5. This bootstrapping action helps to compensate for the unsymmetrical output circuit and permits the positive peak signal swing to approach the amplitude of the negative peak. This positive feedback is offset by about the same magnitude of negative feedback via R2 and R3 to the base of TR1. The net amount of negative feedback is approximately 14 db resulting from R12 connecting the output to the input. In addition, there is the local feedback inherent in the emitter follower stages. The value for the C2 feedback capacitor was chosen for optimum square wave response (i.e., maximum rise time and minimum overshoot).

A ½ ampere fuse is used in the emitter of each output transistor for protective fusing of TR4 and TR5, and also to provide local feedback since the ½ ampere type AGC or 3AG fuse has about 1 ohm D.C. resistance. This local feedback increases the bias stability of the circuit and also improves the declining frequency response of TR4 and TR5 at the upper end of the audio spectrum. Because of the lower transistor efficiency above 10 Kc, care should be used when checking the amplifier for maximum continuous sinewave output at these frequencies. If continuous power is applied for more than a short duration, sufficient heating may result to raise the transistor current enough to blow the ½ A fuses. There is not sufficient sustained high frequency power in regular program material to raise the current to this level. Thus the actual performance of the amplifier does not suffer since the power level in music and speech declines as the frequency increases beyond about 1 to 2 Kc.

The speaker system is shunted by 22 ohms in series with .2 μfd to prevent the continued rise of the amplifier load impedance and its accompanying phase shift beyond the audio spectrum.

The overall result, from using direct-coupling, no transformers, and ample degeneration, is an amplifier with output impedance of about 1 ohm for good speaker damping, low distortion, and good bandwidth. The power response at 1 watt is flat from 30 cycles to 15 KC and is down 3 db at 50 KC. At this level the total harmonic and I.M. distortion are both less than 1%. At 7 watts the I.M. distortion is less than 2½% and the total harmonic distortion is less than 1% measured at 50 cycles, 1 KC, and 10 KC. The performance of the amplifier of Figure 9.5 is about equal for both 8 and 16 ohm loads.

This amplifier is capable of about 8 watts of continuous output power with 1 volt r.m.s. input, or 10 watts of music power into 8 or 16 ohms when used with the power supply of Figure 9.6. This power supply has diode decoupling which provides excellent separation (80 db) between the two stereo amplifier channels.



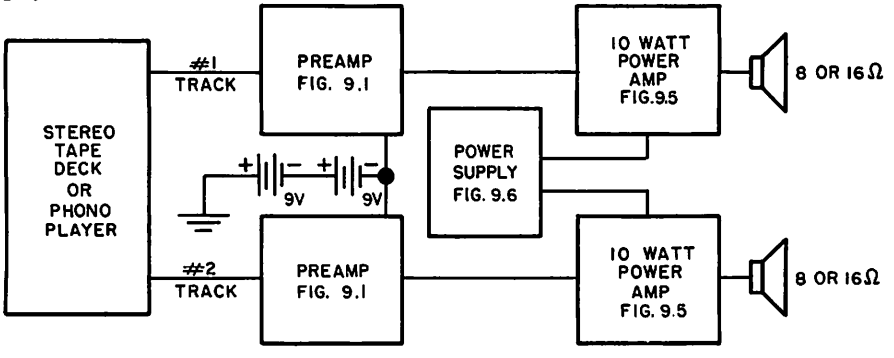

**POWER SUPPLY FOR STEREO SYSTEM**

**Figure 9.6**

The power transistors TR4 and TR5 should each be mounted on an adequate heat radiator such as used for transistor output in an automobile radio, or mounted on a 3" x 3" x 3/32" aluminum plate that is insulated from the chassis.

## STEREOPHONIC SYSTEM

A complete semiconductor, stereophonic playback system may be assembled by using the following circuits in conjunction with a stereophonic tape deck or phono player.




**BLOCK DIAGRAM OF STEREOPHONIC SYSTEM**

**Figure 9.7**

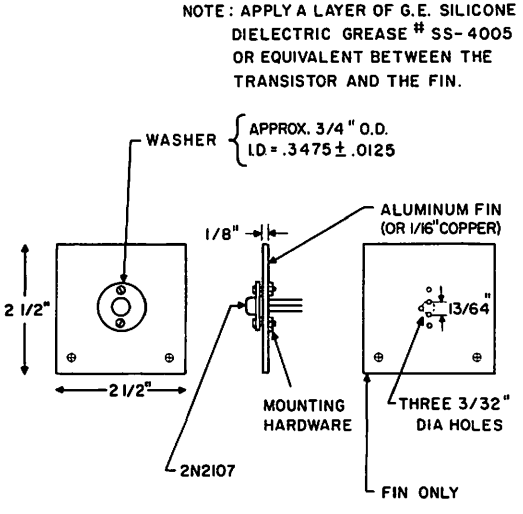
## SILICON POWER AMPLIFIERS

Some of the transistor power amplifiers to date have been lacking in their high frequency performance and their temperature stability. The diffused junctions of the 2N2107 and 2N2196 permit good circuit performance at high frequency. Silicon transistors are desirable for power output stages because of their ability to perform at much higher junction temperatures than germanium. This means smaller heat radiating fins can be used for the same power dissipation. On the negative side, silicon has higher saturation resistance which gives decreased operating efficiency that becomes appreciable when operating from low voltage supplies.

The power handling capability of a transistor is limited by both its electrical and thermal ratings. The electrical rating limit is a function of the transistor's voltage capability, and its maximum current at which the current gain is still usable. The thermal rating is limited by the transistor's maximum junction temperature. Therefore, it is desirable to provide the lowest thermal impedance path that is practical from junction to air. The thermal impedance from junction to case is fixed by the design of the transistor; thus it is advantageous to achieve a low thermal impedance from case to the ambient air.

The 2N2107 and 2N2196 are NPN diffused silicon transistors. They will be limited in their maximum power handling ability by the thermal considerations for many applications unless an efficient thermal path is provided from case to air.

These transistors are constructed with the silicon pellet mounted directly on the metal header, and therefore it is more efficient to have an external heat radiator in direct contact with this header than to make contact with the cap of the transistor package.

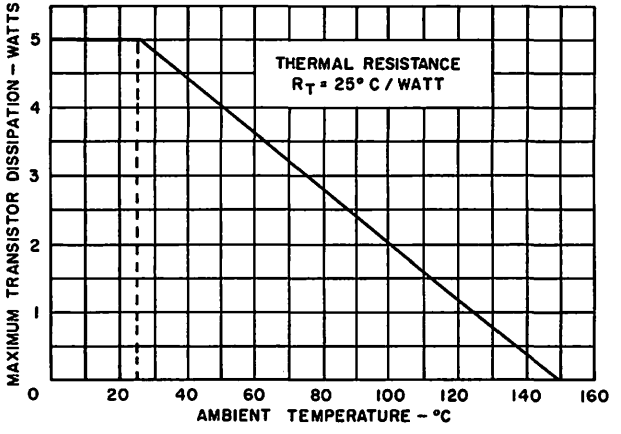



**TRANSISTOR HEAT RADIATOR**

**Figure 9.8**

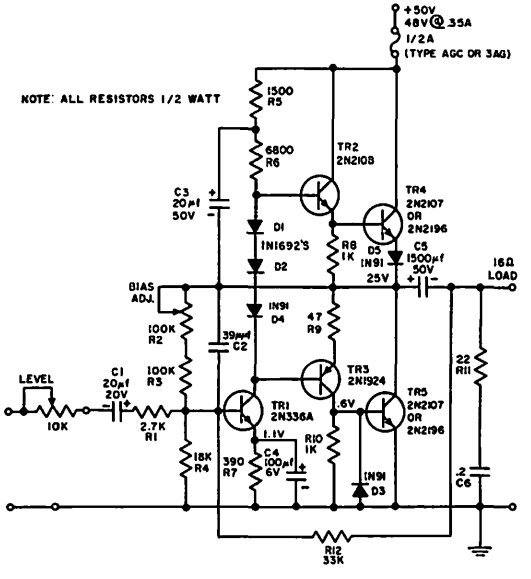
Figure 9.8 shows a practical method for achieving a maximum area of direct contact between the metal header and an aluminum fin for efficient heat transfer to the surrounding air. A plain washer with two holes drilled for the mounting hardware is

simple but quite adequate for securing the transistor header to the fin. Since air is a relatively poor thermal conductor, the thermal transfer can be improved by applying a thin layer of G-E Silicone Dielectric Grease #SS-4005 or equivalent between the transistor and the radiating fin before assembly. The fin may be anodized or flat paint may be used to cover all the surface except for the area of direct contact with the transistor header. An anodized finish would provide the insulation needed between the base and emitter leads and the sides of the feed-through holes in the aluminum fin. Figure 9.9 shows a thermal rating for the 2N2107 as assembled on the radiating fin.




**THERMAL CHARACTERISTIC**

**Figure 9.9**



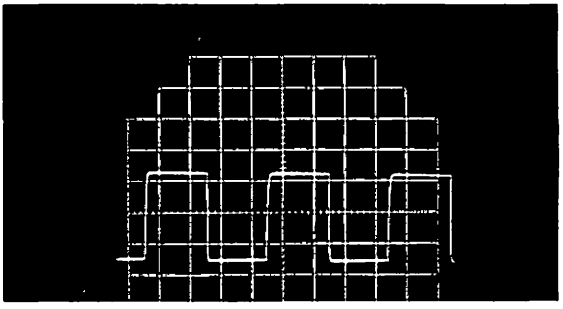

**10-WATT AMPLIFIER**

**Figure 9.10**

The circuit of Figure 9.10 is very much like that described for Figure 9.5. The opposite polarity is used for transistors, capacitors, and supply voltage. The 1N91 connected to the emitter of TR4 gives additional stabilization for this stage for variations in transistor beta and temperature. The forward voltage drop of this germanium diode must be offset by D4 to minimize cross-over distortion. The 1N91 diode at the base of TR5 has a leakage current which increases with temperature in a manner similar to the $I_{co}$ of TR3. D3 can thus shunt this temperature sensitive current to ground, whereas, if it were to flow into the base of TR5, it would be amplified in the output stages.

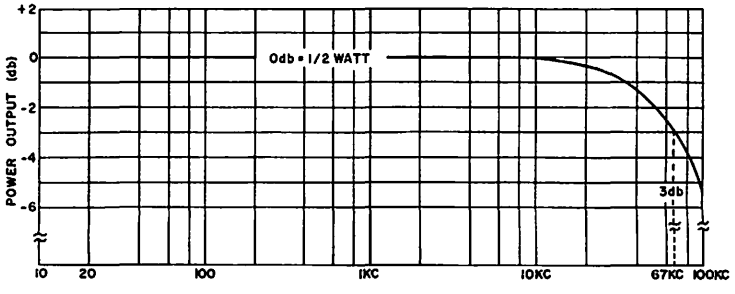
This circuit has about 20 db of overall negative feedback with R12 connecting the output to the input. The higher $h_{FE}$ of the two output units should be used for TR4.

The silicon power amplifier of Figure 9.10 has an output impedance of .5Ω for good speaker damping. The square wave response shown in Figure 9.11 is indicative of an amplifier with a good transient response and also a good bandwidth. The bandwidth is confirmed by the response curve of Figure 9.12. The power response at 5 watts output is flat within ⅓ db from 30 cycles to 15 Kc. The amplifier exhibits good recovery from overload, and the square wave peak power output without distorting the waveform is 12 watts.



**2 KC SQUARE WAVE RESPONSE**

**Figure 9.11**




**FREQUENCY RESPONSE**

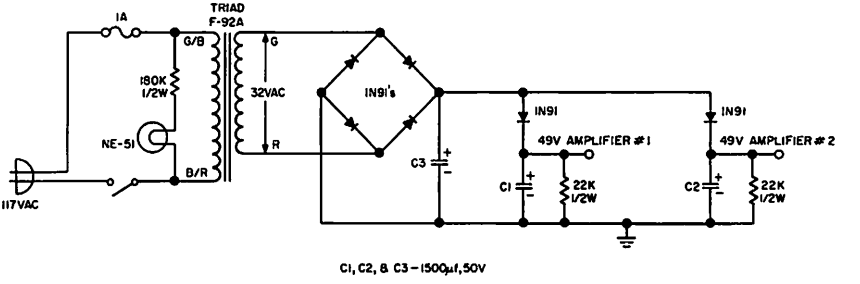
**Figure 9.12**

The 2N2107 output transistors, TR4 and TR5, were mounted on heat dissipating fins as shown in Figure 9.8 and the amplifier operated successfully delivering 1 watt rms 400 ~ continuous power to the load with no increase in total harmonic distortion

from room ambient of 75°F to 175°F (approx. 80°C). At 175°F the DC voltage across TR5 had decreased less than 15% from its room ambient value. Operation at higher temperatures was not attempted because of TR3 being a germanium transistor which has a maximum operating junction temperature of 85°C.

When operated with the 2N2107 heat radiator assembly, this amplifier can safely deliver up to 10 watts rms of continuous power to the load at room temperature. When driving a loudspeaker with program material at a level where peak power may reach 10 watts the rms power would generally be less than 1 watt. This amplifier, when operated with 2N2196's in the outputs, can be mounted on a smaller 2" x 2" fin because of its increased power capabilities. The 2N2196 has a case that simplifies the mounting on a heat radiator, and it has electrical characteristics that equal or excel the 2N2107 for this application.

The I.M. and total harmonic distortion of this amplifier is less than ½% at power levels under 3½ watts. The total harmonic distortion measured at 50 cycles, 400 cycles, and 10 Kc is still under 1% at 6 watts output and the I.M. distortion under 2½%. An rms input signal of 1¼ volts is required for 8 watts continuous output with a supply furnishing 350 ma at 48 volts. This amplifier has a 10-watt music power rating when used with the power supply of Figure 9.13. The amplifier operates with an efficiency of 47 to 60% and has a signal-to-noise ratio of better than 98 db.

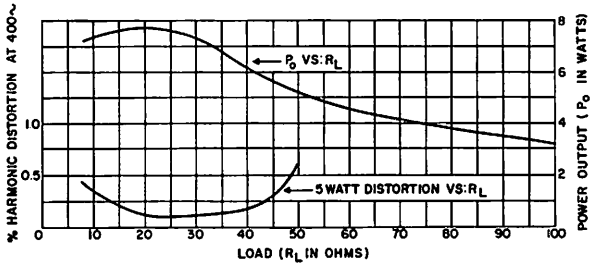



**POWER SUPPLY FOR STEREO SYSTEM**

**Figure 9.13**

The above performance tests were with a 16Ω resistive load. The performance near maximum power output will vary slightly with transistors of different beta values.

Varying values of saturation resistance for the output transistors TR4 and TR5 also affect the maximum power output.




**AMPLIFIER PERFORMANCE VS. LOAD**

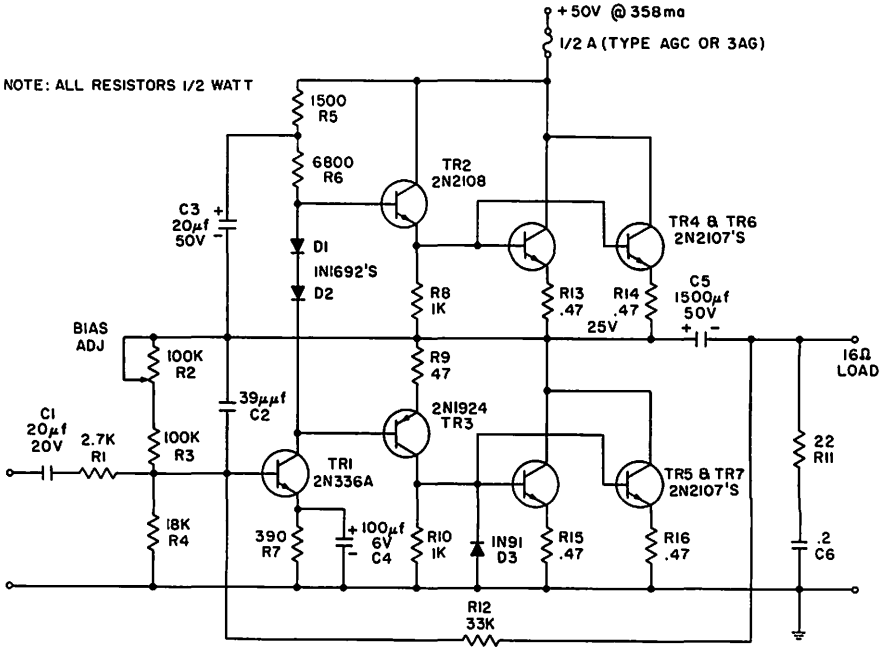
**Figure 9.14**

Figure 9.14 shows the load range for maximum performance. It indicates that for a varying load impedance such as a loudspeaker, the most desirable range is 16 to 40Ω. A 16Ω speaker system is in this range. A 20 to 600Ω auto-transformer should be used for driving a 600Ω line.

## 12-WATT AMPLIFIER

The amplifier of Figure 9.10 is limited in its maximum power output by the supply voltage and the saturation resistance of the output transistors, TR4 and TR5. The supply voltage can not be increased much beyond 50 volts at maximum amplifier signal swing without making the $V_{CE}$ rating for TR1 marginal. Under these conditions the saturation resistance becomes the limiting factor for obtaining increased power output.

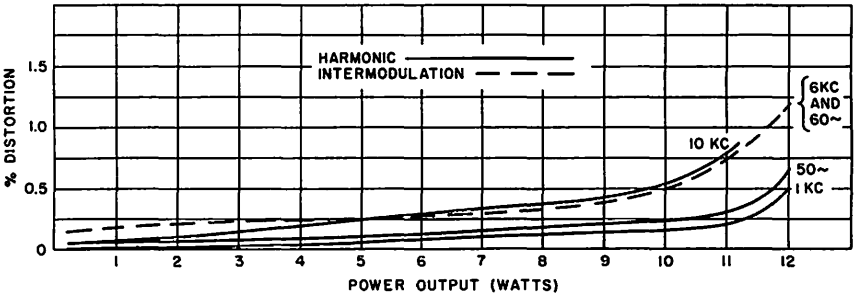
The circuit of Figure 9.15 uses two transistors in parallel for each of the outputs. This enables the saturation resistance to be reduced in half and gives 12 watts output. The .47 ohm resistor used in the emitter of the paralleled transistors gives a more uniform input characteristic for sharing of the input currents. These emitter resistors also give increased bias stabilization. The rest of the circuit is the same as Figure 9.10 except the 1N91 (D4) is not used in the collector of TR1 since there is no diode voltage to offset in series with output emitter.




**12-WATT AMPLIFIER**

**Figure 9.15**

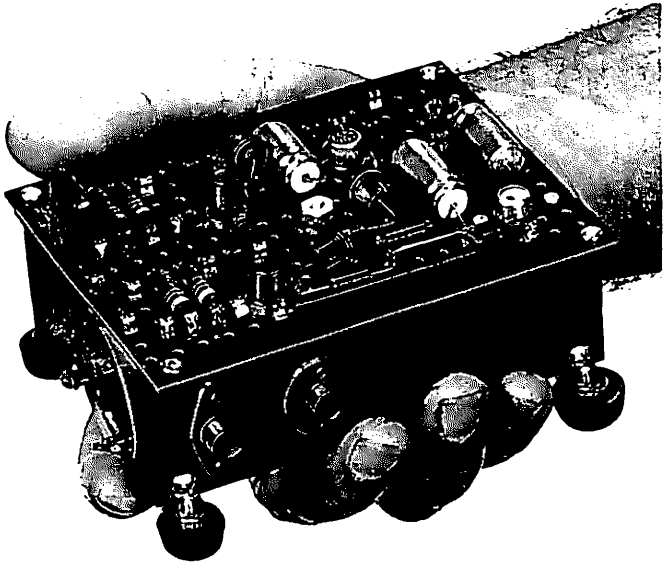
The performance of the 12-watt circuit is like that given previously for the circuit of Figure 9.10 except for the distortion vs.: power output. Figure 9.1 indicates the increased power output and also the lower distortion which is a second advantage of parallel operation of the outputs. Lower distortion results from parallel operation since the signal current swing in each transistor is approximately halfed and thus confined to the more linear portion of the transfer characteristic.




**DISTORTION VS. POWER OUTPUT**

**Figure 9.16**

The amplifier of Figure 9.15 operates at maximum power output with an efficiency of 67%. This circuit can be packaged with a minimum volume and weight without component crowding, see Figure 9.17. One of the paralleled output transistors uses the technique described in Figure 9.8 and the other makes for simplified mounting using the 2N2196 that was discussed previously. All four of the output transistors could be 2N2107's or all 2N2196's. Each mounting fin is 3/32" x 1½" x 4½" aluminum.



**12-WATT AMPLIFIER**

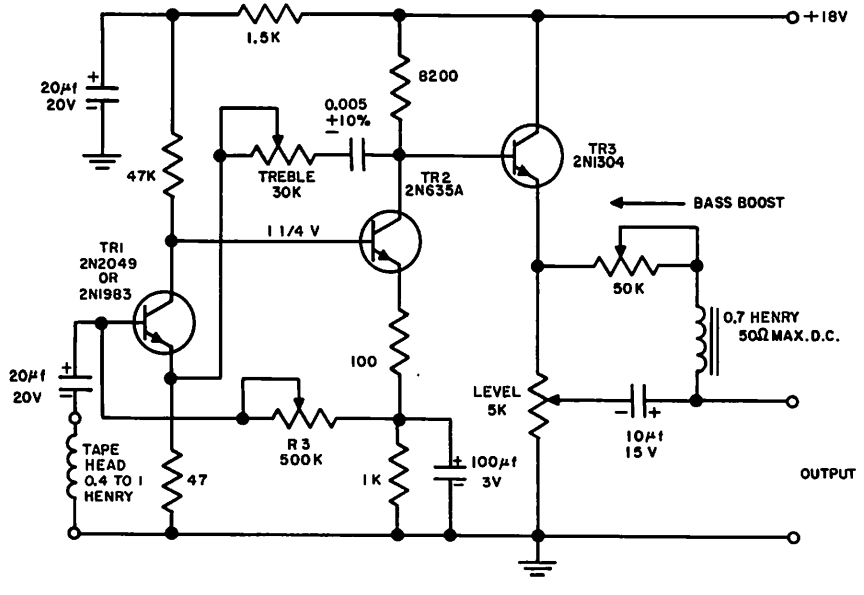
**Figure 9.17**

If the amplifier is powered by the supply of Figure 9.13, it will provide 10 watts of continuous output or 12 watts at Music Power Rating.

Either one of the amplifiers described will give superb performance in a stereo system when used to drive a 16Ω speaker that has at least moderate sensitivity.

## NPN PREAMPLIFIER

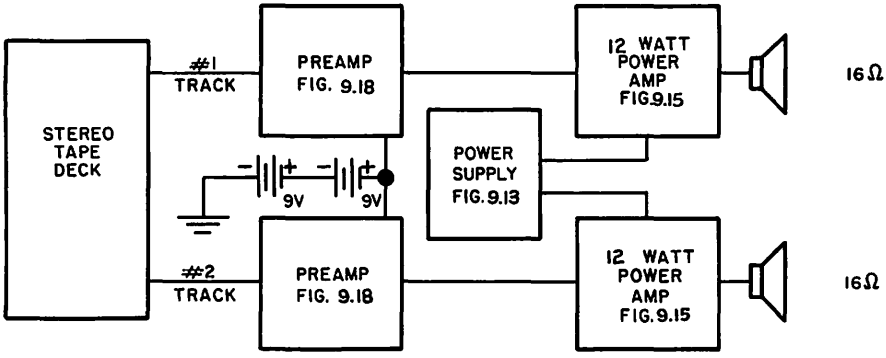
The preamplifier of Figure 9.18 is similar to that of Figure 9.1 except NPN transistors are used and the first stage does not have a compensating collector load. This first stage does not require a temperature sensitive resistance for the collector load since a planar – passivated transistor is used which inherently has very low leakage current ($I_{CBO}$). This preamplifier will operate at even higher ambient temperature than that of Figure 9.1 and has equivalent overall performance including 55 db S/N. 1.2 millivolts of input signal gives 1 volt output at 1 Kc. The input impedance is approximately 39K at 1 Kc. The equalized output from an NAB recorded tape at 7½"/sec. is within ±1 db from 50 cycles to 15 Kc using a .4 henry tape head. The higher input impedance of this preamp gives the best equalized output for a tape head in the .4 to 1 henry range. The value of R3 is selected or adjusted to give approximately 1¼ volts D.C. at the base of TR2 to accommodate the production spread of $h_{FE}$ for transistors used in the first two stages. A switch can be added to give other equalized functions as in Figure 9.1.




**TAPE PREAMPLIFIER**

**Figure 9.18**

A complete semiconductor, stereophonic tape playback system may be assembled by using the following circuits in conjunction with a stereophonic tape deck.




**BLOCK DIAGRAM OF STEREOPHONIC SYSTEM**

**Figure 9.19**

## REFERENCES

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Geiser, D.T., "Using Diodes as Power Supply Filter Elements," *Electronic Design*, June 10, 1959.

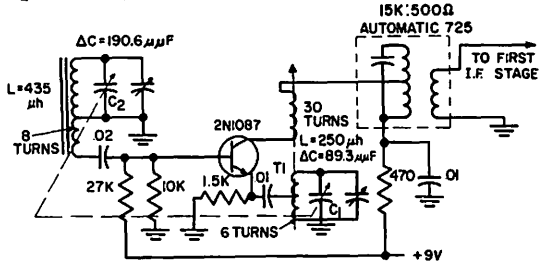
Jones, D.V., "All Transistor Stereo Tape System," *Electronics World*, July 1959.

# RADIO RECEIVER AND TUNER CIRCUITS

CHAPTER 10

## AUTODYNE CONVERTER CIRCUITS

The converter stage of a transistor radio is a combination of a local oscillator, a mixer and an IF amplifier. A typical circuit for this stage is shown in Figure 10.1.




FOR ADDITIONAL INFORMATION SEE PAGE 154

**AUTODYNE CONVERTER**

**Figure 10.1**

Redrawing the circuit to illustrate the oscillator and mixer sections separately, we obtain Figures 10.2 and 10.3.

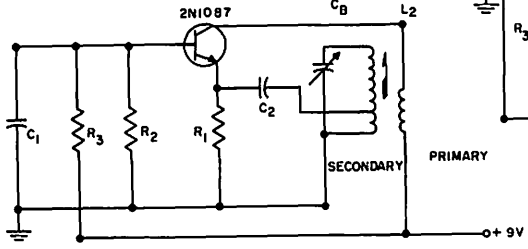



**Figure 10.2**

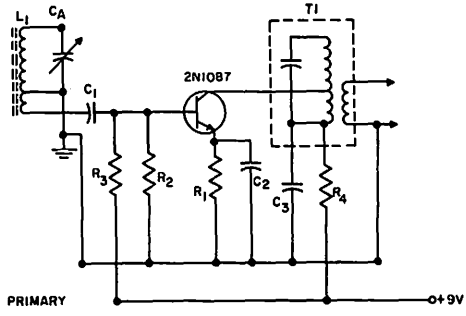



**Figure 10.3**

*The operation of the oscillator section (10.2) is as follows:*

Random noise produces a slight variation in base current which is subsequently amplified to a larger variation of collector current. This A.C. signal in the primary of $L_2$ induces an A.C. current into the secondary of $L_2$ tuned by $C_B$ to the desired oscillator frequency. $C_2$ then couples the resonant frequency signal back into the emitter circuit. If the feedback (tickler) winding of $L_2$ is properly phased the feedback will be positive (regenerative) and of proper magnitude to cause sustained oscillations. The secondary of $L_2$ is an auto-transformer to achieve proper impedance match between the high impedance tank circuit of $L_2$ and the relatively low impedance of the emitter circuit.

$C_1$ effectively bypasses the biasing resistors $R_2$ and $R_3$ to ground, thus the base is A.C. grounded. In other words, the oscillator section operates essentially in the grounded base configuration.

*The operation of the mixer section (10.3) is as follows:*

The ferrite rod antenna $L_1$ exposed to the radiation field of the entire frequency spectrum is tuned by $C_A$ to the desired frequency (broadcast station).

The transistor is biased in a relatively low current region, thus exhibiting quite non-linear characteristics. This enables the incoming signal to mix with the oscillator signal present, creating signals of the following four frequencies:

1. *The local oscillator signal.*
2. *The received incoming signal.*
3. *The sum of the above two.*
4. *The difference between the above two.*

The IF load impedance $T_1$ is tuned here to the difference between the oscillator and incoming signal frequencies. This frequency is called the intermediate frequency (I.F.) and is conventionally 455 KC/S. This frequency will be maintained fixed since $C_A$ and $C_B$ are mechanically geared (ganged) together. $R_4$ and $C_3$ make up a filter to prevent undesirable currents flowing through the collector circuit. $C_2$ essentially bypasses the biasing and stabilizing resistor $R_1$ to ground. Since the emitter is grounded and the incoming signal injected into the base, the mixer section operates in the "grounded emitter" configuration.

## IF AMPLIFIERS

A typical circuit for a transistor IF amplifier is shown by Figure 10.4.

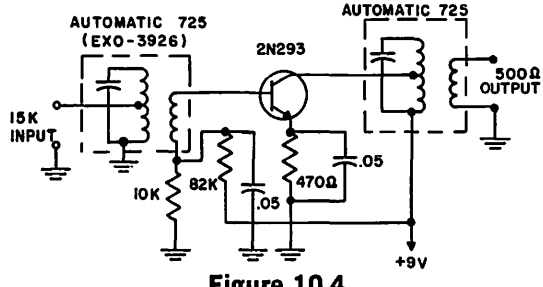



**Figure 10.4**

The collector current is determined by a voltage divider on the base and a large resistance in the emitter. The input and output are coupled by means of tuned IF transformers. The .05 capacitors are used to prevent degeneration by the resistance in the emitter. The collector of the transistor is connected to a tap on the output transformer to provide proper matching for the transistor and also to make the performance of the stage relatively independent of variations between transistors of the same type. With a rate-grown NPN transistor such as the 2N293, it is unnecessary to use neutralization to obtain a stable IF amplifier. With PNP alloy transistors, it is necessary to use neutralization to obtain a stable amplifier and the neutralization capacitor depends on the collector capacitance of the transistor. The gain of a transistor IF amplifier will decrease if the emitter current is decreased. This property of the transistor can be used to control the gain of the IF amplifier so that weak stations and strong stations will produce the same audio output from a radio. Typical

circuits for changing the gain of an IF amplifier in accordance with the strength of the received signal are explained in the A.V.C. section of this chapter.

A.V.C. is a system which automatically varies the total amplification of the signal in a radio receiver with changing strength of the received signal carrier wave.

From the definition given, it would be correctly inferred that a more exact term to describe the system would be automatic gain control (A.G.C.).

Since broadcast stations are at different distances from a receiver and there is a great deal of variation in transmitted power from station-to-station, the field strength around a receiver can vary by several orders of magnitude. Thus, without some sort of automatic control circuit, the output power of the receiver would vary considerably when tuning through the frequency band. It is the purpose of the A.V.C. or A.G.C. circuit to maintain the output power of the receiver constant for large variations of signal strengths.

Another important purpose of this circuit is its so-called "anti-fading" properties. The received signal strength from a distant station depends on the phase and amplitude relationship of the ground wave and the sky wave. With atmospheric changes this relationship can change, yielding a net variation in signal strength. Since these changes may be of periodic and/or temporary nature, the A.V.C. system will maintain the average output power constant without constantly adjusting the volume control.

The A.V.C. system consists of taking, at the detector, a voltage proportional to the incoming carrier amplitude and applying it as a negative bias to the controlled amplifier thereby reducing its gain.

In tube circuits the control voltage is a negative going DC grid voltage creating a loss in transconductance (Gm).

In transistor circuits various types of A.V.C. schemes can be used.

## EMITTER CURRENT CONTROL

As the emitter current of a transistor is reduced (from 1.0 ma to .1 ma for instance) various parameters change considerably (see Figure 10.5).

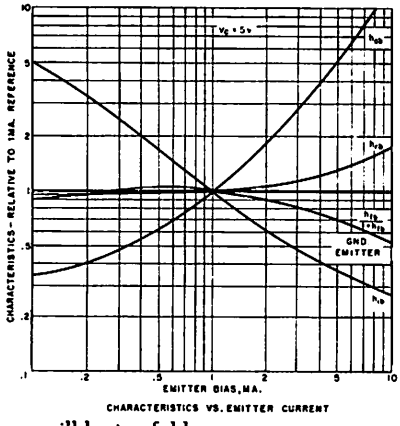



**Figure 10.5**

The effect of these changes will be twofold:

1. *A change in maximum available gain and*
2. *A change in impedance matching since it can be seen that both $h_{ob}$ and $h_{ib}$ vary radically.*

Therefore, a considerable change in power gain can be obtained as shown by Figure 10.6.

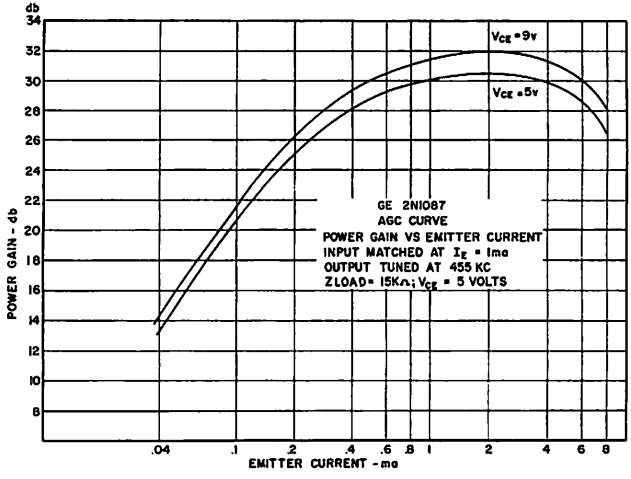



**Figure 10.6**

On the other hand, as a result of $I_{CO}$ (collector leakage current) some current always flows, thus a transistor can be controlled only up to a point and cannot be "cut-off" completely. This system yields generally fair control and is, therefore, used more than others. For performance data see Figure 10.7.

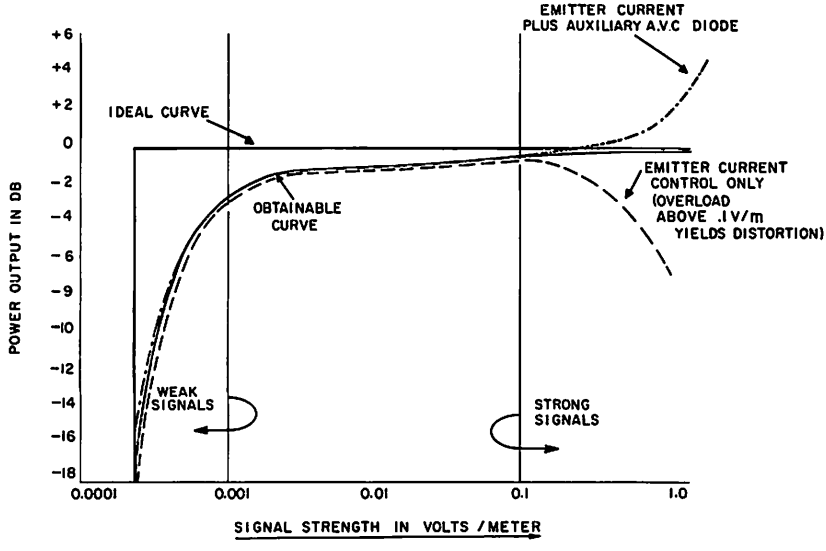



**Figure 10.7**

## AUXILIARY A.V.C. SYSTEMS

Since most A.V.C. systems are somewhat limited in performance, to obtain improved control, auxiliary diode A.V.C. is sometimes used. The technique used is to shunt some of the signal to ground when operating at high signal levels, as shown by Figure 10.8.

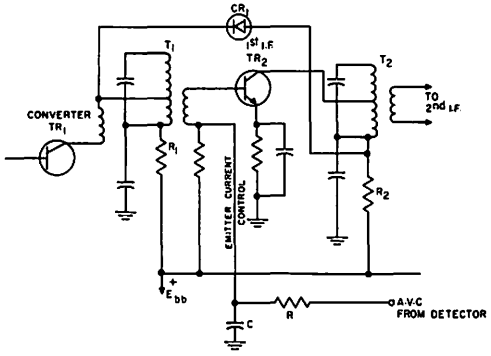



**Figure 10.8**

In the circuit of Figure 10.8, diode $CR_1$ is back-biased by the voltage drops across $R_1$ and $R_2$ and represents a high impedance across $T_1$ at low signal levels. As the signal strength increases, the conventional emitter current control A.V.C. system creates a bias change reducing the emitter current of the controlled stage. This current reduction coupled with the ensuing impedance mismatch creates a power gain loss in the stage. As the current is further reduced, the voltage drop across $R_2$ becomes smaller thus changing the bias across $CR_1$. At a predetermined level $CR_1$ becomes forward biased, constituting a low impedance shunt across $T_1$ and creating a great deal of additional A.V.C. action. This system will generally handle high signal strengths as can be seen from Figure 10.7. Hence, almost all radio circuit diagrams in the circuit section of this manual use this system in addition to the conventional emitter current control.

## DETECTOR STAGE

In this stage (see Figure 10.9), use is made of a slightly forward biased diode in order to operate out of the square law detection portion of the I-E characteristics. This stage is also used as source of AGC potential derived from the filtered portion of the signal as seen across the volume control (R9). This potential, proportional to the signal level, is then applied through the AGC filter network C4, R7 and C5 to the base of the 1st IF transistor in a manner to decrease collector current at increasing signal levels. R8 is a bias resistor used to fix the quiescent operating points of both the 1st IF and the detector stage, while C6 couples the detected signal to the audio amplifier. (See Chapter 8 on Audio Amplifiers.)

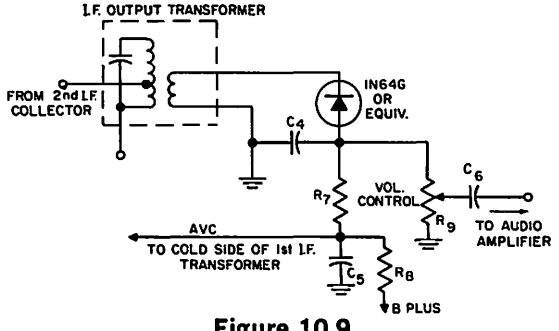



**Figure 10.9**

## REFLEX CIRCUITS

"A reflex amplifier is one which is used to amplify at two frequencies – usually intermediate and audio frequencies."*

The system consists of using an I.F. amplifier stage and after detection to return the audio portion to the same stage where it is then amplified again. Since in Figure 10.10,

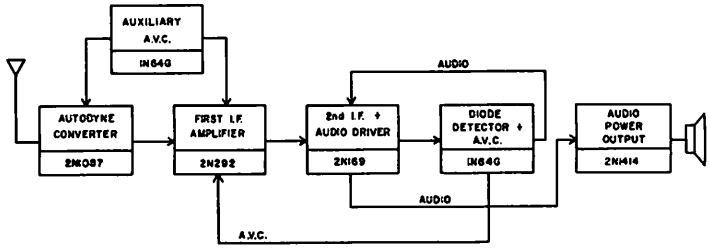



**Figure 10.10** BLOCK DIAGRAM OF RECEIVER

two signals of widely different frequencies are amplified, this does not constitute a *"regenerative effect"* and the input and output loads of these stages can be split audio –I.F. loads. In Figure 10.11, the I.F. signal (455 Kc/s) is fed through T2 to the detector circuit CR1, C3 and R5. The detected audio appears across the volume control R5 and is returned through C4 to the cold side of the secondary of T1.

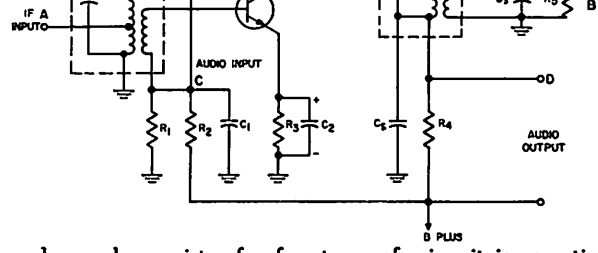



**Figure 10.11**

Since the secondary only consists of a few turns of wire, it is essentially a short circuit at audio frequencies. C1 bypasses the I.F. signal otherwise appearing across the parallel combination of R1 and R2. The emitter resistor R3 is bypassed for both audio and I.F. by the electrolytic condenser C2. After amplification, the audio signal appears across R4 from where it is then fed to the audio output stage. C5 bypasses R4 for I.F. frequencies and the primary of T2 is essentially a short circuit for the audio signal.

The advantage of "reflex" circuits is that one stage produces gain otherwise requiring two stages with the resulting savings in cost, space, and battery drain. The disadvantages of such circuits are that the design is considerably more difficult, although once a satisfactory receiver has been designed, no outstanding production difficulties should be encountered. Other disadvantages are a somewhat higher amount of playthrough (i.e. signal output with volume control at zero setting), and a minimum volume effect. The latter is the occurrence of minimum volume at a volume control setting slightly higher than zero. At this point, the signal is distorted due to the

* F. Langford-Smith, Radiotron Designers Handbook, Australia, 1953, p. 1140

balancing out of the fundamentals from the normal signal and the out-of-phase play-through component. Schematics of complete receivers will be found at the end of this chapter and in Chapter 20.

## FM TUNER

The FM tuner shown in Figure 10.17 is especially suited to the home constructor because it does not require an elaborate alignment procedure. In fact, only the local oscillator is tuned and the only likely adjustment is either to stretch or squeeze the local oscillator coil to give the correct coverage of the FM band. It works in the following manner: See Figure 10.17.

A tunnel diode oscillating at approximately one-half the input signal frequency is inductively coupled to the antenna input. When correctly tuned, the very stable tunnel diode oscillator acts as a second harmonic mixer producing a stable intermediate frequency centered at 200 Kc/sec. The intermediate frequency is amplified by two simple amplifiers, each consisting of two transistors giving a total voltage gain of around 100,000. The signal is then limited to give a square-wave which is being frequency modulated in the same manner as the transmitted signal. The square-wave is used to charge a capacitor-resistor-diode combination having a short time-constant producing a standard-sized pulse every time the square-wave goes positive. Pulse-minded readers will recognize this circuit as being a differentiator with the diode clipping the negative spike produced by differentiation. There is, at this point in the circuit, a string of similarly shaped pulses keeping step with the frequency modulated input signal.

The average value of these pulses can be shown to be the audio originally modulating the FM carrier. This average is obtained by allowing the pulses to charge a capacitor through a resistor (an integrating circuit) the combination having a fairly long time constant. The resulting output is amplified by the final transistor which incorporates de-emphasis in its feed-back loop.

The sensitivity is only 50 $\mu$V/20 db quieting and the receiver, as it stands, is only useful for receiving local stations. Addition of an RF stage would be a significant improvement.

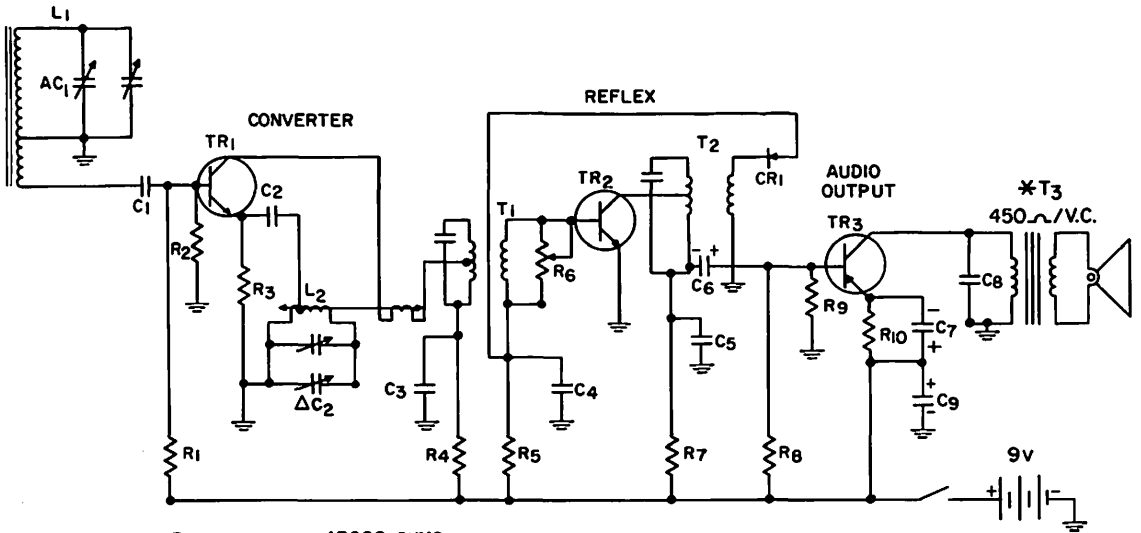
The tuner compares very favorably with circuits using more conventional forms of discrimination because distortion is not dependent on the accurate alignment of many tuned circuits. Harmonic distortion after limiting is excellent, being better than 1%.

## AM TUNER

The tuner shown in Figure 10.18 is useful for high quality reception of local AM broadcast stations. A tuned RF stage is used to drive a Class B emitter-follower detector. The natural base-emitter voltage drop of the emitter-follower is overcome by providing a small amount of bias from a conducting germanium diode. This also compensates for any change in the base-emitter voltage drop with temperature.

The two tuned circuits are aligned by equalizing inductance at the low frequency end of the tuning range (tuning capacitors at maximum value) and trimming capacity at the high frequency end in the conventional manner of aligning T.R.F. receivers. Bandwidth at 6 db is approximately 25 Kc/s. Owing to the wide-band capability of the tuner, difficulty might be experienced in adequately separating stations close to one another in frequency. For this reason, a directional antenna ($L_1$) is used in the design so additional rejection of unwanted signals may be obtained by rotating the antenna.

## COMPLETE RADIO RECEIVER CIRCUIT DIAGRAMS

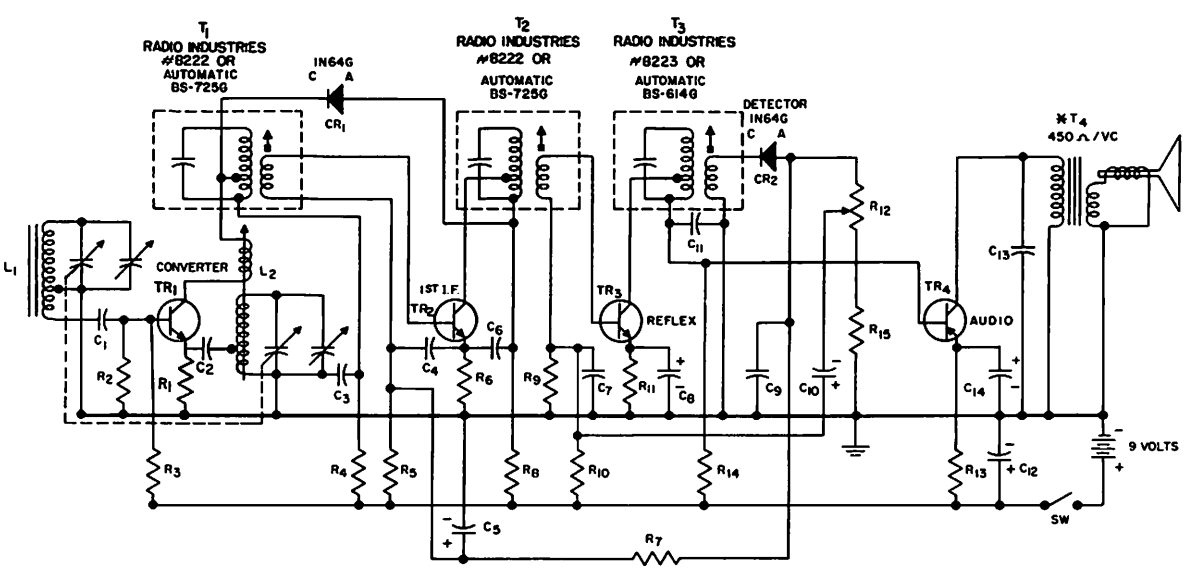



| | | | | | |
|---|---|---|---|---|---|
| $R_1$ | 47,000 OHMS | $C_1$ | .02μf | $TR_1$ | 2N1087 |
| $R_2$ | 10,000 OHMS | $C_2$ | .01 μf | $TR_2$ | 2N1121 OR 2N1087 $CR_1$ IN64G OR EQUIV. |
| $R_3, R_7$ | 1500 OHMS | $C_3$ | .01 μf | $TR_3$ | 2N1415 |
| $R_4$ | 270 OHMS | $C_4$ | .01 μf | $T_1$, | AUTOMATIC BS725G OR RADIO INDUSTRIES #8222 |
| $R_5$ | 33,000 OHMS | $C_5$ | .002μf | $T_2$ | AUTOMATIC BS614G OR RADIO INDUSTRIES #8223 |
| $R_6$ | 2,000 OHMS VOLUME CONTROL | $C_6$ | 5μf - 12V | NOMINAL SENSITIVITY: 2.0 MILLIVOLTS/METER (MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT) | |
| $R_8$ | 1000 OHMS | $C_7$ | 50μf - 3V | MAXIMUM POWER OUTPUT: 75 MILLIWATTS | |
| $R_9$ | 4700 OHMS | $C_8$ | .05μF | SELECTIVITY AT -6db: 10 KC/S | |
| $R_{10}$ | 100 OHMS | $C_9$ | 50μfd-12V | SELECTIVITY AT -60db: 120 KC/S | |
| | | | | TOTAL BATTERY DRAIN: 19 MILLIAMPS | |

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 154

**THREE TRANSISTOR REFLEX RECEIVER**

**Figure 10.12**



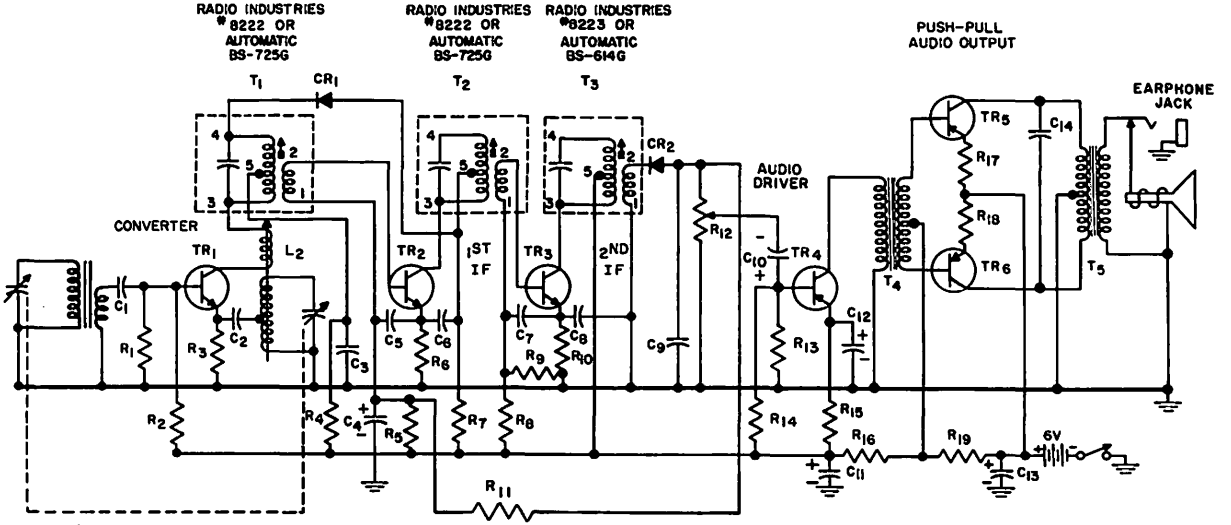

| | | | | | |
|---|---|---|---|---|---|
| $R_1$, $R_{14}$, | 1500 OHM | $C_1$, $C_{11}$, | .02μfd | $L_1$, | 435μh±10% |
| $R_2$, | 6800 OHM | $C_2$, $C_3$, $C_7$, | .01μfd | $L_2$, | 250μh±10% |
| $R_3$, | 27,000 OHM | $C_4$,$C_6$,$C_9$,$C_{13}$ | .05μfd | $CR_1$,$CR_2$, | IN64G OR EQUIV. |
| $R_4$, $R_{11}$, | 470 OHM | $C_5$, | 15μfd, 12V | $\Delta C_1$ — 190.6 | R/C MODEL 242 |
| $R_5$, | 82,000 OHM | $C_8$, | 50μfd, 3V | $\Delta C_2$ — 89.5 | |
| $R_6$, | 330 OHM | $C_{10}$, | 6μfd, 12V | | |
| $R_7$, $R_8$ | 3300 OHM | $C_{12}$, | 50μfd, 12V | | |
| $R_9$, | 10,000 OHM | $C_{14}$, | 100μfd, 12V | | |
| $R_{10}$, | 91,000 OHM | $TR_1$, | GE 2N1086, 2N1086A OR 2N1087 CONVERTOR | | |
| $R_{12}$, | VOLUME CONTROL 10,000 OHM AUDIO TAPER | $TR_2$, | 2N292 1ST I.F. | | |
| $R_{13}$, | 100 OHM | $TR_3$, | GE 2N169 OR 2N1121 REFLEX | | |
| $R_{15}$, | 120 OHM | $TR_4$, | 2N1415 AUDIO | | |

NOMINAL SENSITIVITY: 200 MICROVOLTS/METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT: 75 MILLIWATTS
SELECTIVITY AT -6db : 6.0 KC/S
SELECTIVITY AT -60db : 60.0 KC/S
TOTAL BATTERY DRAIN : 17.0 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 154

**FOUR TRANSISTOR NINE VOLT REFLEX RECEIVER**

**Figure 10.13**




| | |
|---|---|
| $R_1, R_8$ | 10,000 OHM |
| $R_2$ | 15,000 OHM |
| $R_3$ | 1500 OHM |
| $R_4$ | 270 OHM |
| $R_5$ | 47,000 OHM |
| $R_6$ | 220 OHM |
| $R_7, R_9$ | 2200 OHM |
| $R_{10}$ | 1000 OHM |
| $R_{11}, R_{14}$ | 4700 OHM |
| $R_{12}$ | VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER |
| $R_{13}$ | 68,000 OHM |
| $R_{15}$ | 470 OHM |
| $R_{16}$ | 100 OHM |
| $R_{17}, R_{18}$ | 8.2 OHM |
| $R_{19}$ | 33 OHM |

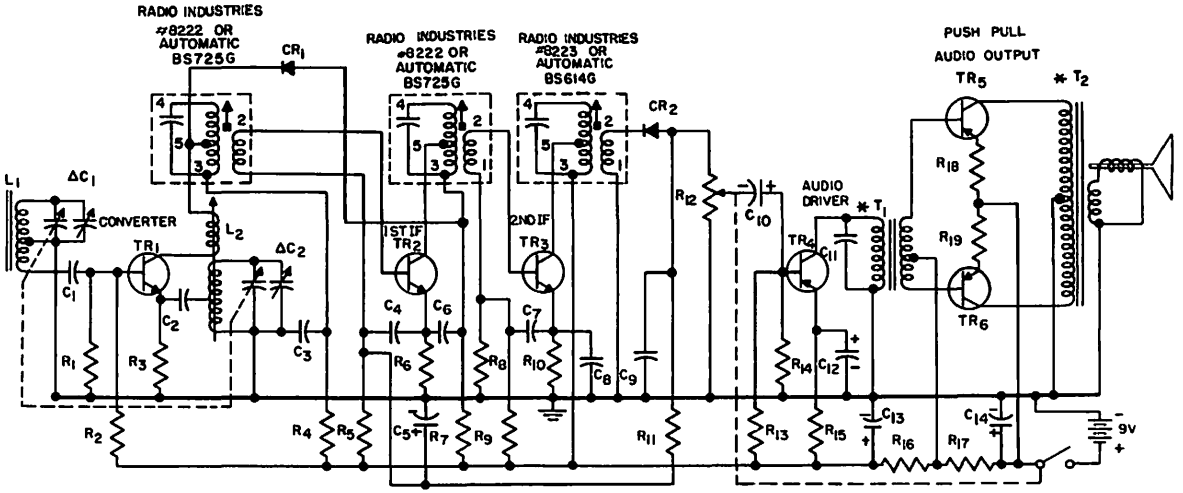
| | |
|---|---|
| $C_1$ | .02 μfd. |
| $C_2, C_3, C_5, C_6, C_7, C_8$ | .01μfd. |
| $C_4, C_{10}$ | 6μfd. - 6V |
| $C_9$ | .05μfd. |
| $C_{11}, C_{12}, C_{13}$ | 50μfd.-12V |
| $C_{14}$ | .2μfd. |
| CR1, CR2 | IN64G OR EQUIV |
| $TR_1$ | G.E. 2N1087 |
| $TR_2$ | G.E. 2N293 |
| $TR_3$ | G.E. 2N169 OR 2N1121 |
| $TR_4$ | G.E. 2N324 |
| $TR_5, TR_6$ | G.E. 2N1415 |
| * $T_4$ | 3600Ω/2000Ω CT |
| * $T_5$ | 360Ω CT/VC |

NOMINAL SENSITIVITY: 200 MICRO VOLTS/METER (MEASURED WITH 50 MILLIWATTS REFERENCE POWER)
MAXIMUM POWER OUTPUT: 200 MW
SELECTIVITY AT -6 db: 8.0 Kc/S
SELECTIVITY AT -60 db: 60.0 Kc/S
ZERO SIGNAL BATTERY DRAIN: 8 MILLIAMPS

* FOR FURTHUR INFORMATION SEE PAGE 154

**SIX TRANSISTOR SIX VOLT BROADCAST RECEIVER**

**Figure 10.14**




| | |
|---|---|
| $R_1$ | 6800 OHM |
| $R_2$ | 27,000 OHM |
| $R_3$ | 1500 OHM |
| $R_4, R_{10}, R_{15}$ | 470 OHM |
| $R_5$ | 68,000 OHM |
| $R_6$ | 330 OHM |
| $R_7$ | 3300 OHM |
| $R_8$ | 10,000 OHM |
| $R_9$ | 82,000 OHM |
| $R_{11}$ | 2700 OHM |
| $R_{12}$ | VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER |
| $R_{13}$ | 4700 OHM |
| $R_{14}$ | 56,000 OHM |
| $R_{16}$ | 220 OHM |
| $R_{17}$ | 33 OHM |

| | |
|---|---|
| $R_{18}, R_{19}$ | 8.2 OHM |
| $C_1$ | .02 μfd |
| $C_2, C_3$ | .01μfd |
| $C_4, C_6, C_7, C_8$ | .05μfd |
| $C_5, C_{10}$ | 6μfd, 12V |
| $C_9$ | .05μfd |
| $C_{11}$ | .003μfd |
| $C_{12}, C_{13}, C_{14}$ | 50μfd, 12V |
| $TR_1$ | G.E. 2N1087 CONVERTER |
| $TR_2$ | G.E. 2N293 IST I.F. |
| $TR_3$ | G.E. 2N169 OR 2N1121 2ND I.F. |
| $TR_4$ | G.E. 2N324 DRIVER |
| $TR_5, TR_6$ | G.E. 2N1415 AUDIO |
| * $T_1$ | 5,000 / 2600Ω CT |
| * $T_2$ | 250Ω CT/V.C. |

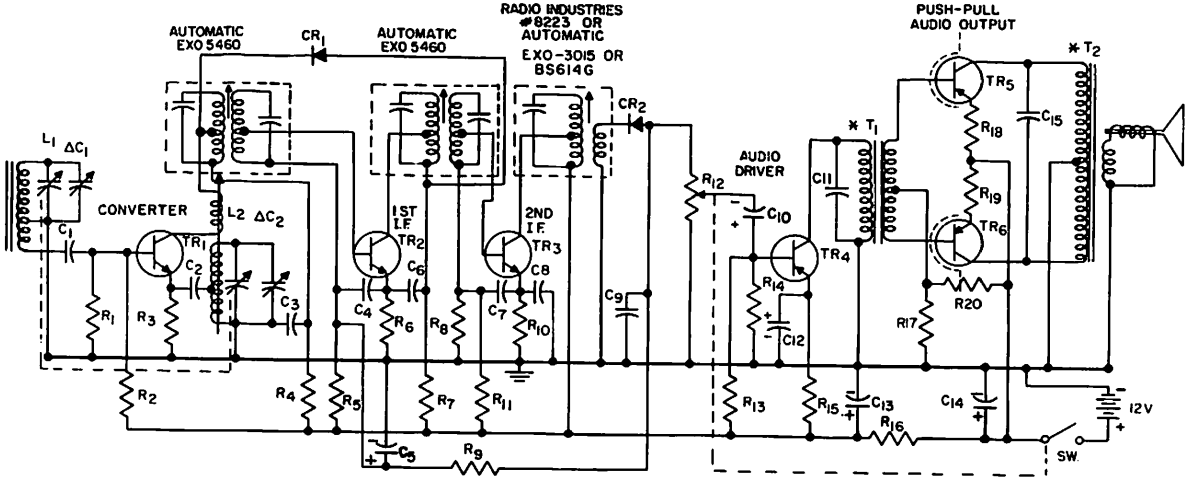
| | |
|---|---|
| * $L_1$ | 435μh ±10% |
| * $L_2$ | 250μh ±10% |
| $CR_1, CR_2$ | DR117, IN64G, OR CK706A OR EQUIV. |
| * $\Delta C_1$ — 190.6<br>* $\Delta C_2$ — 89.3 | R/C MODEL 242 |

NOMINAL SENSITIVITY = 200 MICROVOLTS / METER
(MEASURED WITH 50 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT .6 WATTS.
SELECTIVITY AT −6db : 8.0 KC/S
SELECTIVITY AT −60db : 60.0 KC/S
ZERO SIGNAL BATTERY DRAIN 7.0 MILLIAMPS.

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 154

**SIX TRANSISTOR NINE VOLT BROADCAST RECEIVER**

**Figure 10.15**




| | |
|---|---|
| $R_1, R_{11}$ | 6800 OHM |
| $R_2$ | 33,000 OHM |
| $R_3$ | 1500 OHM |
| $R_4, R_{10}, R_{15}$ | 470 OHM |
| $R_5$ | 100,000 OHM |
| $R_6$ | 330 OHM |
| $R_7, R_{13}$ | 4700 OHM |
| $R_8$ | 2200 OHM |
| $R_9$ | 2,700 OHM |
| $R_{12}$ | VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER |
| $R_{14}$ | 15,000 OHM |
| $R_{16}$ | 220 OHM |
| $R_{17}$ | 2700 OHM |
| $R_{18}, R_{19}$ | 10 OHM |
| $R_{20}$ | 33 OHM |

| | |
|---|---|
| $C_1$ | .02 μfd |
| $C_2, C_3$ | .01 μfd |
| $C_4, C_6, C_7, C_8$ | .1 μfd |
| $C_5$ | 6 μfd, 12V |
| $C_9$ | .05 μfd |
| $C_{10}$ | 6 μfd, 6V |
| $C_{11}$ | .003 μfd |
| $C_{12}, C_{13}, C_{14}$ | 50 μfd, 12V |
| $C_{15}$ | .2 μfd |
| $TR_1$ | G.E. 2N1087 CONVERTER |
| $TR_2$ | G.E. 2N293 IST I.F. |
| $TR_3$ | G.E. 2N169 OR 2N1121 2ND I.F. |
| $TR_4$ | G.E. 2N324 DRIVER |
| $TR_5, TR_6$ | G.E. 2N1415 AUDIO WITH CLIP-ON HEAT SINK (BIRCHER 3AL635-2R OR EQUIV.) |

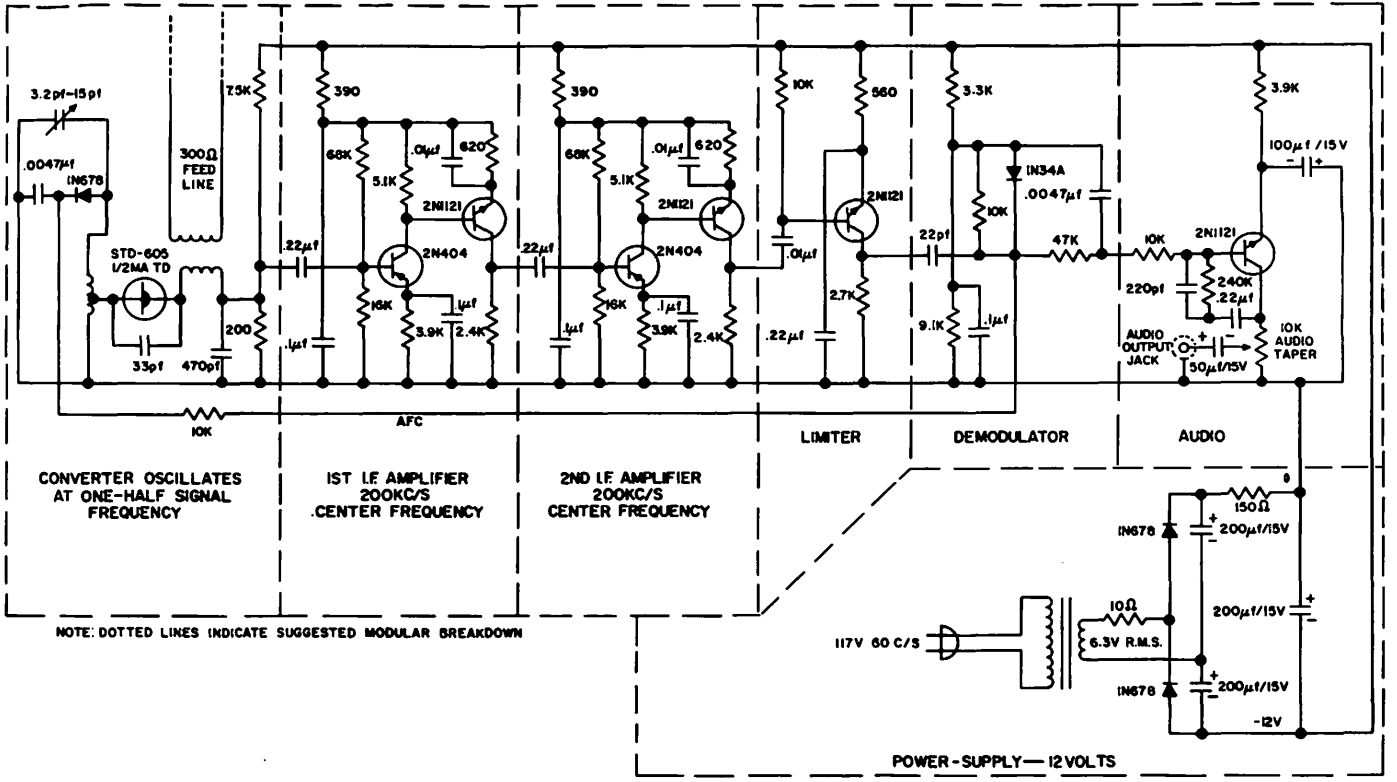
| | |
|---|---|
| * $T_1$ | 2000/2600 CT. |
| * $T_2$ | 200Ω CT/VC |
| $L_1$ | 435 μh ± 10% |
| $L_2$ | 250 μh ± 10% |
| $\Delta C_1$ — 190.6<br>$\Delta C_2$ — 89.3 | R/C MODEL 242 |
| $CR_1, CR_2$ | IN64 OR IN295 OR EQUIV. |

NOMINAL SENSITIVITY : 150 MICROVOLTS/METER
(MEASURED WITH 50 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT : 1 WATT
SELECTIVITY AT -6db : 8.0 KC/S
SELECTIVITY AT -60db : 38.0 KC/S
ZERO SIGNAL BATTERY DRAIN : 10 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 154

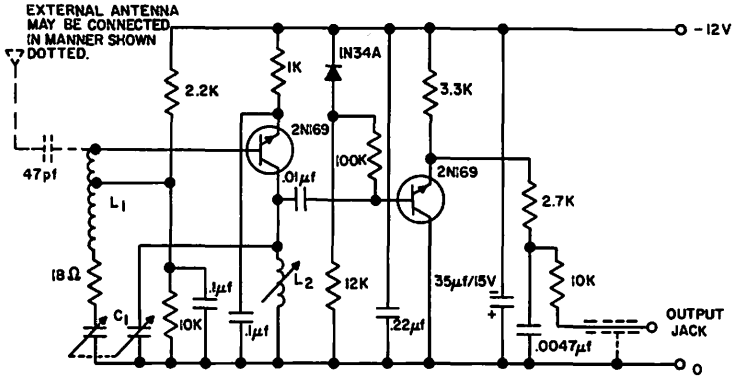
**SIX TRANSISTOR, 12 VOLT 1 WATT RECEIVER**

**Figure 10.16**




FM TUNER

**Figure 10.17**




**AM TUNER**

**Figure 10.18**

## ADDITIONAL COMPONENT INFORMATION

### TRANSFORMERS

The audio transformers used in these diagrams were wound on laminations of 1⅝" by 1⅜" and a ½" stack size, and having an electrical efficiency of about 80%. Smaller or less efficient transformers will degrade the electrical fidelity of the circuits.

### OSCILLATOR COIL

Ed Stanwyck Coil Company #1265

### VARIABLE CONDENSER

Radio Condenser Company Model 242

The receiver circuits shown in Figures 10.1, 10.12, 10.13, 10.14, 10.15, and 10.16 have been designed to give optimum performance with the components specified. Readers wishing to construct any of these receivers may obtain all standard components from local or national electronic parts distributors. If difficulty is encountered in obtaining the more special parts such as ganged tuning capacitors, r.f. and oscillator coils, or i.f., interstage, and audio transformers, the reader should make inquiry of

Jonec-K Company
Box 346
North Syracuse 14, New York

# BASIC COMPUTER CIRCUITS

CHAPTER 11

Computers are generally classified as either analog or digital. An example of an analog computer is the slide rule where the numerical values involved in the calculations are represented by the distance along the scales of the slide rule. For the slide rule, distance is the analog of the numerical values. In an electronic analog computer the voltage or current in the circuit is used as the analog of the numerical values involved in the calculation. Analog computers are used primarily in cases where minimum cost is important and high accuracy is not required.

In a digital computer the numerical values change in discrete steps rather than continuously as in an analog computer. An example of a digital computer is the ordinary desk calculator or adding machine. In an electronic digital computer numerical values involved in the calculation are represented by the discrete states of flip-flops and other switching circuits in the computer. Numerical calculations are carried out in digital computers according to the standard rules of addition, subtraction, multiplication and division. Digital computers are used primarily in cases where high accuracy is required such as in standard accounting work. For example, most desk calculators are capable of giving answers correct to one part in one million, but a slide rule (analog computer) would have to be about ⅛ of a mile long to be read to the same accuracy.

The transistor's small size, low power requirements and inherent reliability have resulted in its extensive use in digital computers. Special characteristics of the transistor such as low saturation resistance, low input impedance, and complementary NPN and PNP types, have permitted new types of digital circuits which are simple, efficient and fast. Computers operating at speeds of 5 megacycles are a commercial reality, and digital circuits have been proved feasible at 160 megacycles.

This chapter offers the design engineer practical basic circuits and design procedures based on proven techniques and components. Flip-flops are discussed in detail because of their extensive use in digital circuits.

## FLIP-FLOP DESIGN PROCEDURES

### SATURATED FLIP-FLOPS

The simplest flip-flop possible is shown in Figure 6.21, however, for standard transistor types the circuit in Figure 11.1(A) is preferable at moderate temperatures. We shall refer to the conducting and non-conducting transistors as the on and off

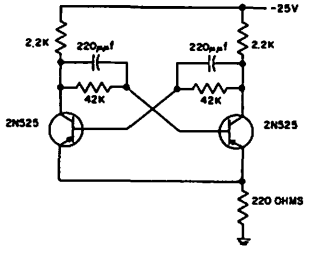



Figure 11.1 (A)

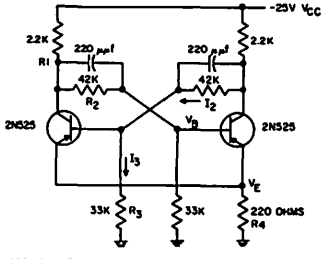
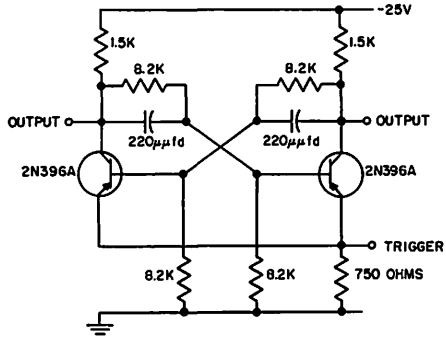



Figure 11.1 (B)

SATURATED FLIP-FLOPS

transistors respectively. For stability, the circuit depends on the low collector to emitter voltage of the saturated on transistor to reduce the base current of the off transistor to a point where the circuit gain is too low for regeneration. The 220Ω emitter resistor can be removed if emitter triggering is not used. By adding resistors from base to ground as in Figure 11.1(B), the off transistor has both junctions reverse biased for greater stability. While the 33K resistors divert some of the formerly available base current, operation no longer depends on a very low saturation voltage consequently less base current may be used. Adding the two resistors permits stable operation beyond 50°C ambient temperature.




**SATURATED FLIP-FLOP**

**Figure 11.1 (C)**

The circuit in Figure 11.1(C) is stabilized to 100°C. The price that is paid for the stability is (1) smaller voltage change at the collector, (2) more battery power consumed, (3) more trigger power required, (4) a low $I_{CO}$ transistor must be used. The capacitor values depend on the trigger characteristics and the maximum trigger repetition rate as well as on the flip-flop design.

By far, the fastest way to design saturating flip-flops is to define the collector and emitter resistors by the current and voltage levels generally specified as load requirements. Then assume a tentative cross-coupling network. With all components specified, it is easy to calculate the on base current and the off base voltage. For example, the circuit in Figure 11.1(B) can be analyzed as follows. Assume $V_{BE} = .3$ volt and $V_{CE} = .2$ volt when the transistor is on. Also assume that $V_{EB} = .2$ volts will maintain the off transistor reliably cut-off. Transistor specifications are used to validate the assumptions.

I. Check for the maximum temperature of stability.

$$V_E = \frac{R_4 V_{CC}}{R_1 + R_4} = \frac{220}{2200 + 220}(25) = 2.3 \text{ volts}$$

$$V_{C\,on} = V_E + V_{CE\,on} = 2.3 + .2 = 2.5 \text{ volts}$$

Assuming no $I_{CO}$, the base of the off transistor can be considered connected to a potential,

$$V'_B = V_{C\,on}\frac{R_3}{R_2 + R_3} \text{ through a resistor } R'_B = \frac{R_2 R_3}{R_2 + R_3}$$

$$V'_B = \frac{(2.5)(33K)}{(42K + 33K)} = 1.1 \text{ volts}$$

$$R'_B = \frac{(33K)(42K)}{75K} = 18.5K$$

The $I_{CO}$ of the off transistor will flow through $R'_B$ reducing the base to emitter potential. If the $I_{CO}$ is high enough, it can forward bias the emitter to base junction causing the off transistor to conduct. In our example, $V_E = 2.3$ volts and $V_{EB} = .2$ volts will maintain off conditions. Therefore, the base potential can rise from 1.1 volts to 2.1 volts (2.3 — .2) without circuit malfunction. This potential is developed across $R'_B$ by $I_{CO} = \frac{2.1 - 1.1}{18.5K} = 54\ \mu a$. A germanium transistor with $I_{CO} = 10\ \mu a$ at 25°C will not exceed 54 $\mu a$ at 50°C. If a higher operating temperature is required, $R_2$ and $R_3$ may be decreased and/or $R_4$ may be increased.

II. Check for sufficient base current to saturate the on transistor.

$$V_{B\,on} = V_E + V_{BE\,on} = 2.3 + .3 = 2.6 \text{ volts}$$

The current through $R_3 = I_3 = \frac{2.6v}{33K} = .079$ ma

The current through $R_1$ and $R_2$ in series is $I_2 = \frac{V_{CC} - V_{B\,on}}{R_1 + R_2} = \frac{25 - 2.6}{42K + 2.2K} = .506$ ma

The available base current is $I_B = I_2 - I_3 = .43$ ma

The collector current is $I_C = \frac{V_{CC} - V_{C\,on}}{R_1} = \frac{25 - 2.5}{2.2K} = 10.25$ ma

The transistor will be in saturation if $h_{FE}$ at 10 ma is greater than

$$\frac{I_C}{I_B} = \frac{10.25}{.43} = 24$$

If this circuit were required to operate to —55°C, allowance must be made for the reduction of $h_{FE}$ at low temperatures. The minimum allowable room temperature $h_{FE}$ should be 50% higher or $h_{FE\,min} = 36$.

Generally it is not necessary to include the effect of $I_{CO}$ flowing through $R_1$ when calculating $I_2$ since at temperatures where $I_{CO}$ subtracts from the base drive it simultaneously increases $h_{FE}$. If more base drive is required, $R_2$ and $R_3$ may be decreased. If their ratio is kept constant, the off condition will not deteriorate, and so need not be rechecked.

III. Check transistor dissipation to determine the maximum junction temperature.

The dissipation in the on transistor is

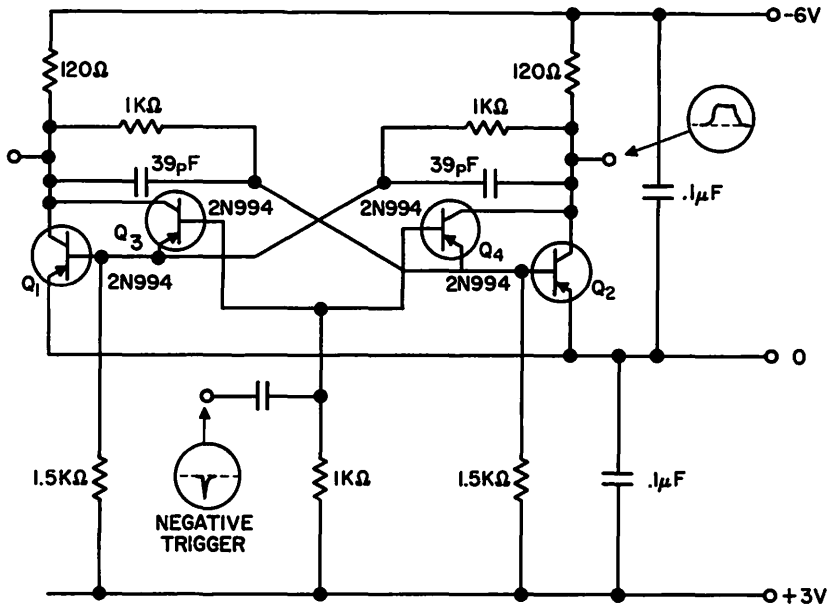
$$V_{BE\,on}\, I_B + V_{CE\,on}\, I_C = \frac{(.3)(.43)}{1000} + \frac{(.2)(10.25)}{1000} = 2.18 \text{ mw}$$

The dissipation in the off transistor resulting from the maximum $I_{CO}$ is

$$V_{CB} I_{CO} \approx \frac{(25)(55)}{10^6} = 1.4 \text{ mw}$$

Generally the dissipation during the switching transient can be ignored at speeds justifying saturated circuitry. In both transistors the junction temperature is within 1°C of the ambient temperature if transistors in the 2N394-97 or 2N524-27 series are used.

A saturated flip-flop using 2N994 germanium epitaxial transistors is shown in Figure 11.1(D). This flip-flop is capable of 30 mcs operation with a typical transition time of 10 nanoseconds. In this circuit $Q_1$ and $Q_2$ form the usual flip-flop configuration. However, the trigger input is steered through either $Q_3$ or $Q_4$ whose gain is used to quickly saturate $Q_1$ or $Q_2$, whichever is in the "off" state. Simultaneously it is ensured that the cross-coupling capacitors are discharged to their rest potentials in the shortest possible time. For those flip-flop circuit applications not requiring the speed of the 2N994 circuit, 2N781 transistors may be used.

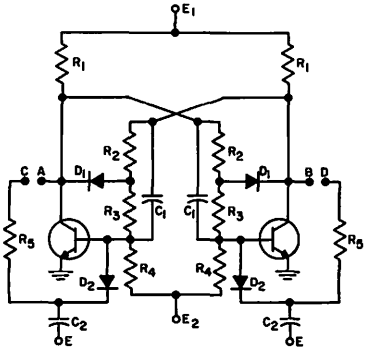



**30 MEGACYCLE SATURATED FLIP-FLOP**

**Figure 11.1 (D)**

## NON-SATURATED FLIP-FLOP DESIGN

The abundance of techniques to prevent saturation makes a general design procedure impractical if not impossible. While it is a simple matter to design a flip-flop as shown above, it becomes quite tedious to check all the worst possible combinations of component change to ensure manufacturability and long term reliability. Often the job is assigned to a computer which calculates the optimum component values and tolerances. While a number of flip-flop design procedures have been published, they generally make simplifying assumptions concerning leakage currents and the voltages developed across the conducting transistors.



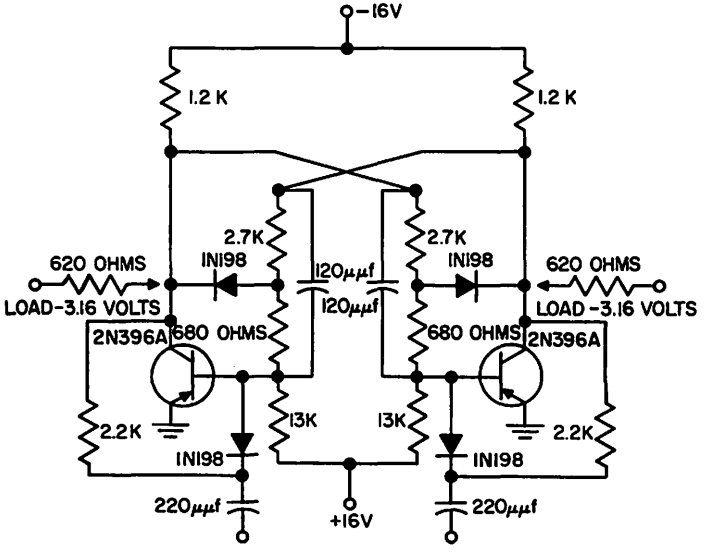

CIRCUIT CONFIGURATION FOR NON-SATURATING FLIP-FLOP DESIGN PROCEDURE

Characteristics:

- Trigger input at points E
- Trigger steering by $D_2$ and $R_5$
- Collector clamping by $D_1$ and $R_5$
- Connect points A, B, C, D, E as shown in Figure 11.3 to get counter or shift register operation
- C1 and C2 chosen on basis of speed requirements

**Figure 11.2 (A)**

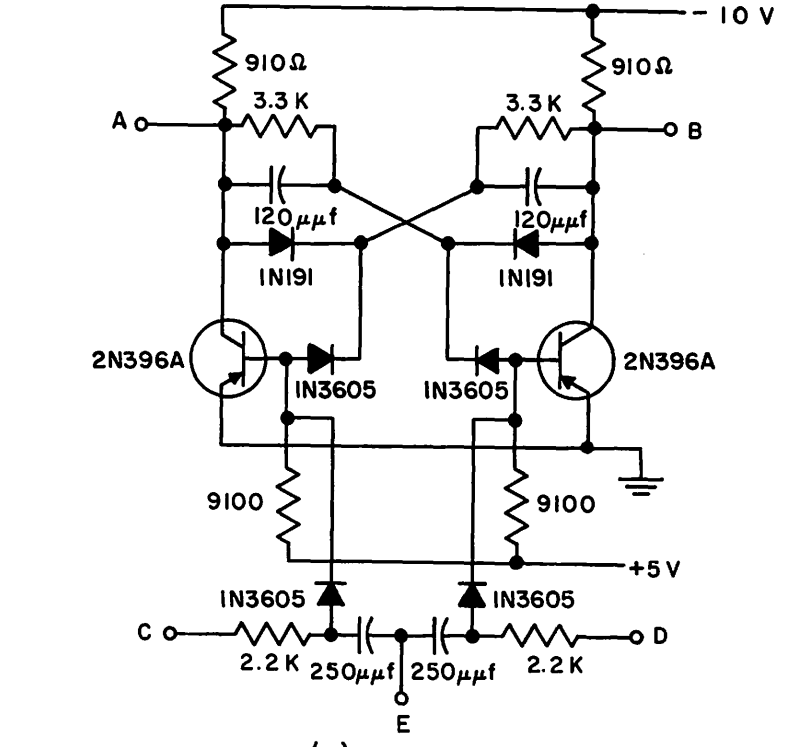
The design procedure described here is for the configuration in Figure 11.2(A). No simplifying assumptions are made but all the leakage currents and all the potentials are considered. The design makes full allowance for component tolerances, voltage fluctuations, and collector output loading. The anti-saturation scheme using one resistor (R3) and one diode (D1) was chosen because of its effectiveness, low cost and simplicity. The trigger gating resistors (R5) may be returned to different collectors to get different circuit functions as shown in Figure 11.3. This method of triggering offers the trigger sensitivity of base triggering and the wide range of trigger amplitude permissible in collector triggering. The derivation of the design procedure would require much space, therefore for conciseness, the procedure is shown without any substantiation. The procedure involves defining the circuit requirements explicitly then determining the transistor and diode characteristics at the anticipated operating points. A few astute guesses of key parameters yield a fast solution. However, since the procedure deals with only one section of the circuit at a time, a solution is readily reached by cut and try methods without recourse to good fortune. A checking procedure permits verification of the calculations. The symbols used refer to Figure 11.2(A) or in some cases are used only to simplify calculations. A bar over a symbol denotes its maximum value; a bar under it, its minimum. The example is based on polarities associated with NPN transistors for clarity. The result is that only $E_2$ is negative. While the procedure is lengthly, its straightforward steps lend themselves to computation by technically unskilled personnel and the freedom from restricting assumptions guarantees a working circuit when a solution is reached. A circuit designed by this procedure is shown in Figure 11.2(B).



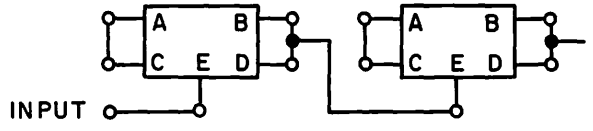

**NON-SATURATED FLIP-FLOP**

**Figure 11.2 (B)**

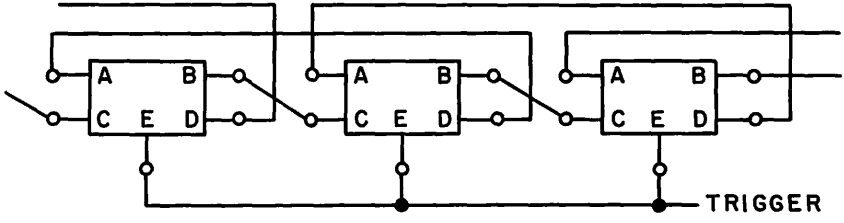
The same procedure can be used to analyze existing flip-flops of this configuration by using the design check steps.




(a) FLIP—FLOP




(b) INTER CONNECTION AS COUNTER




(c) INTERCONNECTION AS SHIFT REGISTER

**500 KC COUNTER-SHIFT REGISTER FLIP-FLOP**

**Figure 11.3**

## NON-SATURATING FLIP-FLOP DESIGN PROCEDURE

| STEP | DEFINITION OF OPERATION | SYMBOL | SAMPLE DESIGN FOR 2N396 TRANSISTOR |
|---|---|---|---|
| *(A)* | *Circuit Requirements and Device Characteristics* | | |
| 1 | Assume maximum voltage design tolerance | $\Delta e$ | Let $\Delta e = \pm 5\%$ |
| 2 | Assume maximum resistor design tolerance | $\Delta r$ | Let $\Delta r = \pm 7\%$ (assuming $\pm 5\%$ resistors) |
| 3 | Assume maximum ambient temperature | $T_A$ | Let $T_A = 40°C$ |
| 4 | Assume maximum load current out of the off side | $I_0$ | Let $I_0 = 1$ ma |
| 5 | Assume maximum load current into the on side | $I_1$ | Let $I_1 = 0.2$ ma |
| 6 | Estimate the maximum required collector current in the on transistor | $I_1$ | Let $I_1 \leq 17.5$ ma |
| 7 | Assume maximum design $I_{CO}$ at 25°C | | From spec sheet $I_{CO} < 6\ \mu a$ |
| 8 | Estimate the maximum junction temperature | $T_J$ | Let $T_J = 60°C$ |
| 9 | Calculate $I_{CO}$ at $T_J$ assuming $I_{CO}$ doubles every 10°C or $I_{CO_{T_J}} = I_{CO_{25}} e^{.07(T_J-25)}$ | $I_2$ | $I_2 = 6e^{.07T_J} = 71\ \mu a$; Let $I_2 = 100\ \mu a$ |
| 10 | Assume the maximum base leakage current is equal to the maximum $I_{CO}$ | $I_3$ | Let $I_3 = 100\ \mu a$ |
| 11 | Calculate the allowable transistor dissipation | | 2N396 is derated at 3.3 mw/°C. The junction temperature rise is estimated at 20°C therefore 67 mw can be allowed. Let $P_C = 67$ mw |
| 12 | Estimate $h_{FE}$ minimum taking into account low temperature degradation and specific assumed operating point | $\beta_{min}$ | Let $\alpha_{min} = 0.94$ or $\beta_{min} = 15.67$ |
| 13 | Estimate the maximum design base to emitter voltage of the "on" transistor | $V_1$ | Let $V_1 = 0.35$ volts |
| 14 | Assume voltage logic levels for the outputs | | Let the level separation be $\geq 7$ volts |

## NON-SATURATING FLIP-FLOP DESIGN PROCEDURE (CONTINUED)

| STEP | DEFINITION OF OPERATION | SYMBOL | SAMPLE DESIGN FOR 2N396 TRANSISTOR |
|---|---|---|---|
| 15 | Choose the maximum collector voltage permissible for the "on" transistor | $V_2$ | Let $V_2 \leq 2.0$ volts |
| 16 | Choose suitable diode types | | Let all diodes be 1N198 |
| 17 | Estimate the maximum leakage current of any diode | $I_4$ | Maximum leakage estimated as $\leq 25$ $\mu$a. Let $I_4 = 40$ $\mu$a at end of life |
| 18 | Calculate $I_5 = I_3 + I_4$ | $I_5$ | $40 + 100 = 140$ $\mu$a |
| 19a | Choose the minimum collector voltage for the "off" transistor keeping in mind 14 and 15 above | $V_3$ | Let $V_3 \geq 9.0$ volts |
| 19b | Choose the maximum collector voltage for the "off" transistor | $V_4$ | Let $V_4 \leq 13.0$ volts |
| 20 | Choose the minimum design base to emitter reverse bias to assure off conditions | $V_5$ | Let $V_5 = 0.5$ volt |
| 21a | Estimate the maximum forward voltage across the diodes | $V_6$ | Let $V_6 = 0.8$ volt |
| 21b | Estimate the minimum forward voltage | $V_7$ | Let $V_7 = 0.2$ volt |
| 22 | Estimate the worst saturation conditions that can be tolerated. | | |
| 22a | Estimate the minimum collector voltage that can be tolerated | $V_8$ | Let $V_8 = 0.1$ volt |
| 22b | Estimate the maximum base to collector forward bias voltage that can be tolerated | $V_9$ | Let $V_9 = 0.1$ volt |
| 23a | Calculate $V_2 + V_7$ | $V_{10}$ | $2 + 0.2 = 2.2$ volts |
| 23b | Calculate $V_2 + V_6$ | $V_{11}$ | $2 + 0.8 = 2.8$ volts |
| 24a | Calculate $V_8 + V_7$ | $V_{12}$ | $0.1 + 0.2 = 0.3$ volt |

| STEP | DEFINITION OF OPERATION | SYMBOL | SAMPLE DESIGN FOR 2N396 TRANSISTOR |
|---|---|---|---|
| 24b | Calculate $V_8 + V_6$ | $V_{13}$ | $0.1 + 0.8 = 0.9$ volt |
| 25 | Calculate $V_8 + V_9$ | $V_{14}$ | $0.1 + 0.1 = 0.2$ volt |
| *(B)* | *Cut and Try Circuit Design* | | |
| 1 | Assume $E_2$ | $E_2$ | Let $E_2 = -16$ volts $\pm$ 5%; $\overline{E_2} = -15.2$ v; $\underline{E_2} = -16.8$ v |
| 2a | Calculate $\frac{(1 + \Delta r)}{(1 - \Delta r)}$ | $K_1$ | $\frac{1.07}{0.93} = 1.15$ |
| 2b | Calculate $\frac{(1 + \Delta e)}{(1 - \Delta e)}$ | $K_2$ | $\frac{1.05}{0.95} = 1.105$ |
| 2c | Calculate $\frac{I_1}{\beta_{min}}$ | $K_3$ | $\frac{17.5}{15.67} = 1.117$ ma |
| 2d | Calculate $I_2 + I_0 + 2I_4$ | $K_4$ | $0.1 + 1.0 + 0.08 = 1.18$ ma |
| 2e | Calculate $\frac{V_6 - V_9}{V_8 + V_9 - \overline{E_2}}$ | $K_5$ | $\frac{0.8 - 0.1}{0.1 + 0.1 + 15.2} = 0.0454$ volts |
| 3 | Calculate $\overline{R_4} \leq \frac{1}{K_3}\left[\frac{V_{10} - V_1}{K_1 K_5} - K_1 (V_1 - \underline{E_2})\right]$ | | $\frac{1}{1.117}\left[\frac{2.2 - 0.35}{(1.15)(0.0454)} - 1.15 (0.35 + 16.8)\right] = 14.03$ K |
| 4 | Choose $R_4$ | $R_4$ | Let $R_4 = 13$K $\pm$ 7%; $\overline{R_4} = 13.91$ K; $\underline{R_4} = 12.09$ K |
| 5 | Calculate $\underline{R_3} \geq K_5 \overline{R_4}$ | | $(0.0454)(13.91\text{K}) = 0.632$ K |
| 6 | Choose $R_3$ | $R_3$ | Let $R_3 = 0.68$ K $\pm$ 7%; $\overline{R_3} = 0.7276$ K; $\underline{R_3} = 0.6324$ K |
| 7 | Check $R_3$ by calculating $\overline{R_3} \leq \frac{\underline{R_4} (V_{10} - V_1)}{V_1 - \underline{E_2} + K_3 \underline{R_4}}$ | | $\frac{(12.09\text{ K})(2.2 - 0.35)}{0.35 + 16.8 + (1.117)(12.09)} = 0.730$ K; choice of $R_3$ satisfactory |
| 8 | Calculate $\frac{\overline{R_4}}{-V_8 - \overline{E_2} - I_8 \overline{R_4}}$ | $K_6$ | $\frac{13.91\text{ K}}{-0.5 + 15.2 - (0.14)(13.91)} = 1.091$ K/V |

## NON-SATURATING FLIP-FLOP DESIGN PROCEDURE (CONTINUED)

| STEP | DEFINITION OF OPERATION | SYMBOL | SAMPLE DESIGN FOR 2N396 TRANSISTOR |
|---|---|---|---|
| 9 | Calculate $\underline{R_2} \geq \frac{K_6 (V_2 + V_5) - \underline{R_3}}{1 - K_6 I_4}$ | | $\frac{(1.091)\,(2.0 + 0.5)\text{ K} - 0.632\text{ K}}{1 - (1.091)\,(0.04)} = 2.19\text{ K}$ |
| 10 | Choose $R_2$ — *If there are difficulties at this point, assume a different* $E_2$. | $R_2$ | Let $R_2 = 2.7\text{ K} \pm 7\%$; $\overline{R_2} = 2.889\text{ K}$; $\underline{R_2} = 2.511\text{ K}$ |
| 11 | Calculate $\frac{K_1^2 [V_3 - V_{12} + K_4 \underline{R_2}]}{V_4 - V_{11}}$ | $K_7$ | $\frac{(1.15)^2[9.0 - 0.3 + (1.18)\,(2.511)]}{13.0 - 2.8} = 1.51$ |
| 12 | Calculate $\overline{E_1} \leq \frac{K_7 V_4 - V_3}{K_7 - 1/K_2}$ | | $\frac{(1.51)\,(13.0) - 9.0}{1.51 - 1/1.105} = 17.63$ |
| 13 | Choose $E_1$ | $E_1$ | Let $E_1 = 16$ volts $\pm 5\%$; $\overline{E_1} = 16.8$ volts; $\underline{E_1} = 15.2$ volts |
| 14 | Calculate $\overline{R_1} \leq \frac{(E_1 - V_3)\,\underline{R_2}}{V_3 - V_{12} + K_4 \underline{R_2}}$ | | $\frac{(15.2 - 9.0)\,(2.511)}{9.0 - 0.3 + (1.18)\,(2.511)} = 1.335\text{ K}$ |
| 15 | Calculate $\underline{R_1} \geq \frac{(\overline{E_1} - V_4)\,(\overline{R_2})}{V_4 - V_{11}}$ | | $\frac{(16.8 - 13.0)\,(2.889)}{13.0 - 2.8} = 1.077\text{ K}$ |
| 16 | Choose $R_1$ | $R_1$ | Let $R_1 = 1.2\text{ K} \pm 7\%$; $\overline{R_1} = 1.284\text{ K}$; $\underline{R_1} = 1.116\text{ K}$ |
| *(C)* | *Design Checks* | | |
| 1 | Check "off" stability. Reverse bias voltage is given by: $V_{EB} \leq \overline{E_2} + \frac{\overline{R_4}}{\overline{R_4} + \underline{R_3} + \underline{R_2}} [V_2 - \overline{E_2} + I_4 \underline{R_2} + I_5 (\underline{R_2} + \underline{R_3})]$ Circuit stable if $V_{EB} \leq -V_5$ | $V_{EB}$ | $-15.2 + \frac{13.91}{17.05}$ $[2 + 15.2 + (0.04)\,(2.511) + (0.14)\,(3.14)] = -0.7$ volts The design value of $V_5$ was 0.5 volts. Therefore, the "off" condition is stable. |

| STEP | DEFINITION OF OPERATION | SYMBOL | SAMPLE DESIGN FOR 2N396 TRANSISTOR |
|---|---|---|---|
| 2 | Check for non-saturation under the worst conditions.<br>$V_{BE} \leq \overline{E_2} + \dfrac{\overline{R_4}\,(V_{12} - \overline{E_2})}{\overline{R_4} + \underline{R_3}}$<br>Circuit non-saturated if $V_{BE} \leq V_{14}$ | $V_{BE}$ | $-15.2 + \dfrac{13.91\,(0.9 + 15.2)}{14.54} = 0.19$ volts<br>The design maximum of $V_{14}$ was 0.2 volts. |
| 3<br>3a | Check for stability. Calculate:<br>$R_A = \overline{R_1} + \overline{R_2}$ | $R_A$ | $1.284 + 2.889 = 4.173$ K |
| 3b | $R_B = \overline{R_1} + \overline{R_2} + \overline{R_3} + \underline{R_4}$ | $R_B$ | $1.284 + 2.889 + .728 + 12.09 = 16.99$ K |
| 3c | $R_C = \overline{R_2} + \underline{R_4}$ | $R_C$ | $.728 + 12.09 = 12.82$ K |
| 3d | $E'_1 = \underline{E_1} - K_4\,\overline{R_1}$ | $E'_1$ | $15.2 - (1.18)\,(1.284) = 13.68$ volts |
| 3e | $R_D = \underline{R_1} + \overline{R_2} + \overline{R_3} + \overline{R_4}$ | $R_D$ | $1.116 + 2.889 + .728 + 13.91 = 18.643$ K |
| 3f | $I_6 = \dfrac{R_D\,(\overline{E_1} - V_2) - \underline{R_1}\,[\overline{E_1} - \underline{E_2} - I_5\,\overline{R_4} - I_4\,(\overline{R_3} + \overline{R_4})]}{\underline{R_1}\,(R_D - \underline{R_1})}$ | $I_6$ | $\dfrac{18.64\,(16.8 - 2) - 1.116\,[16.8 + 16.8 - (0.14)\,(13.91)}{1.116\,(18.64 - 1.116)}$<br>$\dfrac{-(.04)\,(.728 + 13.91)]}{} = 12.34$ ma |
| 3g | $I_7 = \dfrac{R_B}{R_A R_C}\,(E'_1 - V_{10}) - \dfrac{1}{R_C}\,(E'_1 - \underline{E_2})$ | $I_7$ | $\dfrac{16.99}{(4.173)\,(12.82)}(13.68 - 2.2) - \dfrac{(13.68 + 16.8)}{12.82} = 1.266$ ma |
| 3h | $I_8 = \dfrac{I_1 + I_6 + I_7}{\beta_{min} + \underline{R_4}/R_C}$ | $I_8$ | $\dfrac{0.2 + 12.34 + 1.266}{15.67 + 12.09/12.82} = 0.831$ ma |
| 3i | $V'_{BE} = \underline{E_2} + \dfrac{\underline{R_4}}{R_B}\left(1 + \dfrac{R_A}{R_C}\right)\left(E'_1 - \underline{E_2}\right)$<br>$- \dfrac{\underline{R_4}}{R_C}\left(E'_1 - V_{10}\right) - I_5\dfrac{\underline{R_4}}{R_B}\left(\dfrac{R_A \underline{R_4}}{R_C} - R_A - \overline{R_2}\right)$ | $V'_{BE}$ | $-16.8 + \dfrac{12.09}{16.99}\left(1 + \dfrac{4.173}{12.818}\right)\left(13.683 + 16.8\right)$<br>$- \dfrac{12.09}{12.818}\left(13.683 - 2.2\right) - 0.831\dfrac{12.09}{16.99}$<br>$\left(\dfrac{(4.173)\,(12.09)}{12.818} - 4.173 - 0.7276\right) = .55$V<br>.55V is greater than $V_1 = .35$V, therefore the design is satisfactory. |

## TRIGGERING

Flip-flops are the basic building blocks for many computer and switching circuit applications. In all cases it is necessary to be able to trigger one side or the other into conduction. For counter applications, it is necessary to have pulses at a single input make the two sides of the flip-flop conduct alternately. Outputs from the flip-flop must have characteristics suitable for triggering other similar flip-flops. When the counting period is finished, it is generally necessary to reset the counter by a trigger pulse to one side of all flip-flops simultaneously. Shift registers and ring counters have similar triggering requirements.

In applying a trigger to one side of a flip-flop, it is preferable to have the trigger turn a transistor off rather than on. The off transistor usually has a reverse-biased emitter junction. This bias potential must be overcome by the trigger before switching can start. Furthermore, some transistors have slow turn on characteristics resulting in a delay between the application of the trigger pulse and the actual switching. On the other hand, since no bias has to be overcome, there is less delay in turning off a transistor. As turn-off begins, the flip-flop itself turns the other side on.

A lower limit on trigger power requirements can be determined by calculating the base charge required to maintain the collector current in the on transistor. The trigger source must be capable of neutralizing this charge in order to turn off the transistor. It has been determined that the base charge for a non-saturated transistor is approximately $Q_B = 1.22\ I_C/2\pi f_\alpha$ using the equivalent circuit approach, or $\tau_c\ I_C$ using charge parameters. The turn-off time constant is approximately $h_{FE}/2\pi f_\alpha$ or $\tau_a$. This indicates that circuits utilizing high speed transistors at low collector currents will require the least trigger power. Consequently, it may be advantageous to use high speed transistors in slow circuitry if trigger power is critical. If the on transistor was in saturation, the trigger power must also include the stored charge. The stored charge is given approximately by

$$Q_s = \frac{1}{2\pi}\left(\frac{1}{f_\alpha} + \frac{1}{f_{\alpha 1}}\right)\left(\frac{1}{1 - \alpha_N \alpha_I}\right)\left(I_{B1} - \frac{I_C}{h_{FE}}\right)$$

using the equivalent circuit approach. Using charge parameters the stored charge is approximately

$$Q_s = \tau_b \left(I_{B1} - \frac{I_C}{h_{FE}}\right)$$

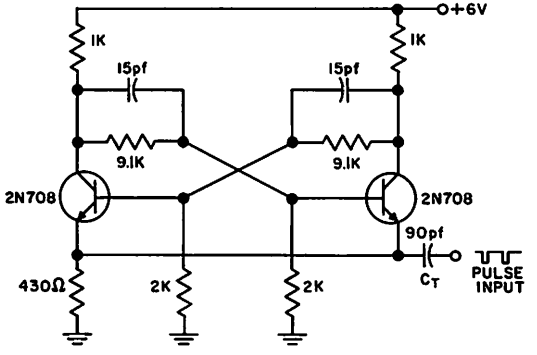
where the symbols are defined in the section on transient response time.

Generally, the trigger pulse is capacitively coupled. Small capacitors permit more frequent triggering but a lower limit of capacitance is imposed by base charge considerations. When a trigger voltage is applied, the resulting trigger current causes the charge on the capacitor to change. When the change is equal to the base charge just calculated, the transistor is turned off. If the trigger voltage or the capacitor are too small, the capacitor charge may be less than the base charge resulting in incomplete turn-off. In the limiting case $C = \frac{Q_B}{V_T}$. The speed with which the trigger turns off a transistor depends on the speed in which $Q_B$ is delivered to the base. This is determined by the trigger source impedance and $r_b'$.

In designing counters, shift registers or ring counters, it is necessary to make alternate sides of a flip-flop conduct on alternate trigger pulses. There are so-called steering circuits which accomplish this. At low speeds, the trigger may be applied at the emitters as shown in Figure 11.4. It is important that the trigger pulse be shorter

than the cross coupling time constant for reliable operation. The circuit features few parts and a low trigger voltage requirement. Its limitations lie in the high trigger current required.

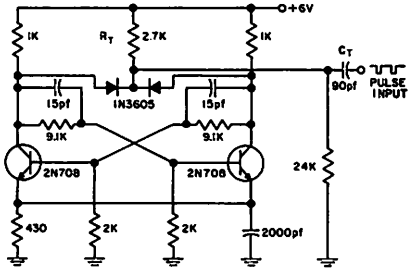
At this point, the effect of trigger pulse repetition rate can be analyzed. In order that each trigger pulse produce reliable triggering, it must find the circuit in exactly the same state as the previous pulse found it. This means that all the capacitors in the circuit must stop charging before a trigger pulse is applied. If they do not, the result is equivalent to reducing the trigger pulse amplitude. The transistor being turned off presents a low impedance permitting the trigger capacitor to charge rapidly. The capacitor must then recover its initial charge through another impedance which is generally much higher. The recovery time constant can limit the maximum pulse rate.




EMITTER TRIGGERING
MAXIMUM TRIGGER RATE EXCEEDS 2MC WITH TRIGGER AMPLITUDE FROM 4V TO 12V.

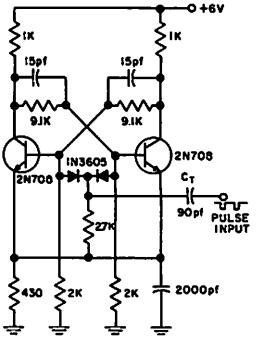
**Figure 11.4**

Steering circuits using diodes are shown in Figures 11.5 and 11.6. The collectors are triggered in 11.5 by applying a negative pulse. As a diode conducts during triggering, the trigger pulse is loaded by the collector load resistance. When triggering is accomplished, the capacitor recovers through the biasing resistor $R_T$. To minimize




COLLECTOR TRIGGERING
MAXIMUM TRIGGER RATE EXCEEDS 5MC WITH TRIGGER AMPLITUDE FROM 4V TO 12V.

**Figure 11.5**



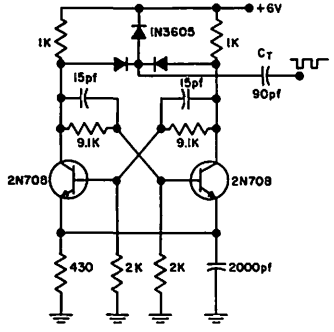

BASE TRIGGERING
MAXIMUM TRIGGER RATE EXCEEDS 5MC WITH TRIGGER AMPLITUDE FROM 0.75 TO 2 VOLTS.

**Figure 11.6**

trigger loading, $R_T$ should be large; to aid recovery, it should be small. To avoid the recovery problem mentioned above, $R_T$ can be replaced by a diode as shown in 11.7. The diode's low forward impedance ensures fast recovery while its high back impedance avoids shunting the trigger pulse during the triggering period.

Collector triggering requires a relatively large amplitude low impedance pulse but has the advantage that the trigger pulse adds to the switching collector waveform to enhance the speed. Large variations in trigger pulse amplitude are also permitted.

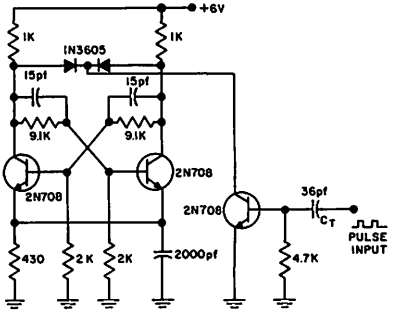
In designing a counter, it may be advantageous to design all stages identically the same to permit the economies of automatic assembly. Should it prove necessary to increase the speed of the early stages, this can be done by adding a trigger amplifier as shown in Figure 11.8 without any change to the basic stage.




COLLECTOR TRIGGERING

DIODE TO SUPPLY VOLTAGE REDUCES TRIGGER POWER AND EXTENDS MAXIMUM TRIGGER RATE.

**Figure 11.7**

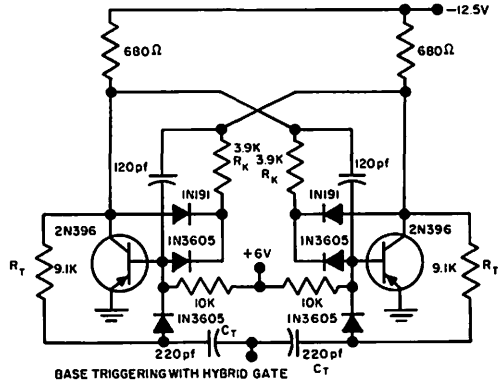



COLLECTOR TRIGGERING WITH TRIGGER AMPLIFIER

FOR IMC TRIGGER RATE LESS THAN 1 VOLT TRIGGER AMPLITUDE REQUIRED.

**Figure 11.8**

Base triggering shown in Figure 11.6 produces steering in the same manner as collector triggering. The differences are quantitative with base triggering requiring less trigger energy but a more accurately controlled trigger amplitude. A diode can replace the bias resistor to shorten the recovery time.




BASE TRIGGERING WITH HYBRID GATE

**Figure 11.9**

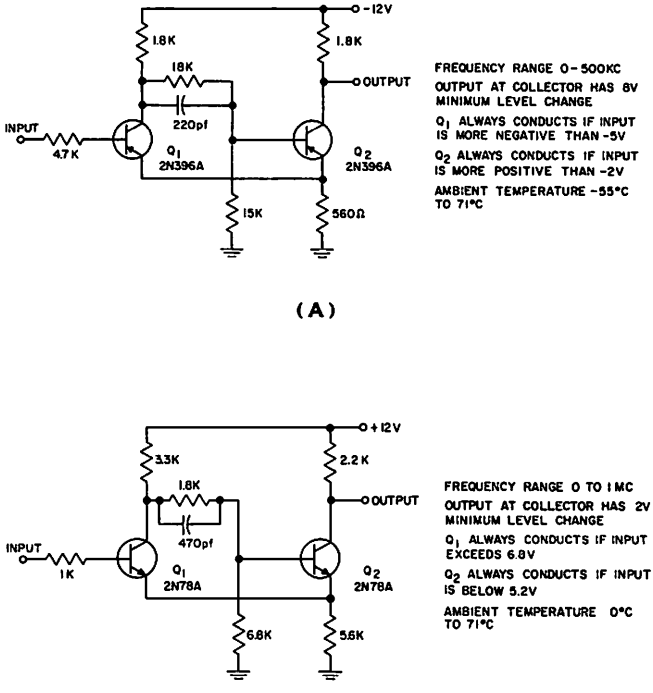
Hybrid triggering illustrated in Figure 11.9 combines the sensitivity of base triggering and the trigger amplitude variation of collector triggering. In all the other steering circuits the bias potential was fixed, in this one the bias potential varies in order to more effectively direct the trigger pulse. By returning the bias resistor to the collector the bias voltage is $V_{CB}$. For the conducting transistor, $V_{CB}$ is much less than for the off transistor, consequently, the trigger pulse is directed to the conducting transistor. This steering scheme is particularly attractive if $V_{CB}$ for the conducting transistor is very small as it is in certain non-saturating circuits such as shown in Figure 6.23.

Care should be taken that the time constant $C_T R_T$ does not limit the maximum counting rate. Generally $R_T$ can be made approximately equal to $R_K$, the cross-coupling resistor.

## SPECIAL PURPOSE CIRCUITS

### SCHMITT TRIGGER

A Schmitt trigger is a regenerative bistable circuit whose state depends on the amplitude of the input voltage. For this reason, it is useful for waveform restoration, signal level shifting, squaring sinusoidal or non-rectangular inputs, and for DC level detection. Practical circuits are shown in Figure 11.10.



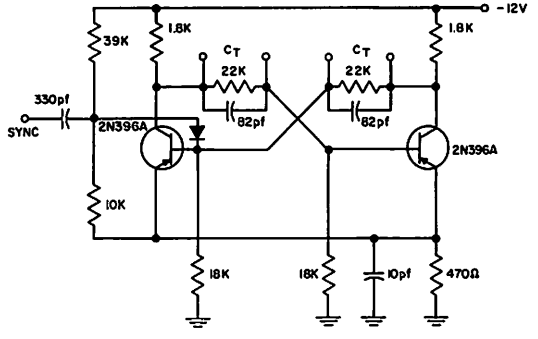

**SCHMITT TRIGGERS**

**Figure 11.10**

Circuit operation is readily described using Figure 11.10(B). Assuming Q1 is non-conducting, the base of Q2 is biased at approximately +6.8 volts by the voltage divider consisting of resistors 3.3K, 1.8K and 6.8K. The emitters of both transistors are then at 6.6 volts due to the forward bias voltage required by Q2. If the input voltage is less than 6.6 volts, Q1 is off as was assumed. As the input approaches 6.6 volts, a critical voltage is reached where Q1 begins to conduct and regeneratively turns off Q2. If the input voltage is now lowered below another critical value, Q2 will again conduct.

## ASTABLE MULTIVIBRATOR

The term multivibrator refers to a two stage amplifier with positive feedback. Thus a flip-flop is a bistable multivibrator; a "one-shot" switching circuit is a monostable multivibrator and a free-running oscillator is an astable multivibrator. The astable multivibrator is used for generating square waves and timing frequencies and for frequency division. A practical circuit is shown in Figure 11.11. The circuit is symmetrical with the transistors DC biased so that both can conduct simultaneously. The cross-coupling capacitors prevent this, however, forcing the transistors to conduct alternately. The period is approximately $T = \frac{C_T + 100}{40}$ microseconds where $C_T$ is measured in pf ($\mu\mu$f). A synchronizing pulse may be used to lock the multivibrator to an external oscillator's frequency or subharmonic.




**ASTABLE MULTIVIBRATOR**

**Figure 11.11**

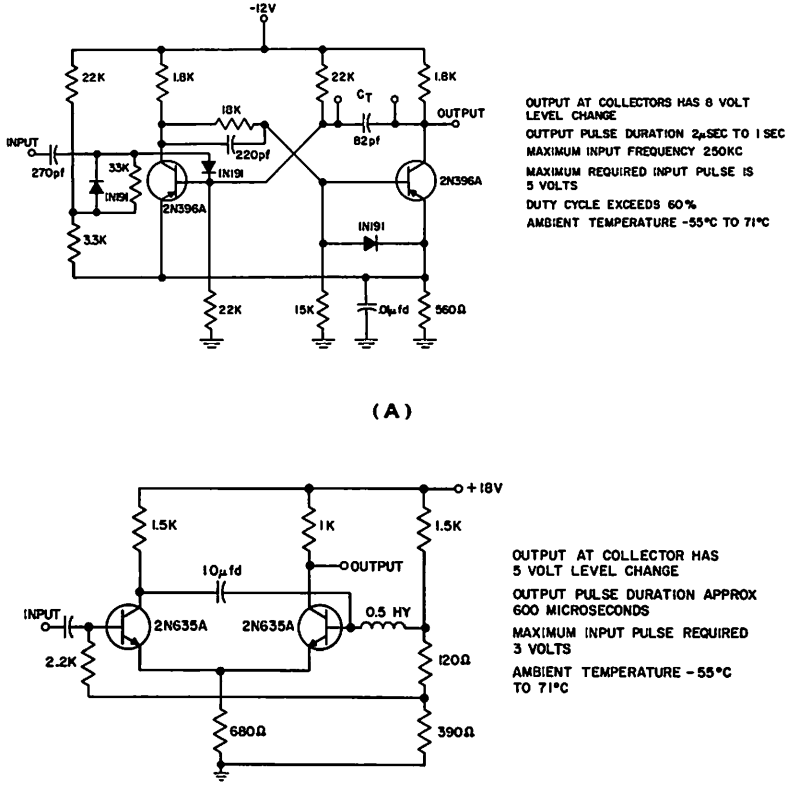
## MONOSTABLE MULTIVIBRATOR

On being triggered a monostable multivibrator switches to its unstable state where it remains for a predetermined time before returning to its original stable state. This makes the monostable multivibrator useful in standardizing pulses of random widths or in generating time delayed pulses. The circuit is similar to that of a flip-flop except that one cross-coupling network permits AC coupling only. Therefore, the flip-flop can only remain in its unstable state until the circuit reactive components discharge. Two circuits are shown in Figure 11.12 to illustrate timing with a capacitor and with an inductor. The inductor gives much better pulse width stability at high temperatures.

## INDICATOR LAMP DRIVER

The control panel of a computer frequently has indicator lamps to permit monitoring the computer's operation. The circuit in Figure 11.13 shows a bistable circuit which permits controlling the lamp by short trigger pulses.

A negative pulse at point A turns on the lamp, which remains on due to regenerative feedback in the circuit. A positive pulse at A will turn off the lamp. The use of complementary type transistors minimizes the standby power while the lamp is off.

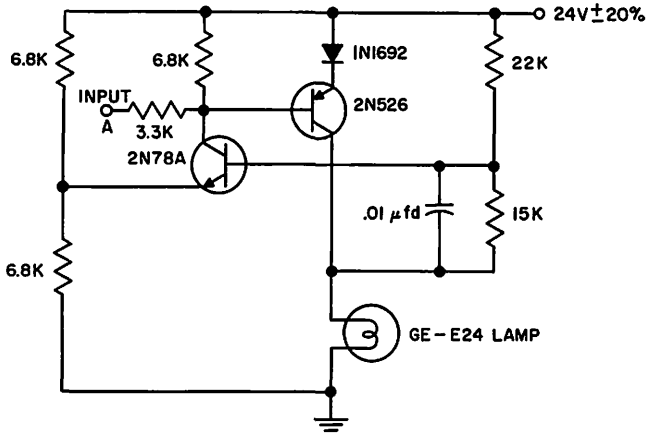



**MONOSTABLE MULTIVIBRATOR**

**Figure 11.12**

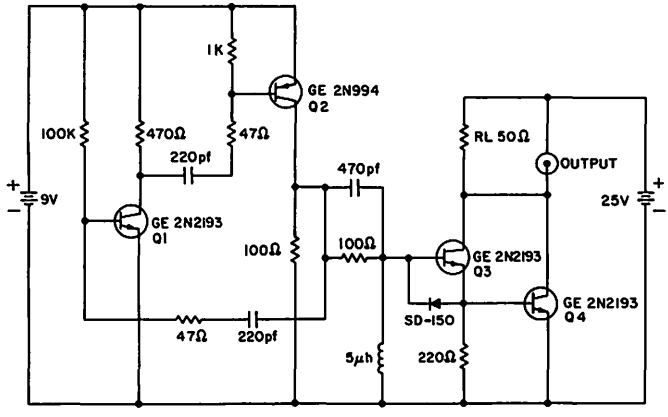
## PULSE GENERATOR

Frequently, in computer circuits a clock pulse is required to set the timing in an array of circuits. A pulse generator is shown in Figure 11.14 which delivers a very fast rise time (25 nsec.) pulse of high power. The circuit is basically composed of two parts. A multivibrator is formed by $Q_1$ and $Q_2$ and their associated circuitry and triggers the pulse generator formed by $Q_3$ and $Q_4$.




TRIGGER PULSE REQUIREMENT 2 VOLTS MAXIMUM.
AMBIENT TEMPERATURE -55°C TO 71°C
RESISTOR TOLERANCE ± 10% AT END OF LIFE.

**BISTABLE INDICATOR LAMP DRIVER**
**Figure 11.13**

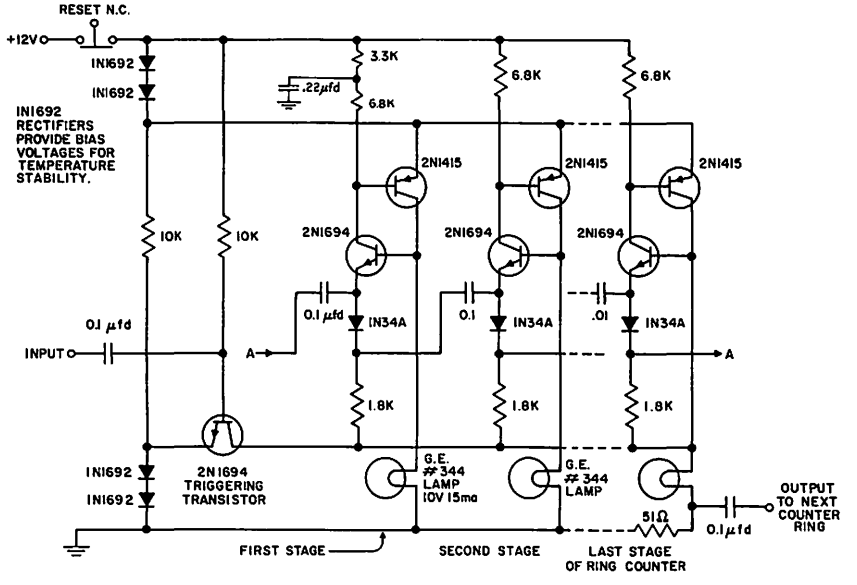



Pulse Generator Characteristics: Amplitude - 25 volts, Width - 200 nanoseconds, Rise Time - 25 nanoseconds, Fall Time - 30 nanoseconds, Impedance - 50 ohms, Repetition Rate - 100 kilocycles.

**PULSE GENERATOR WITH 0.5 AMPS. IN 25 NSEC.**
**Figure 11.14**

## RING COUNTER

The circuit of Figure 11.15 forms a digital counter or shift register with visual readout. The circuit operates from a 12 volt source and uses six components per stage. The counter and indicator functions are combined to insure low battery drain. The .22 μfd capacitor ensures that the first stage turns on after the reset button is released. No current is drawn by the stages except when a lamp is on. As many stages as desired may be included in a ring.




**RING COUNTER WITH VISUAL READOUT**

**Figure 11.15**

# LOGIC

CHAPTER 12

Large scale scientific computers, smaller machine control computers and electronic animals all have in common the facility to take action without any outside help when the situation warrants it. For example, the scientific computer recognizes when it has completed an addition, and tells itself to go on to the next part of the problem. A machine control computer recognizes when the process is finished and another part should be fed in. Electronic animals can be made to sense obstructions and change their course to avoid collisions. Mathematicians have determined that such logical operations can be described using the conjunctives AND, OR, AND NOT, OR NOT. Boolean algebra is the study of these conjunctives, the language of logic. A summary of the relations and operations of Boolean algebra follow the example of its use below.

Transistors can be used to accomplish logic operations. To illustrate this, an example from automobile operation will be used. Consider the interactions between the ignition switch, the operation of the motor and the oil pressure warning light. If the ignition is off, the motor and light will both be off. If the ignition is turned on, but the starter is not energized the warning lamp should light because the motor has not generated oil pressure. Once the motor is running, the ignition is on and the lamp should be off. These three combinations of ignition, motor and lamp conditions are the only possible combinations signifying proper operation. Note that the three items discussed have only two possible states each, they are on or off. This leads to the use of the binary arithmetic system, which has only two symbols corresponding to the two possible states. Binary numbers will be discussed later in the chapter.

| | I | M | L | Result |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | ✓ |
| 2 | 0 | 0 | 1 | X |
| 3 | 0 | 1 | 0 | X |
| 4 | 0 | 1 | 1 | X |
| 5 | 1 | 0 | 0 | X |
| 6 | 1 | 0 | 1 | ✓ |
| 7 | 1 | 1 | 0 | ✓ |
| 8 | 1 | 1 | 1 | X |

I = IGNITION
M = MOTOR
L = LAMP
R = RESULT
1 = ON
0 = OFF
✓ = ACCEPTABLE
X = UNACCEPTABLE
N = 3 = NO. OF VARIABLES
$2^N = 8$

**TABLE OF ALL POSSIBLE COMBINATIONS OF IGNITION, MOTOR AND LAMP CONDITIONS**

**Figure 12.1**

To write the expressions necessary to derive a circuit, first assign letters to the variables, e.g., I for ignition, M for motor and L for lamp. Next assign the number one to the variable if it is on; assign zero if it is off. Now we can make a table of all possible combinations of the variables as shown in Figure 12.1. The table is formed by writing ones and zeros alternately down the first column, writing ones and zeros in series of two down the second; in fours down the third, etc. For each additional variable, double the number of ones or zeros written in each group. Only $2^N$ rows are written,

where N is the number of variables, since the combinations will repeat if more rows are added. Indicate with a check mark in the result column if the combination represented in the row is acceptable. For example, combination 4 reads, the ignition is off and the motor is running and the warning light is on. This obviously is an unsatisfactory situation. Combination 7 reads, the ignition is on and the motor is running and the warning light is off. This obviously is the normal situation while driving. If we indicate that the variable is a one by its symbol and that it is a zero by the same symbol, with a bar over it and if we use the symbol plus (+) to mean "OR" and multiplication to mean "AND" we can write the Boolean equation $\overline{I}\overline{M}L + I\overline{M}L + IM\overline{L} = R$ where R means an acceptable result. The three terms on the left hand side are combinations 1, 6, and 7 of the table since these are the only ones to give a check mark in the result column. The plus signs indicate that any of the three combinations individually is acceptable. While there are many rules for simplifying such equations, they are beyond the scope of this book.

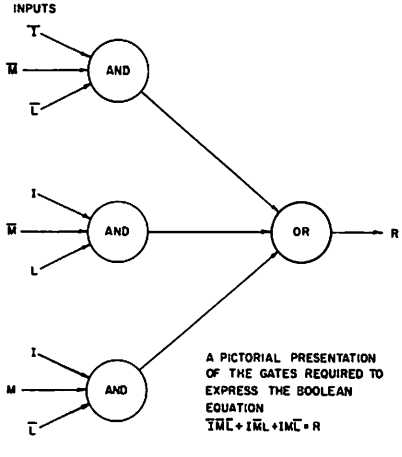



**Figure 12.2**

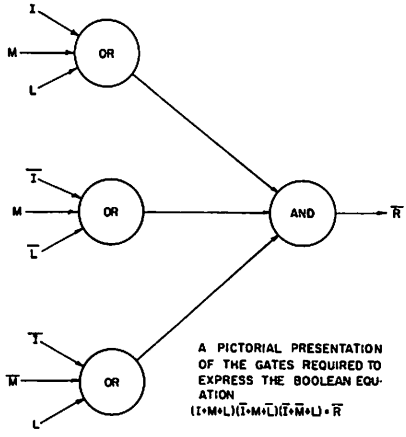



**Figure 12.3**

To express this equation in circuitry, two basic circuits are required. They are named gates because they control the signal passing through. An "AND" gate generates an output only if all the inputs representing the variables are simultaneously applied and an "OR" gate generates an output whenever it receives any input. Our equation translated into gates would be as shown in Figure 12.2. Only if all three inputs shown for an "AND" gate are simultaneously present will an output be generated. The output will pass through the "OR" gate to indicate a result. Note that any equation derived from the table can be written as a series of "AND" gates followed by one "OR" gate.

It is possible to rearrange the equation to give a series of "OR" gates followed by one "AND" gate. To achieve this, interchange all plus and multiplication signs, and remove bars where they exist and add them where there are none. This operation gives us,

$$(I + M + L)(\overline{I} + M + \overline{L})(\overline{I} + \overline{M} + L) = \overline{R}$$

In ordinary language this means if any of the ignition or motor or lamp is on, and simultaneously either the ignition is off or the motor is on or the lamp is off, and simultaneously either the ignition is off or the motor is off or the lamp is on, then the result is unacceptable. Let us apply combination 4 to this equation to see if it is accept-

able. The ignition is off therefore the second and third brackets are satisfied. The first bracket is not satisfied by the ignition because it requires that the ignition be on. However, the motor is on in combination 4, satisfying the conditions of the first bracket. Since the requirements of all brackets are met, an output results. Applying combination 7 to the equation we find that the third bracket cannot be satisfied since its conditions are the opposite of those in combination 7. Consequently, no output appears. Note that for this equation, an output indicates an unacceptable situation, rather than an acceptable one, as in the first equation. In gate form, this equation is shown in Figure 12.3.

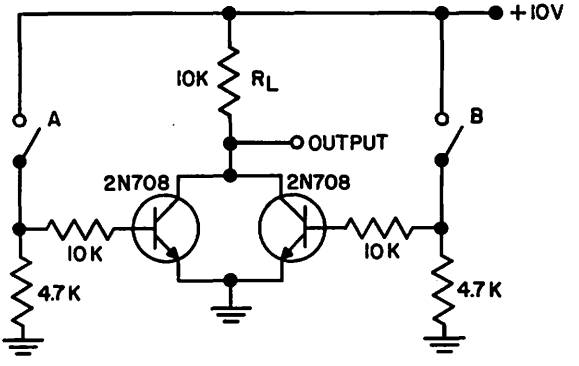
Table 12.1 summarizes the definitions used with the Boolean equations above and indicates some of the rules which were used to convert the equation represented in Figure 12.2 to that of Figure 12.3. The more conventional symbols a, b, c are used in place of I, M, and L.

| DEFINITIONS | |
|---|---|
| a, b, c, etc. | Symbols used in equations |
| ab or $a \cdot b$ or (a)(b) | Reads as "a and b" |
| $\underline{a} + b$ | Reads as "a or b" |
| $\overline{a}$ | Reads as "not a" |
| 1 | Reads as "true" or "on" |
| 0 | Reads as "false" or "off" |
| **LAWS** | |
| Commutative Laws | Distributive Law |
| $a + b = b + a$ | $a(b + c) = ab + ac$ |
| $ab = ba$ | Special Distributive Law |
| Associative Laws | $(a + b)(a + c) = a + bc$ |
| $(a + b) + c = a + (b + c)$ | De Morgan's Theorem |
| $(ab)c = a(bc)$ | $\overline{a + b} = (\overline{a}\overline{b}) \quad \overline{ab} = (\overline{a} + \overline{b})$ |
| **RELATIONSHIPS** | |
| $1 = \overline{0}$ | $0 = \overline{1}$ |
| $a + a = a$ | $a \cdot a = a$ |
| $a + \underline{1} = 1$ | $a \cdot \underline{1} = a$ |
| $\underline{a} + \overline{a} = 1$ | $a \cdot \overline{a} = 0$ |
| $\overline{\overline{a}} = a$ | $a + ab = a(1 + b) = a$ |

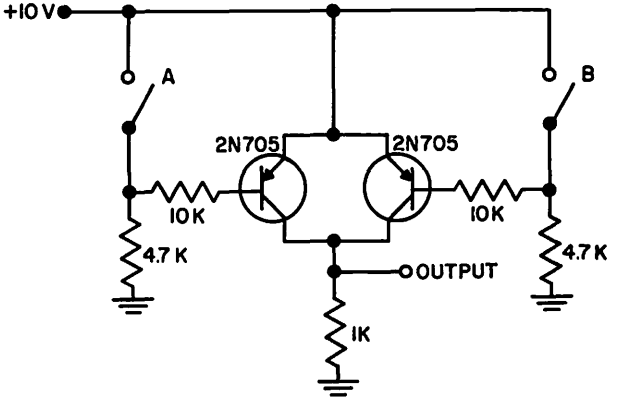
**Table 12.1**

Methods for using transistors in gate circuits are illustrated in Figure 12.4. The base of each transistor can be connected through a resistor either to ground or a positive voltage by operating a switch. In Figure 12.4(A) if both switches are open, both transistors will be non-conducting except for a small leakage current. If either switch A *or* switch B *is* closed, current will flow through $R_L$. If we define *closing* a switch as being

synonymous with applying an input then we have an "OR" gate. When either switch is closed, the base of the transistor sees a positive voltage, therefore, in an "OR" gate the output should be a positive voltage also. In this circuit it is negative, or "NOT OR". The circuit is an "OR" gate with phase inversion. It has been named a "NOR" circuit. Note that if we define *opening* a switch as being synonymous with applying an input, then we have an "AND" circuit with phase inversion since both switch A *and* switch B must be open before the current through $R_L$ ceases. We see that the same circuit can be an "AND" or an "OR" gate depending on the polarity of the input.




(A) GATE USING NPN TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT, THIS IS AN "OR" GATE
IF OPENING A SWITCH IS AN INPUT, THIS IS AN "AND" GATE
NOTE: PHASE INVERSION OF INPUT



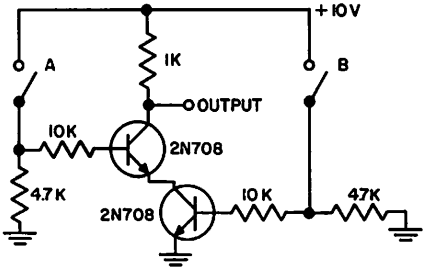

(B) GATE USING PNP TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
NOTE: PHASE INVERSION OF INPUT

**BASIC LOGIC CIRCUITS USING PARALLEL TRANSISTORS**

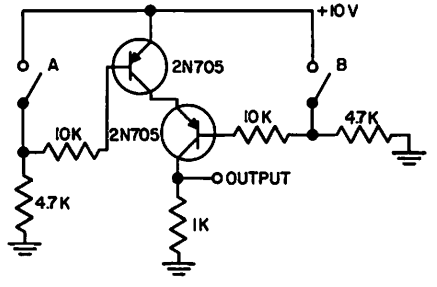
**Figure 12.4**

The circuit in Figure 12.4(B) has identically the same input and output levels but uses PNP rather than NPN transistors. If we define closing a switch as being an input, we find that both switches must be closed before the current through $R_L$ ceases. Therefore, the inputs which made the NPN circuit an "OR" gate make the PNP circuit an "AND" gate. Because of this, the phase inversion inherent in transistor gates does not complicate the overall circuitry excessively.

Figure 12.5(A) and (B) are very similar to Figure 12.4(A) and (B) except that the transistors are in series rather than in parallel. This change converts "OR" gates into "AND" gates and vice versa.




(A) GATE USING NPN TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
NOTE: PHASE INVERSION OF INPUT

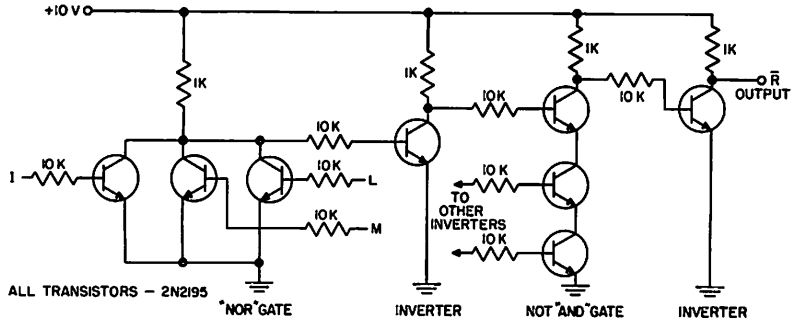



(B) GATE USING PNP TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
NOTE: PHASE INVERSION OF INPUT

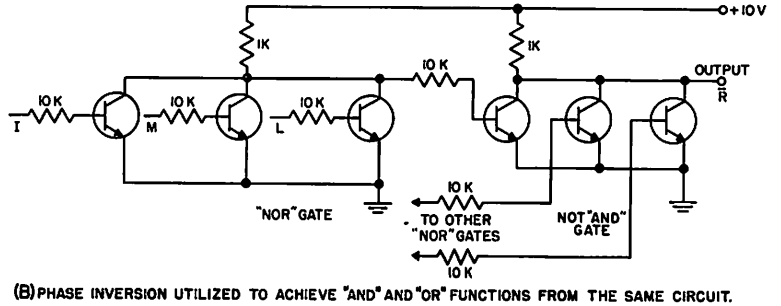
**BASIC LOGIC CIRCUITS**
(USING SERIES TRANSISTORS)
**Figure 12.5**

Looking at the logic of Figure 12.3, let us define an input as a positive voltage; a lack of an input as zero voltage. By using the circuit of Figure 12.4(A) with three transistors in parallel, we can perform the "OR" operation but we also get phase inversion. We can apply the output to an inverter stage which is connected to an "AND" gate of three series transistors of the configuration shown in Figure 12.5(A). An output inverter stage would also be required. This is shown in Figure 12.6(A).

By recognizing that the circuit in Figure 12.4(A) becomes an "AND" gate if the input signal is inverted, the inverters can be eliminated as shown in Figure 12.6(B).




(A) INVERTERS COMPENSATE FOR PHASE INVERSION OF GATES




(B) PHASE INVERSION UTILIZED TO ACHIEVE "AND" AND "OR" FUNCTIONS FROM THE SAME CIRCUIT.

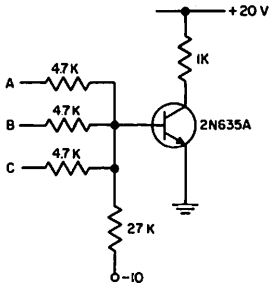
**CIRCUITS REPRESENTING $(I + M + L)(\bar{I} + M + \bar{L})(\bar{I} + \bar{M} + L) = \bar{R}$**

**Figure 12.6**

If the transistors are made by processes yielding low saturation voltages and high base resistance, the series base resistors may be eliminated. Without these resistors the logic would be called direct-coupled transistor logic DCTL. While DCTL offers extreme circuit simplicity, it places severe requirements on transistor parameters and does not offer the economy, speed or stability offered by other logical circuitry.

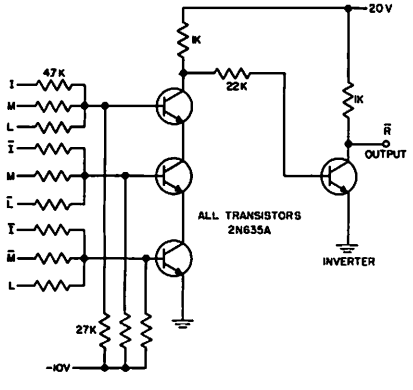
The base resistors of Figure 12.6 relax the saturation voltage and base input voltage requirements. Adding another resistor from each base to a negative bias potential would enhance temperature stability.

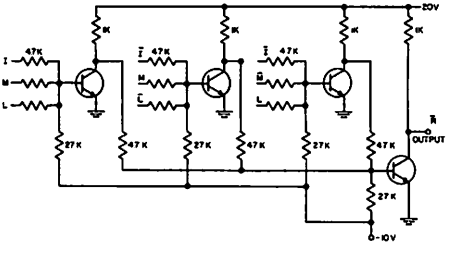
Note that the inputs include both "on" and "off" values of all variables e.g., both I and $\bar{I}$ appear. In order that the gates function properly, I and $\bar{I}$ cannot both be positive simultaneously but they must be identical and oppositely phased, i.e. when I is positive $\bar{I}$ must be zero and vice versa. This can be accomplished by using a phase inverter to generate $\bar{I}$ from I. Another approach, more commonly used, is to take I and $\bar{I}$ from opposite sides of a symmetrical flip-flop.




**BASIC NOR CIRCUIT**
**Figure 12.7**

"NOR" logic is a natural extension of the use of resistors in the base circuit. In the circuit of Figure 12.7, if any of the inputs is made positive, sufficient base current results to cause the transistor to conduct heavily. The "OR" gating is performed by the resistors; the transistor amplifying and inverting the signal. The logic of Figure 12.3 can now be accomplished by combining the "NOR" circuit of Figure 12.7 with the "AND" circuit of Figure 12.5(A). The result is shown in Figure 12.7. In comparing the circuits in Figure 12.6(A) and 12.8, we see that the "NOR" circuit uses one-fourth as many transistors and one-half as many resistors as the brute force approach. In fact if we recall that the equation we are dealing with gives $\overline{R}$ rather than R, we see that we can get R by removing the output phase inverter and making use of the inherent inversion in the "NOR" circuit. In the circuit of Figure 12.7 two supply voltages of +20 and −10 volts are used. The −10 volt supply is to insure that the transistor is held off when $I_{co}$ increases at elevated temperatures. If silicon transistors (such as the 2N708, 2N914, or 2N2193A) are used in NOR logic circuits the hold off supply may not be necessary. Since $V_{BE}$ is larger for silicon devices and $I_{co}$ is very low a resistor returned to the emitter reference may result in sufficient circuit stability.



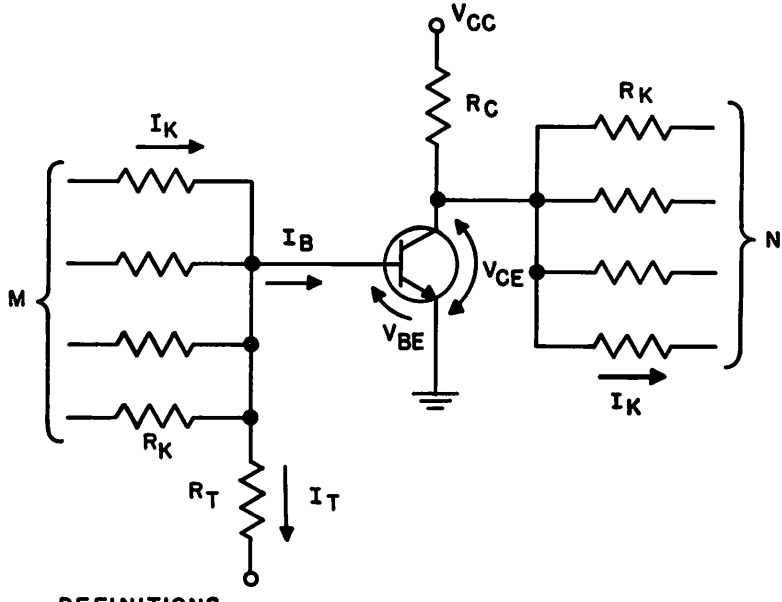




**(A) NOR LOGIC USING SERIES TRANSISTORS FOR "AND" GATE**

**(B) NOR LOGIC USING INVERSION FOR "AND" GATE**

**Figure 12.8**

Because of the fact that a generalized Boolean equation can be written as a series of "OR" gates followed by an "AND" gate as was shown, it follows that such equations can be written as a series of "NOR" gates followed by a "NOR" gate. The low cost of the resistors used to perform the logic and the few transistors required make "NOR" logic attractive.




DEFINITIONS

$I_K$ = MINIMUM CURRENT THROUGH $R_K$ FOR TURNING TRANSISTOR ON

$I_B$ = MINIMUM BASE CURRENT FOR TURNING TRANSISTOR ON

$I_T$ = BIAS CURRENT TO KEEP TRANSISTOR OFF AT HIGH TEMPERATURES

M = MAX. NUMBER OF INPUTS PERMITTED

N = MAX. NUMBER OF OUTPUTS PERMITTED

$V_{BE}$ = MAX. BASE TO EMITTER VOLTAGE WHEN THE TRANSISTOR IS ON.

$V_{CE}$ = MAX. COLLECTOR TO EMITTER VOLTAGE WHEN THE TRANSISTOR IS ON.

**CIRCUIT USED FOR DESIGN OF NOR CIRCUITRY**

**Figure 12.9**

A detailed "NOR" building block is shown in Figure 12.9. The figure defines the basic quantities. The circuit can readily be designed with the aid of three basic equations. The first derives the current $I_K$ under the worst loading conditions at the collector of a stage.

$$I_K = \frac{V_{CC} - V_{BE} - I_{COM}R_C}{R_K + NR_C} \qquad (12a)$$

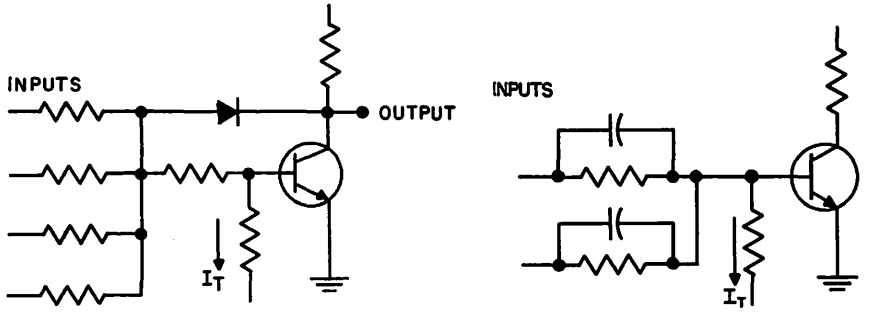
where $I_{COM}$ is the maximum $I_{CO}$ that is expected at the maximum junction temperature. The second equation indicates the manner in which $I_K$ is split up at the base of the transistor.

$$I_K = I_B + \frac{M\,(V_{CEM} - V_{CEN} + V_{BE} - V_{EB}) - (V_{BE} - V_{CEN})}{R_K} + I_{COM} \qquad (12b)$$

where $V_{CEN}$ is the minimum expected saturation voltage, $V_{CEM}$ is the maximum expected saturation voltage and $V_{EB}$ is the reverse bias required to reduce the collector current to $I_{CO}$. $V_{EB}$ is a negative voltage. The third equation ensures that $V_{EB}$ will be reached to turn off the transistor.

$$I_{COM} + \frac{(V_{CEM} - V_{EB})M}{R_K} = I_T \qquad (12c)$$

Knowing $I_T$ and choosing a convenient bias potential permits calculation of $R_T$. In using these equations, first select a transistor type. Assume the maximum possible supply voltage and collector current consistent with the rating of the transistor and the maximum anticipated ambient temperature. This will ensure optimization of N and M. From the transistor specifications, values of $I_{COM}$, $V_{BE}$, $V_{CEN}$, and $I_B$ (min) can be calculated. $I_B$ (min) is the minimum base current required to cause saturation. $R_C$ is calculated from the assumed collector current. In equation (12a) solve for $I_K$ using the desired value of N and an arbitrary value for $R_K$. Substitute the value for $I_K$ in equation (12b) along with a chosen value for M and solve for $I_B$. While superficially $I_B$ need only be large enough to bring the transistor into saturation, increasing $I_B$ will improve the rise time.

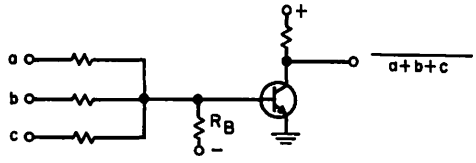
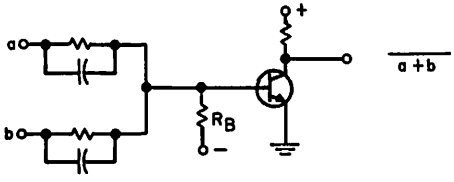
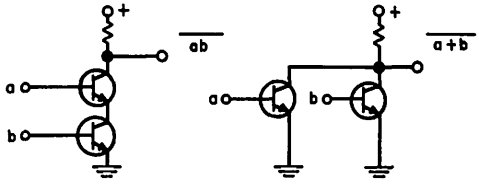
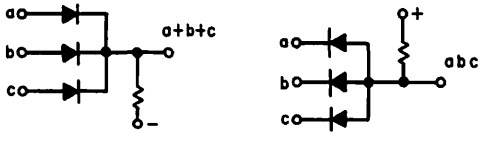
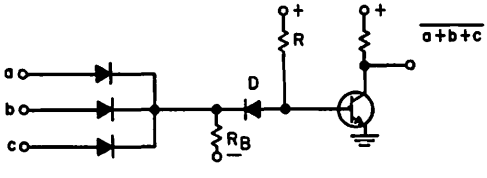



CLAMPING DIODE REDUCES STORAGE TIME TO INCREASE SPEED
(A)

CAPACITORS REDUCE STORAGE TIME TO INCREASE SPEED
(B)

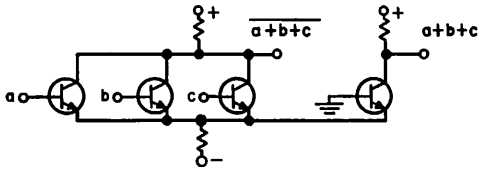
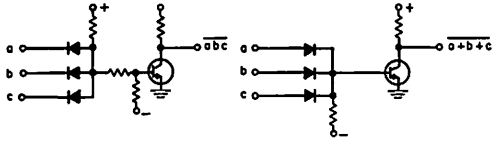
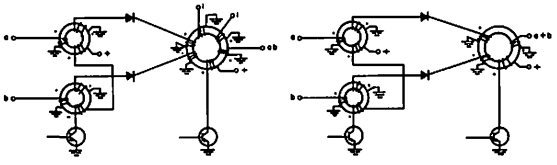
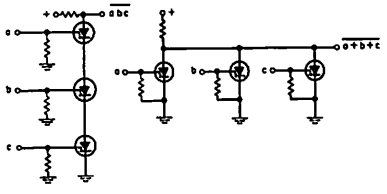
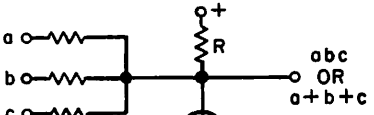
**Figure 12.10**

Circuit speed can also be enhanced by using a diode as shown in Figure 12.10(A) to prevent severe saturation or by shunting $R_K$ by a capacitor as in 12.10(B). The capacitors may cause malfunction unless the stored charge during saturation is carefully controlled; they also aggravate crosstalk between collectors. For this reason it is preferable to use higher frequency transistors without capacitors when additional speed is required. Table 12.2 lists the characteristics of common logic systems employing transistors.

| NAME | TYPICAL CIRCUIT (Positive signals are defined as 1) | DESCRIPTION |
|---|---|---|
| **RTL** Resistor transistor logic (NOR) |   | Logic is performed by resistors. Any positive input produces an inverted output irrespective of the other inputs. Resistor $R_B$ gives temperature stability. (See Fig. 12.7) |
| **RCTL** Resistor capacitor transistor logic |   | Same as RTL except that capacitors are used to enhance switching speed. The capacitors increase the base current for fast collector current turn on and minimize storage time by supplying a charge equal to the stored base charge. |
| **DCTL** Direct coupled transistor logic |   | Logic is performed by transistors. $V_{CE}$ and $V_{BE}$, measured with the transistor in saturation, define the two logic levels. $V_{CE}$ must be much less than $V_{BE}$ to ensure stability and circuit flexibility. (See Fig. 12.6) |
| **DL** Diode logic |   | Logic is performed by diodes. The output is not inverted. Amplifiers are required to maintain the correct logic levels through several gates in series. |
| **LLL** Low level logic |   | Logic is performed by diodes. The output is inverted. The diode D isolates the transistor from the gate permitting R to turn on the collector current. By proper choice of voltage changes occur. This method is also called current switching diode logic. |

| FEATURES | SUITABLE TRANSISTORS | | | | SUITABLE DIODES |
|---|---|---|---|---|---|
| | GERMANIUM | | SILICON | | SILICON |
| | Low Speed ($f_a < 15$ mcs.) | High Speed ($f_a > 15$ mcs.) | Low Speed ($f_a < 15$ mcs.) | High Speed ($f_a > 15$ mcs.) | High Speed |
| The circuit design is straightforward. All logical operations can be performed with only this circuit. Many transistors readily meet the steady state requirements. | 2N78*<br>2N167*<br>2N169A<br>2N398A*<br>2N525<br>2N526*<br>2N635A<br>2N1304<br>2N1305<br>2N1924 | 2N705<br>2N711<br>2N828<br>2N964<br>2N994 | 2N335<br>2N656A | 2N706<br>2N708<br>2N914<br>2N1613<br>2N2193 | |
| Faster than RTL at the expense of additional components and stringent stored charge requirements. | 2N398A*<br>2N404<br>2N634 | 2N705<br>2N711 | | 2N1613<br>2N2193 | |
| Very low supply voltages may be used to achieve high power efficiency and miniaturization. Relatively fast switching speeds are practical. | | 2N781 | | 2N708<br>2N914 | |
| Several gates may be used between amplifiers. High speeds can be attained. Non-inversion simplifies circuit design problems. Relatively inexpensive components are used. | 2N78*<br>2N167<br>2N398A*<br>2N526*<br>2N635A | 2N705<br>2N711<br>2N964<br>2N994 | 2N333*<br>2N337*<br>2N656A | 2N706<br>2N708<br>2N914<br>2N1613<br>2N2193 | 1N3604<br>1N3605<br>1N3606 |
| The number of inputs to the diode gate does not affect the transistor base current thus giving predictable performance. The small voltage excursions minimize the effects of stray capacitance and enhance switching speed. | 2N398A*<br>2N525<br>2N526*<br>2N635<br>2N1304<br>2N1305 | 2N781<br>2N828 | 2N335*<br>2N338* | 2N914<br>2N1711<br>2N2192 | 1N3604<br>1N3605<br>1N3606 |

**Table 12.2**

| NAME | TYPICAL CIRCUIT (Positive signals are defined as 1) | DESCRIPTION |
|---|---|---|
| **CML** Current mode logic |  | Logic is performed by transistors which are biased from constant current sources to keep them far out of saturation. Both inverted and non-inverted outputs are available. |
| **DTL** Diode transistor logic |  | Logic is performed by diodes. The output is inverted. The transistor acts as an amplifier. This is essentially an extension of the diode logic discussed above. |
| **CDL** Core diode logic |  | Logic is performed by cores and transmitted by diodes. Transistors act as drivers to shift information. Each transistor can drive many cores but not successive cores in the logic line. |
| **4 Layer** Device logic |  | Logic is performed by silicon controlled switches which are triggered on at the gate lead. The gates can be actuated by pulse or DC levels. The gates have a built in memory and must be reset. |
| **TDL** Tunnel diode logic |  | Logic is performed by tunnel diode switching from low voltage to high voltage state. Whether circuit represents AND or OR gate depends on bias current through resistor R. Tunnel diode biased near peak current for OR gate, and close to ground for AND. |

| FEATURES | SUITABLE TRANSISTORS | | | | SUITABLE DIODES |
|---|---|---|---|---|---|
| | GERMANIUM | | SILICON | | SILICON |
| | Low Speed ($f_a < 15$ mcs.) | High Speed ($f_a > 15$ mcs.) | Low Speed ($f_a < 15$ mcs.) | High Speed ($f_a > 15$ mcs.) | High Speed |
| Very high switching speeds are possible because the transistors are operated at optimum operating conditions. Although the voltage excursion is small the circuitry is relatively unaffected by noise. | | 2N705<br>2N711<br>2N964<br>2N994 | 2N337*<br>2N338* | 2N708<br>2N914 | |
| High speeds can be attained. The impedance and voltage levels from stage to stage are well defined. | 2N78*<br>2N167<br>2N396A*<br>2N526*<br>2N635A<br>2N1304<br>2N1305 | 2N705<br>2N711<br>2N964<br>2N994 | 2N333*<br>2N337* | 2N706<br>2N708<br>2N914<br>2N1613 | 1N3604<br>1N3605<br>1N3606 |
| These core modules can be made very small. Speed is limited by core switching speeds. | | | | 2N697<br>2N1613<br>2N1893<br>2N2193<br>2N2243 | 1N3604<br>1N3605<br>1N3606<br>1N3607<br>1N3608<br>1N3609 |
| These gates are pulse or dc actuated and the input need not be maintained. High output power capability is available. In general, in the presence of radiation, units will turn on permitting fail-safe design in this atmosphere. | SUITABLE DEVICES<br>3N58, 3N59 } Silicon Controlled Switches | | | | |
| Current flowing through input resistors determines logic. Circuit is basically simple and very high speed is obtainable. | SUITABLE DEVICES<br>TD-1A, TD-2A, TD-3A, TD-311B } Germanium Tunnel Diodes<br>NOTE: Other peak current diodes are listed in Chapter 22. | | | | |

*Military types

**Table 12.2 (Continued)**

## BINARY ARITHMETIC

Because bistable circuits can be readily designed using a variety of components from switches to transistors, it is natural for counters to be designed to use binary numbers, i.e., numbers to the base, or radix, 2. In the conventional decimal system, a number written as 2904 is really a contraction for $2 \times 10^3 + 9 \times 10^2 + 0 \times 10^1 + 4 \times 1$. Each place refers to a different power of 10 in ascending order from the right. In the binary system, only two symbols are permitted, 0 and 1. All numbers are constructed on the basis of ascending powers of 2. For example, 11011 means $1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 1$. This is 27 in the decimal system.

This notation applies also to decimal fractions as well as integers. For example, the number 0.204 is a contraction of $2 \times 10^{-1} + 0 \times 10^{-2} + 4 \times 10^{-3}$. Similarly, the binary number 0.1011 is a contraction of $1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4}$. Using this construction, a table of equivalent binary and decimal numbers can be obtained as shown below.

| *Binary* | *Decimal* | *Binary* | *Decimal* |
|---|---|---|---|
| 0 | 0 | 0.000 | 0.000 |
| 1 | 1 | 0.001 | 0.125 |
| 10 | 2 | 0.010 | 0.250 |
| 11 | 3 | 0.011 | 0.375 |
| 100 | 4 | 0.100 | 0.500 |
| 101 | 5 | 0.101 | 0.625 |
| 110 | 6 | 0.110 | 0.750 |
| 111 | 7 | 0.111 | 0.875 |

Arithmetic operations can best be described by comparative examples..

| Addition | | Subtraction | |
|---|---|---|---|
| 42 | 101010 | 44 | 101100 |
| +18 | 10010 | −18 | 10010 |
| 60 | 111100 | 26 | 11010 |

During addition, the digits in a column are added to the carry from the previous column. The result is expressed as a sum digit which is recorded and a carry digit which is applied to the next column. The term digit generally refers to the figures in a decimal number; the term bit (an abbreviation of binary digit) is used with binary numbers. If the digit being subtracted is the larger of the two in the column, the techniques used to handle this situation in decimal subtraction are also applicable in the binary system.

| Multiplication | | Division | |
|---|---|---|---|
| 42 | 101010 | 1.35 | 1.0101 |
| 21 | 10101 | $5\sqrt{6.7500}$ | $101\sqrt{110.11000}$ |
| 42 | 101010 | 5 | 101 |
| 84 | 101010 | 17 | 111 |
| 882 | 101010 | 15 | 101 |
| | 1101110010 | 25 | 1000 |
| | | 25 | 101 |
| | | | 110 |

Multiplying a binary number by two is equivalent to adding a zero to its right hand

side, just as multiplying a decimal number by 10 adds a zero. This is equivalent to shifting the number one place to the left. In computers, this operation is done by a shift register. Division can be readily understood since it involves the operations of additions, subtraction and multiplication only.

Computers generally employ circuits called adders which can perform the operation of addition. Adders can also perform other arithmetic operations besides addition. For example, an adder can perform subtraction by the use of a number's complement. The complement is obtained numerically by interchanging all ones and zeros. In equipment the complement can be obtained by taking the output from the opposite side of flip-flops.

The manner in which subtraction with an adder is accomplished is given by the following example:

| | |
|---|---|
| Problem: | Calculate<br>1101 − 1001 |
| Complement of | 1001 is 0110<br>(1111 − 1001 = 0110) |
| Add: | 1101 + 0110 = 10011 |
| Add 1 | 10011 + 1 = 10100 |
| Omit left hand digit to obtain | 1101 − 1001 = 100 |

Flip-flops can be connected in series so that the first flip-flop will alternate states with each input pulse, and successive flip-flops will alternate states at half the rate of the preceding flip-flop. In this way the flip-flops assume a unique configuration of states for a given number of input pulses. The flip-flops actually perform the function of binary counting. A practical circuit of a binary counter is shown in Figure 11.3(B) The count in a binary counter can be determined by noting whether each stage is in the 1 or 0 condition, and then assigning the appropriate power of 2 to the stage to reconstruct the number as in the examples above.

If it is required to count to a base other than 2, a binary counter can be modified to count to the new base.

The rules for accomplishing the modification will be illustrated for a counter to the base 10.

| Rule | Example |
|---|---|
| 1) Determine the number of binary stages (N) required to count to the desired new base (M) | M = 10<br>$2^3 < 10 < 2^4$<br>N = 4 |
| 2) Subtract M from $2^N$ | $2^4 - 10 = 6$ |
| 3) Write the remainder in binary form | 6 = 110 |
| 4) When the count reaches $2^{N-1}$, feed back a one to each stage of the counter having a one in the remainder shown in 3) | $2^{N-1} = 2^3 = 1000$<br>Feedback added gives<br>1 110 |

As additional pulses are added beyond the count $2^{N-1}$, they will count through to M and then recycle to zero. This method is based on advancing the count at the point $2^{N-1}$ to the extent that the indicated count is $2^N$ when M input pulses are applied. The feedback is applied when the most significant place becomes a one but it is imperative that feedback be delayed until the counter settles down in order to avoid interference with the normal counter action.

# UNIJUNCTION TRANSISTOR CIRCUITS

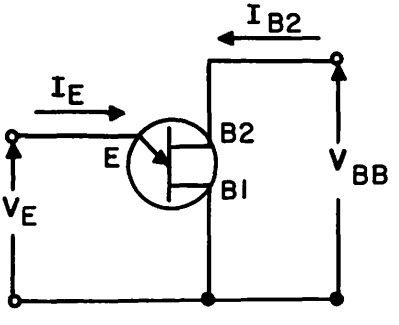
CHAPTER 13

The unijunction transistor is a three-terminal semiconductor device which has electrical characteristics quite different from those of a conventional two-junction transistor. Its most important features are: (1) a stable firing voltage which is a fixed fraction of the applied interbase voltage, (2) a very low value of firing current ($I_p$), (3) a negative resistance characteristic which is uniform from unit to unit and stable with temperature and life, (4) a high pulse current capability, and (5) a low cost. These characteristics make the unijunction transistor advantageous in oscillators, timing circuits, voltage sensing circuits, SCR firing circuits and bistable circuits.

The unijunction transistor is available in 28 distinct types to meet the needs of a wide range of applications. Types 2N489 to 2N494 feature tight control on all parameters, particularly on $\eta$ ($\pm 10\%$ limits) and $R_{BB}$ ($\pm 20\%$ limits). These types differ from one another primarily in the limit values of $\eta$ and $R_{BB}$. Military versions of types 2N489 to 2N494 are available to meet military specifications MIL-T-19500A/75. Type 2N1671 and 2N2160 are low cost types, suitable for applications where lower voltage ratings and wider ranges of $\eta$ and $R_{BB}$ can be tolerated. Types 2N1671A and 2N489A to 2N494A have guaranteed characteristics for firing Silicon Controlled Rectifiers. Types 2N1671B and 2N489B to 2N494B have lower limits on peak point current and emitter leakage current and are intended for applications such as time delay circuits where a sensitive characteristic is required.

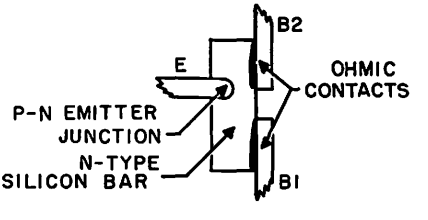
## THEORY OF OPERATION

The construction of the unijunction transistor is shown in Figure 13.2. Two ohmic contacts, called base-one (B1) and base-two (B2) are made at opposite ends of a small bar of n-type silicon. A single rectifying contact, called the emitter (E), is made on the opposite side of the bar close to base-two. An interbase resistance, $R_{BB}$, of between 5K and 10K exists between base-one and base-two. In normal circuit opera-




SYMBOL FOR UNIJUNCTION TRANSISTOR WITH INDENTIFICATION OF PRINCIPLE VOLTAGES AND CURRENTS

Figure 13.1

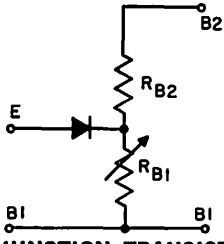



CONSTRUCTION OF UNIJUNCTION TRANSISTOR — CROSS SECTIONAL VIEW

Figure 13.2

tion, base-one is grounded and a positive bias voltage, $V_{BB}$, is applied at base-two. With no emitter current flowing, the silicon bar acts like a simple voltage divider (Figure 13.3) and a certain fraction, $\eta$ of $V_{BB}$ will appear at the emitter. If the emitter voltage, $V_E$, is less than $\eta$ $V_{BB}$, the emitter will be reverse-biased and only a small emitter leakage current will flow. If $V_E$ becomes greater than $\eta$ $V_{BB}$, the emitter will be forward biased and emitter current will flow. This emitter current consists primarily of holes injected into the silicon bar. These holes move down the bar from the emitter to base-one and result in an equal increase in the number of electrons in the emitter to base-one region. The net result is a decrease in the resistance between emitter and base-one so that as the emitter current increases, the emitter voltage decreases and a negative resistance characteristic is obtained (Figure 13.5).

The operation of the unijunction transistor may be best understood by the representative circuit of Figure 13.3. The diode represents the emitter diode, $R_{B1}$ represents the resistance of the region in the silicon bar between the emitter and base-one and $R_{B2}$ represents the resistance between the emitter and base-two. The resistance $R_{B1}$ varies with the emitter current as indicated in Figure 13.4.




**UNIJUNCTION TRANSISTOR REPRESENTATIVE CIRCUIT**

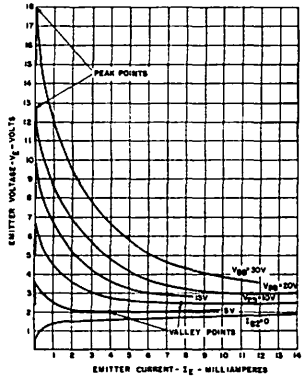
**Figure 13.3**

| $I_E$ (MA) | $R_{B1}$ (OHMS) |
|---|---|
| 0 | 4600 |
| 1 | 2000 |
| 2 | 900 |
| 5 | 240 |
| 10 | 150 |
| 20 | 90 |
| 50 | 40 |

**VARIATION OF $R_{B1}$ WITH $I_E$ IN REPRESENTATIVE CIRCUIT (TYPICAL 2N492)**

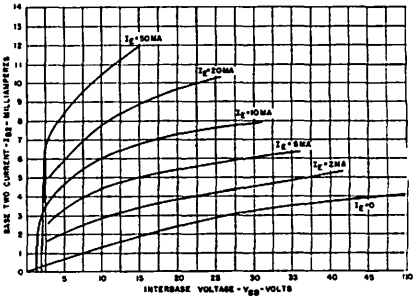
**Figure 13.4**

The large signal properties of the unijunction transistor are usually given in the form of characteristic curves. Figure 13.5 gives typical emitter characteristic curves as plots of emitter voltage vs. emitter current for fixed values of interbase voltage. Figure 13.6 gives typical interbase characteristic curves as plots of interbase voltage vs. base-




**TYPICAL EMITTER CHARACTERISTICS (TYPE 2N492)**

**Figure 13.5**




**TYPICAL INTERBASE CHARACTERISTICS (TYPE 2N492)**

**Figure 13.6**

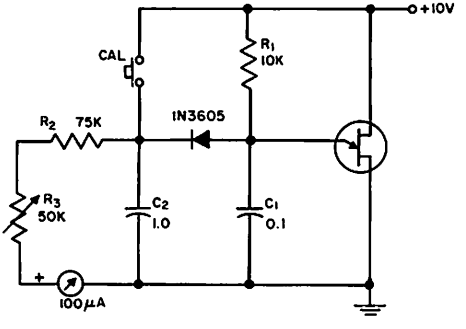
two current for fixed values of emitter current. On each of the emitter characteristic curves there are two points of interest, the peak point and the valley point. On each of the emitter characteristic curves the region to the left of the peak point is called the cut-off region; here the emitter is reverse biased and only a small leakage current flows. The region between the peak point and the valley point is the negative resistance region. The region to the right of the valley point is the saturation region; here the dynamic resistance is positive and lies in the range of 5 to 20Ω.

## PARAMETERS – DEFINITION AND MEASUREMENT

1. $R_{BB}$ – Interbase Resistance. The interbase resistance is the resistance measured between base-one and base-two with the emitter open circuited. It may be measured with any conventional ohmmeter or resistance bridge if the applied voltage is five volts or less. The interbase resistance increases with temperature at about 0.8%/°C. This temperature variation of $R_{BB}$ may be utilized for either temperature compensation or in the design of temperature sensitive circuits.

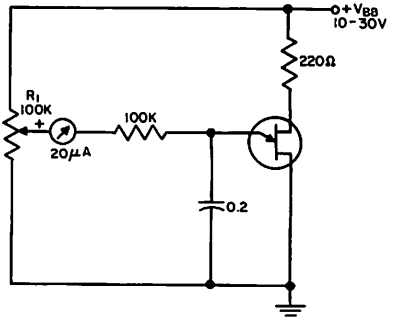
2. $\eta$ – Intrinsic Stand-off Ratio. This parameter is defined in terms of the peak point voltage, $V_P$, by means of the equation: $V_P = \eta V_{BB} + V_D$ . . . where $V_D$ is about 0.67 volt at 25°C and decreases with temperature at about 3 millivolts/°C. It is found that $\eta$ is constant over wide ranges of temperature and interbase voltage. A circuit which may be used to measure $\eta$ is shown in Figure 13.7. In this circuit $R_1$, $C_1$ and the unijunction transistor form a relaxation oscillator and the remainder of the circuit serves as a peak voltage detector with the diode automatically subtracting the voltage $V_D$. To use the circuit, the "cal" button is pushed and $R_3$ adjusted to make the meter read full scale. The "cal" button is then released and the value of $\eta$ is read directly from the meter (1.0 full scale). If the voltage $V_1$ is changed, the meter must be recalibrated.

3. $I_P$ – Peak Point Current. The peak point current corresponds to the emitter current at the peak point. It represents the minimum current which is required to fire the unijunction transistor or required for oscillation in the relaxation oscillator circuit. $I_P$ is inversely proportional to the interbase voltage. $I_P$ may be measured in the circuit of Figure 13.8. In this circuit the potentiometer setting is slowly increased until the unijunction transistor fires as evidenced by a sudden jump and oscillation of the meter needle. The current reading just prior to when the jump takes place is the peak point current.




TEST CIRCUIT FOR INTRINSIC STANDOFF RATIO ($\eta$)

Figure 13.7




TEST CIRCUIT FOR PEAK POINT EMITTER CURRENT ($I_p$)

Figure 13.8

4. $V_P$ – Peak Point Emitter Voltage. This voltage depends on the interbase voltage as indicated in (2). $V_P$ decreases with increasing temperature because of the change in $V_D$ and may be stabilized by a small resistor in series with base-two.

5. $V_E$ (sat) – Emitter Saturation Voltage. This parameter indicates the forward drop of the unijunction transistor from emitter to base-one in the saturation region. It is measured at an emitter current of 50 ma and an interbase voltage of 10 volts.

6. $I_{B2}$ (mod) – Interbase Modulated Current. This parameter indicates the effective current gain between emitter and base-two. It is measured as the base-two current under the same condition used to measure $V_E$ (sat).

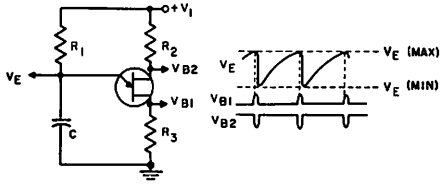
7. $I_{EO}$ – Emitter Reverse Current. The emitter reverse current is measured with 60 volts between base-two and emitter with base-one open circuit. This current varies with temperature in the same way as the $I_{CO}$ of a conventional transistor.

8. $V_V$ – Valley Voltage. The valley voltage is the emitter voltage at the valley point. The valley voltage increases as the interbase voltage increases, it decreases with resistance in series with base-two and increases with resistance in series with base-one.

9. $I_V$ – Valley Current. The valley current is the emitter current at the valley point. The valley current increases as the interbase voltage increases and decreases with resistance in series with base-one or base-two.

## RELAXATION OSCILLATOR

The relaxation oscillator circuit shown in Figure 13.9 is a basic circuit for many applications. It is chiefly useful as a timing circuit, a pulse generator, a trigger circuit or a sawtooth wave generator.




**BASIC RELAXATION OSCILLATOR WITH TYPICAL WAVEFORMS**
**Figure 13.9**

Conditions for Oscillation.

$$\frac{V_1 - V_P}{R_1} > I_p, \quad \frac{V_1 - V_V}{R_1} < I_V$$

It is found that these conditions are very broad permitting a 1000 to 1 range of $R_1$ from about 2K to 2M. $R_2$ is used for temperature compensation, its value may be calculated from the equation:

$$R_2 \cong \frac{0.40\, R_{BB}}{\eta V_1} \text{ (units are ohms, volts)}$$

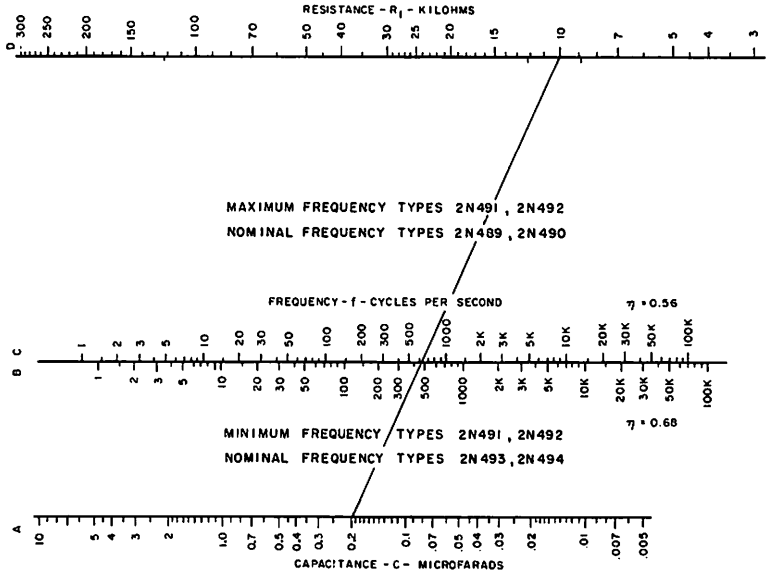
The maximum and minimum voltages of the emitter voltage waveform may be calculated from:

$$V_E \text{ (max)} = V_P = \eta V_{BB} + .67 \text{ volt}$$
$$V_E \text{ (min.)} \cong 0.5\, V_E \text{ (sat)}$$

The frequency of oscillation is given by the equation:

$$f \cong \frac{1}{R_1 C \ln\left(\frac{1}{1-\eta}\right)}$$

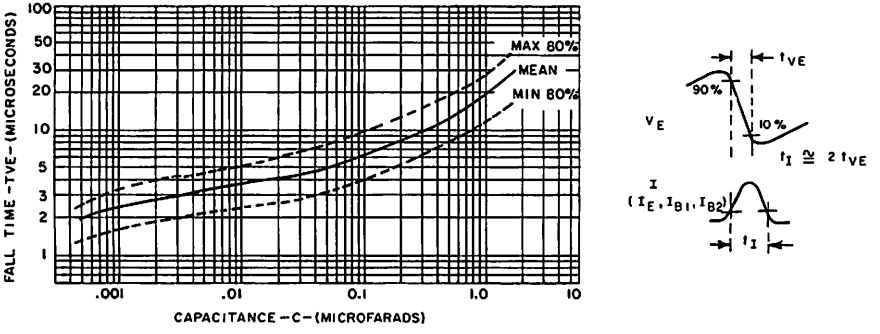
and may be obtained conveniently from the nomogram of Figure 13.10.




**NOMOGRAM FOR CALCULATING FREQUENCY OF RELAXATION OSCILLATION**

**Figure 13.10**

The emitter voltage recovery time, $t_{VE}$, is defined as the time between the 90% and 10% points on the emitter voltage waveform. The value of $t_{VE}$ is determined primarily by the size of the capacitor C in Figure 13.9 and may be obtained from Figure 13.11.




**RECOVERY TIME OF UNIJUNCTION TRANSISTOR RELAXATION OSCILLATOR VS. CAPACITY**

**Figure 13.11**

The pulse amplitude at base-one or base-two may be determined from the equations:

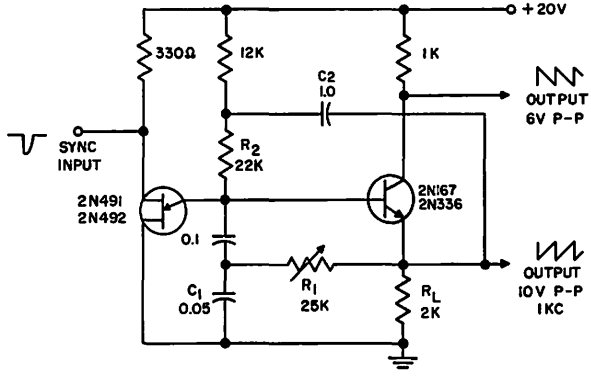
$$I_{E(peak)} \cong \frac{[V_p - 1/2\,V_E(sat)]\,C}{t_{VE}}$$

$$I_{B2(peak)} \cong \frac{I_{B2}(mod)}{7}\sqrt{I_{E(peak)}}$$

Units are ma, volts, mμf, μsec.

## ULTRA-LINEAR SAWTOOTH WAVE GENERATOR

The circuit of Figure 13.12 may be used as a linear sawtooth wave generator. The NPN transistor serves as an output buffer amplifier with the capacitor $C_2$ and resistor $R_2$ serving in a bootstrap circuit to improve the linearity of the sawtooth. $R_1$ and $C_1$ give integrator type feedback which compensates for the loading of the output stage. Optimum linearity is obtained by adjusting $R_1$. Linearity is 0.3% or more depending on $h_{FE}$ of the NPN transistor.




**SAWTOOTH GENERATOR WITH HIGH LINEARITY**

**Figure 13.12**

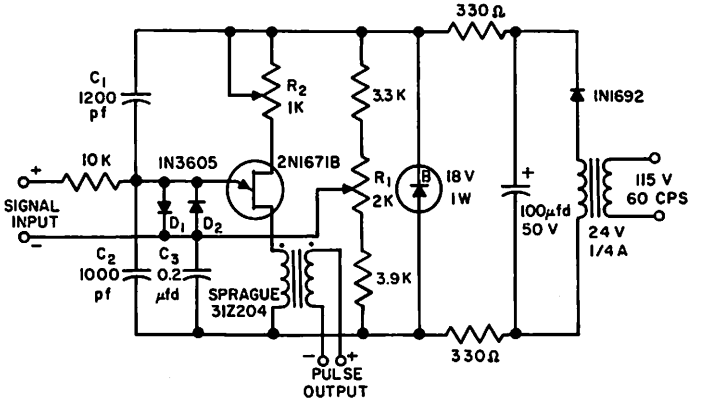
## VOLTAGE SENSING CIRCUIT

The high sensitivity of the unijunction transistor and the extreme stability of its firing characteristic make it ideally suited for use in go no-go types of voltage sensing circuits such as shown in Figure 13.13. This circuit includes a simple floating power supply with zener diode regulation which operates from the 115 volt AC line. If the input signal is negative the unijunction transistor will not fire and there will be no output. If the input signal is slightly positive, the unijunction transistor will fire and pulses will occur at the output as long as the input signal remains positive. The output pulses are of sufficient magnitude to trigger a flip-flop, an SCR, or other pulse sensitive devices. Note that the transformer coupled supply and output of this circuit give complete freedom of choice in connecting the circuit to the signal source since there are no common grounds.

Most of the output pulse energy is supplied by capacitor $C_3$. This capacitor is charged rapidly through $R_1$ after each pulse and hence does not limit the response time of the circuit. Diode $D_2$ provides a discharge path for $C_3$ and diode $D_1$ and $D_2$ clamp the input voltage to enable $C_3$ to charge to its steady state voltage when very large voltages are present at the signal input. Capacitors $C_1$ and $C_2$ provide the initial firing energy for the unijunction transistor and also serve as a filter for transients appearing at the signal input and across the supply. In some cases a small capacitor will also be required across the primary of the pulse transformer to prevent false triggering due to transients.

The circuit is initially adjusted by shorting the signal input and setting $R_1$ so that the circuit is on the verge of firing. If close temperature compensation is needed $R_2$ is adjusted so that the firing voltage does not change appreciably when the unijunction transistor is heated or cooled. It is normally possible to adjust the temperature com-

pensation so that the drift in firing voltage is within ±2 millivolts from 0°C to 55°C. After the temperature compensation is completed it will normally be necessary to reset $R_1$. The long term stability of this circuit is normally better than ±10 millivolts and the hysteresis is normally less than 1 millivolt. The change in firing voltage with a change in the supply voltage ($\Delta V_1$) will be less than 0.7 $\Delta V_1/V_1$. The voltage stability can be improved by adding two silicon diodes in series with $R_2$.



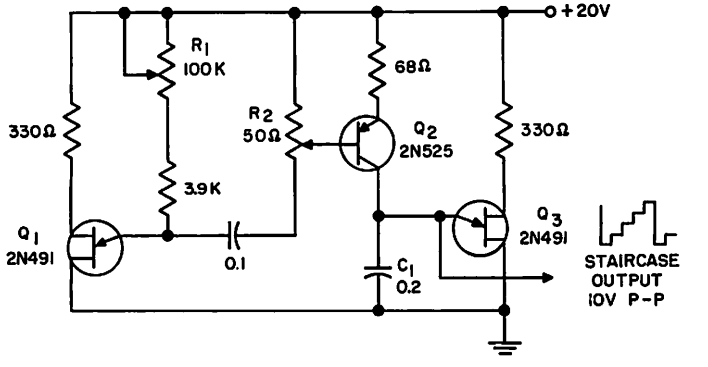

**VOLTAGE SENSING AND TRIGGER CIRCUIT**

**Figure 13.13**

## STAIRCASE WAVE GENERATOR

Figure 13.14 shows a simple staircase wave generator which has good stability and a wide operating range. The unijunction transistor $Q_1$ operates as a free running oscillator which generates negative pulses across $R_2$. These pulses produce current pulses from the collector of $Q_2$ which charge capacitor $C_1$ in steps. When the voltage across $C_1$ reaches the peak point voltage of $Q_3$ this transistor fires and discharges $C_1$.

Resistor $R_1$ determines the frequency of the steps and resistor $R_2$ determines the number of steps per cycle. The circuit shown can be adjusted for a step frequency



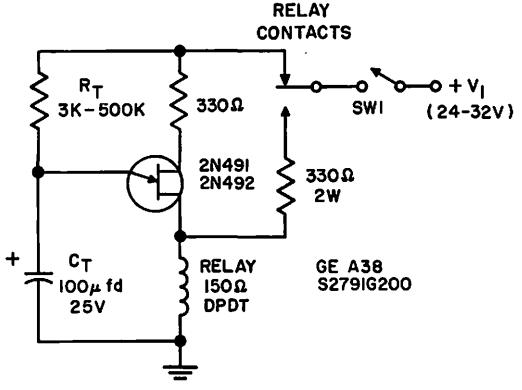

**STAIRCASE WAVE GENERATOR**
(FREQUENCY DIVIDER)

**Figure 13.14**

from 100 cps to 2 KC and the number of steps per cycle can be adjusted from one to several hundred. This circuit can also be adapted to a frequency divider by cascading stages similar to the stage formed by $Q_2$ and $Q_3$.

## TIME DELAY RELAY

Figure 13.15 shows how the unijunction transistor can be used to obtain a precise delay in the operation of a relay. When the switch SW1 is closed, capacitor $C_T$ is




**TIME DELAY CIRCUIT WITH RELAY**

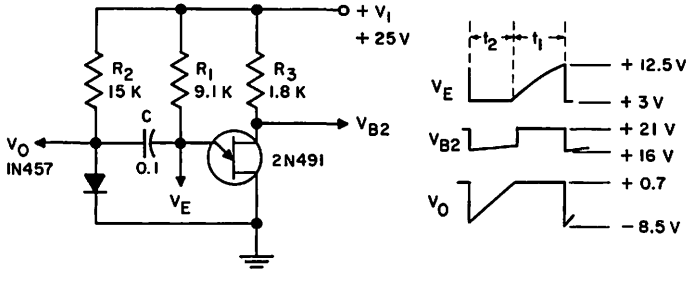
**Figure 13.15**

charged to the peak point voltage at which time the unijunction transistor fires and the capacitor discharges through the relay thus causing it to close. One set of relay contacts hold the relay closed and the second set of contacts can be used for control functions. To be used in this circuit, relays must have fast operating times, low coil resistance and low operating power.

The time delay of this circuit is determined by $R_T$, about one second of delay is obtained for each 10K of resistance, $R_T$. The time delay is quite independent of temperature and supply voltage.

## MULTIVIBRATOR

Figure 13.16 shows a unijunction transistor multivibrator circuit which has a frequency of about 1 Kc. The conditions for oscillation of this circuit are the same as for




**UNIJUNCTION TRANSISTOR MULTIVIBRATOR WITH TYPICAL WAVE FORMS**

**Figure 13.16**

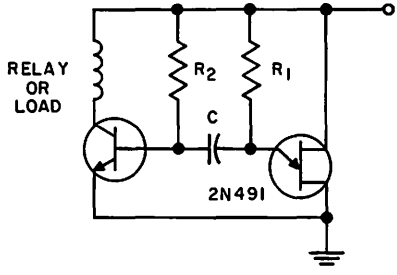
the relaxation oscillator. The length of time during which the unijunction transistor is off (no emitter current flowing) is determined primarily by $R_1$. The length of time during which the unijunction transistor is on is determined primarily by $R_2$. The periods may be calculated from the equations:

$$t_1 = R_1 C \ln\left[\frac{V_1 - V_E}{V_1 - V_p}\right]$$

$$t_2 = R_2 C \ln\left[\frac{V_1 + V_p - V_E}{V_1 - V_p}\right]$$

Where $V_E$ is measured at an emitter current of $I_E = \frac{V_1 (R_1 + R_2)}{R_1 R_2}$ and may be obtained from the emitter characteristic curves.

An NPN transistor may be direct coupled to the multivibrator circuit by replacing the diode as shown in Figure 13.17. This circuit has the advantage that the load does not have any effect on the timing of the circuit.




**UNIJUNCTION TRANSISTOR MULTIVIBRATOR USED TO DRIVE NPN TRANSISTOR**

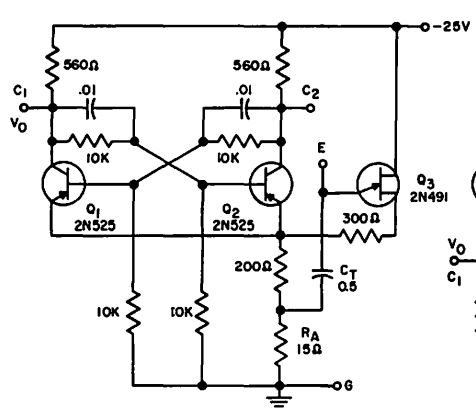
**Figure 13.17**

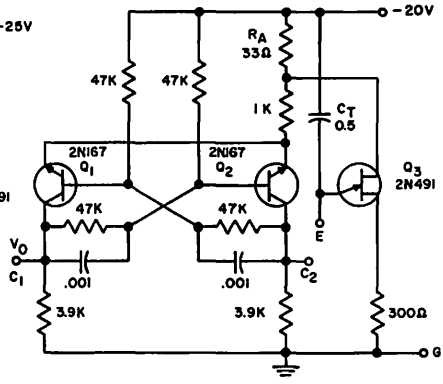
## HYBRID TIMING CIRCUITS

The unijunction transistor can be used in conjunction with conventional PNP or NPN transistors to obtain versatile timing circuits such as symmetrical and unsymmetrical multivibrators, one-shot multivibrators, variable frequency oscillators and time delay circuits. The advantages of these circuits include: (1) The output at the collector of each transistor is very nearly an ideal rectangular waveform. (2) The circuits will tolerate large variations in $h_{FE}$ or $I_{CO}$ of the transistors as compared to conventional circuits. (3) The circuits are not prone to "lock-up" or non-oscillation. (4) The timing stability is excellent. (5) A single small timing capacitor $C_T$ can be used, avoiding the use of electrolytic capacitors in many applications.

The hybrid timing circuits can use either germanium or silicon transistors as desired. The basic circuits for PNP or NPN transistors are shown in Figures 13.18 and 13.19. In both of these circuits, the junction transistors form a conventional flip-flop with the unijunction transistor serving the timing and triggering functions. Each time the unijunction transistor fires the discharge current from the capacitor $C_T$ develops a pulse across $R_A$ which triggers the flip-flop from one state to the other.

The basic circuits as shown in Figures 13.18 and 13.19 will operate at frequencies from about 1 cps to 500 cps and at temperatures above 75°C. Frequencies from 1 cycle per minute to 100 KC can be obtained by proper choice of $C_T$ and $R_A$ and suitable flip-flop design. The operating temperature range may be extended to 150°C by the use of silicon transistors.



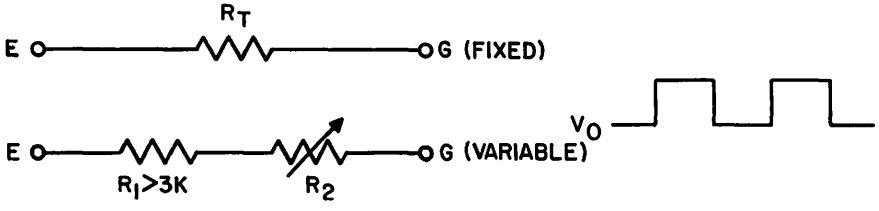




**BASIC HYBRID TIMING CIRCUITS USING PNP AND NPN TRANSISTORS**

**Figure 13.18** **Figure 13.19**

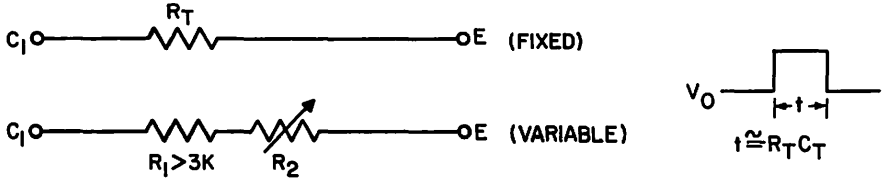
The basic hybrid timing circuits in Figures 13.18 and 13.19 can be adapted to perform desired functions by connecting resistors or potentiometers between the points in the circuit ($C_1$, $C_2$, E, G) as indicated below.

(A) Symmetrical Multivibrator — Square Wave Generator



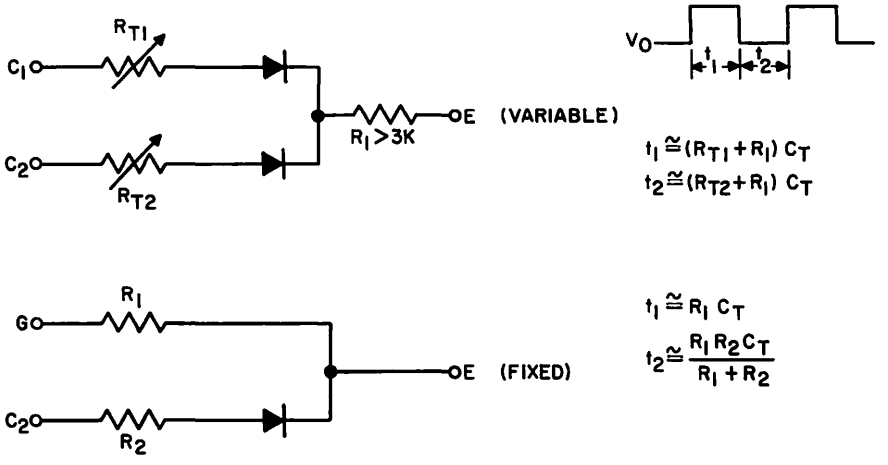

Connecting the resistor between points E and G in the basic circuits gives a square wave generator which has perfect symmetry. By the use of a 2 megohm potentiometer the frequency may be varied continuously from 1 cps to 500 cps. The frequency is $f = 1/2\, R_T C_T$.

(B) One-Shot Multivibrator



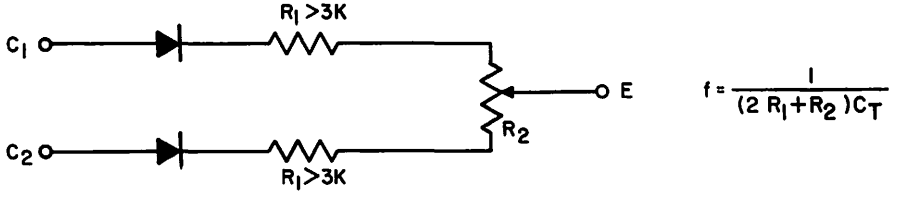

The collector of $Q_2$ will be positive in the quiescent state. A positive pulse at the base of $Q_2$ in Figure 13.18 or a negative pulse at the base of $Q_1$ in Figure 13.19 will trigger the circuit. At the end of the timing interval, the unijunction transistor will fire and cause the circuit to revert to its quiescent state. This circuit has the advantage of a fast recovery time so it may be operated at a high duty ratio without any loss of accuracy.

(C) Non-symmetrical Multivibrator




The timing capacitor $C_T$ will be charged through the resistor $R_{T1}$ or $R_{T2}$ which is connected to the positive collector. The diodes will isolate the other resistor from the timing capacitor. The two parts of the period ($t_1$, $t_2$) can thus be set independently by $R_{T1}$ and $R_{T2}$ and may differ by as much as 1000 to 1.

(D) Non-symmetrical Multivibrator — Constant Frequency




This configuration gives a multivibrator which has a constant frequency but a variable duty cycle.

Further information on the characteristics and circuit applications of the unijunction transistor is given in application note 90.10, "Notes on the Application of the Silicon Unijunction Transistor." Available on written request.

# FEEDBACK AND SERVO AMPLIFIERS — TRANSISTOR CHOPPERS

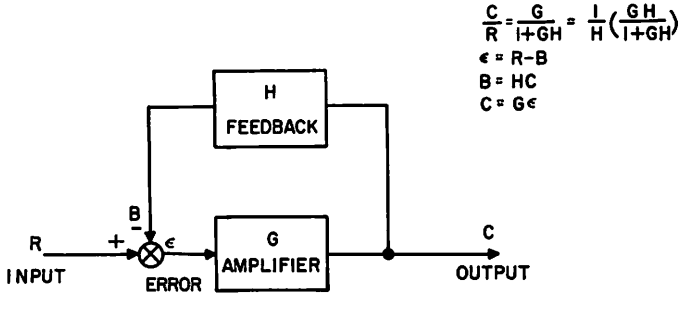
CHAPTER 14

## USE OF NEGATIVE FEEDBACK IN TRANSISTOR AMPLIFIERS

Negative feedback is used in transistor amplifiers to fix the amplifier gain, increase the bandwidth (if the number of transistors is less than three),[1] reduce distortion, and change the amplifier input and output impedances. Feedback is used in servo amplifiers to obtain one or more of these characteristics.

Gain is reduced at the midband frequencies as the feedback is increased, and the predictability of the midband gain increases with increasing feedback. Thus, the greater the feedback, the less sensitive will be the amplifier to the gain changes of its transistors with operating point and temperature, and to the replacement of transistors.

The output and input impedances of the amplifier are dependent upon the type of feedback. If the output voltage is fed back, the output impedance is lowered. In contrast, feedback of the output current raises the output impedance. If the feedback remains a voltage, the input impedance is increased, while if it is a current, the input impedance is decreased.




**SERVO-TYPE FEEDBACK SYSTEM**

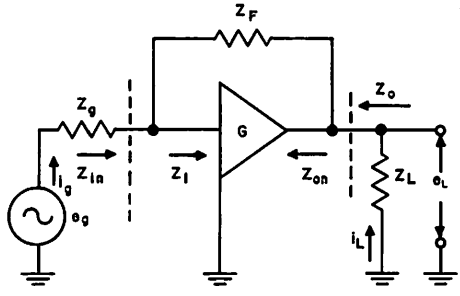
**Figure 14.1**

A convenient method for evaluating the external gain of an amplifier with feedback is the single loop servo-type system as shown in Figure 14.1. (The internal feedback of transistors can be neglected in most cases.) The forward loop gain of the amplifier without feedback is given by G and it includes the loading effects of the feedback network and the load. H is the feedback function, and is usually a passive network. In using this technique, it is assumed that the error current or voltage does not affect the magnitude of the feedback function. The closed loop gain is then

$$\frac{C}{R} = \frac{G}{1+GH} = \frac{1}{H}\left(\frac{GH}{1+GH}\right)$$

where C is the output function and R is the input. If GH is made much larger than one, the closed loop response approaches 1/H and becomes independent of the amplifier gain. Thus, GH determines the sensitivity of the closed loop gain to changes in amplifier gain.

Since GH is a complex quantity whose magnitude and phase are a function of frequency, it also determines the stability of the amplifier. The phase shift of GH for all frequencies must be less than 180° for a loop gain equal to or greater than one or the amplifier will become unstable and oscillate. Therefore, if the number of transistors in the amplifier is greater than two, the phase shift of GH can exceed 180° at some frequency, and stabilization networks must be added to bring the loop gain to one before the phase shift becomes 180°.




(A) BLOCK DIAGRAM

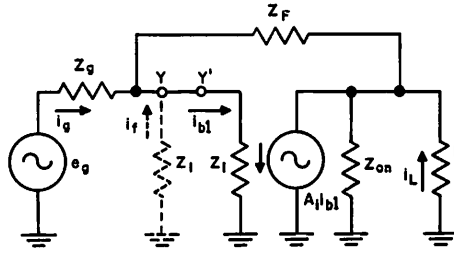
GAIN AND IMPEDANCE RELATIONSHIPS

$$\frac{i_L}{i_g} \approx \frac{\gamma A_i}{1 + \frac{A_i \gamma Z_L}{Z_F}} \approx \frac{Z_F}{Z_L}$$

$$\frac{e_L}{e_g} = \frac{Z_L}{Z_g}\left(\frac{I_L}{I_g}\right) \approx \frac{Z_F}{Z_g}$$

$$Z_{in} \approx \frac{Z_i}{1 + GH} \approx \frac{Z_i}{1 + \frac{A_i \gamma Z_L}{Z_f + \gamma Z_L}}$$

$$Z_o \approx \frac{Z_{on}}{1 + \frac{A_i Z_{on}}{Z_F}}$$




(B) SIMPLIFIED EQUIVALENT CIRCUIT

$$GH = \frac{A_i \gamma Z_L}{Z_f + \gamma Z_L}$$

$$\gamma = \frac{1}{1 + \frac{Z_L}{Z_{on}}}$$

CONDITIONS: $\frac{Z_i}{Z_g} \ll 1$;

$$\frac{Z_i}{Z_F} \ll GH + 1$$

**VOLTAGE FEEDBACK AMPLIFIER**

**Figure 14.2**

Figure 14.2 shows a voltage feedback amplifier where both the input and output impedances are lowered. A simplified diagram of the amplifier is shown in 14.2(B), which is useful in calculating the various gains and impedances. $Z_i$ is the input impedance of the first stage without feedback, and $Z_{on}$ is the output impedance of the last stage without feedback. Ai is the short circuit current gain of the amplifier without feedback (the current in the load branch with $R_L = 0$ for a unit current into the base of the first transistor). Any external resistors, such as the collector resistor which are not part of the load can be combined with $Z_{on}$. The gain and impedance equations shown are made assuming that the error voltage ($i_b Z_i$) is zero which is nearly correct in most cases. If this assumption is not made, the loop gain of the amplifier can be

derived by breaking the loop at y-y' and terminating the point y with $Z_1$.[2] The loop gain is then $i_f/i_{b1}$ with the generator voltage set equal to zero. Since the loop is a numeric, the voltage and current loop gains are identical. The loop gain is then

$$Ai\left(\frac{Z_L'}{Z_L' + Z_F + Z_1'}\right)\left(\frac{Z_g}{Z_g + Z_1}\right) \tag{14a}$$

where

$$Z_L' = \frac{Z_L Z_{on}}{Z_L + Z_{on}} = Z_L\gamma, \text{ and}$$

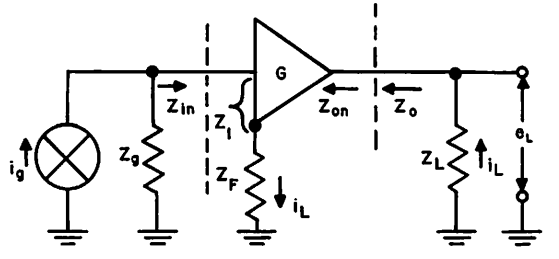
$$Z_1' = \frac{Z_g Z_1}{Z_g + Z_1}$$

Notice that if $Z_g >> Z_i$ and $Z_F >> Z_1$, then the loop gain is very nearly equal to GH as given in Figure 14.2.

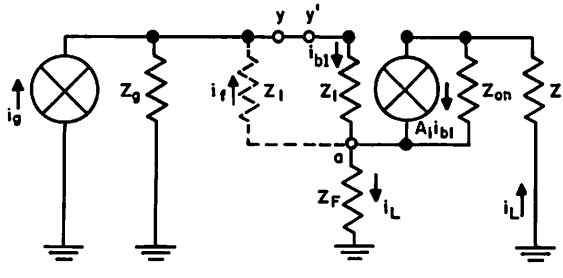
The input impedance of the amplifier is reduced by 1 + GH, while the output impedance is also decreased.

Figure 14.3 shows a current amplifier where both the output and input impedances are increased. The loop is obtained by breaking the circuit at y-y' and terminating points y-a with $Z_1$. The loop gain is $i_f/i_b$ and is approximately equal to

$$\frac{\gamma Ai\, Z_F}{Z_g + Z_1} \tag{14b}$$




(A) BLOCK DIAGRAM




(B) SIMPLIFIED EQUIVALENT CIRCUIT

GAIN AND IMPEDANCE RELATIONSHIPS

$$\frac{i_L}{i_g} = \frac{\frac{A_1\gamma Z_g}{Z_g + Z_1}}{1 + \frac{A_1\gamma Z_F}{Z_1 + Z_g}}$$

$$\frac{e_L}{e_g} = \frac{A_1\gamma Z_L}{1 + \frac{A_1\gamma Z_F}{Z_1 + Z_g}}$$

$$Z_{in} = Z_1\left(1 + \frac{A_1\gamma Z_F}{Z_1}\right)$$

$$Z_o = Z_{on}\left(1 + \frac{A_1 Z_F}{Z_1 + Z_g}\right)$$

$$GH = \frac{A_1\gamma Z_F}{Z_1 + Z_g}$$

$$\gamma = \frac{1}{1 + \frac{Z_L}{Z_{on}}}$$

$$I_g = \frac{e_g}{Z_g}$$

CONDITIONS:

$Z_F << Z_1$; $Z_F << Z_L$

**CURRENT FEEDBACK AMPLIFIER**

**Figure 14.3**

## SERVO AMPLIFIER FOR TWO PHASE SERVO MOTORS

### PREAMPLIFIERS

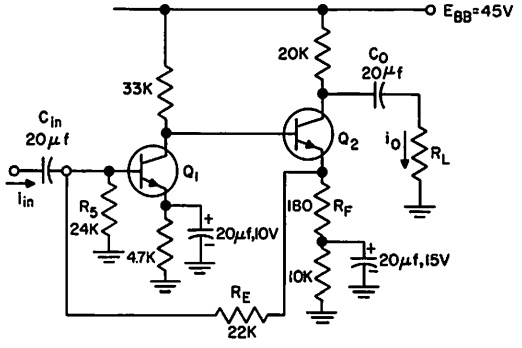
Figure 14.4 shows a two stage preamplifier which has a low input impedance, and which is quite stable in bias point and gain over wide temperature ranges. In addition, no selection of transistors is required.

Because only two stages are involved, the amplifier is stable, and frequency stabilization networks are not required. The current gain $i_o/i_{in}$ is approximately $R_E/R_F$ if the generator impedance and $R_E$ are much larger than the grounded emitter input impedance of $Q_1$. $R_F$ should not exceed a few hundred ohms because it contributes to the loss of gain in the interstage coupling network. The loss of gain in the interstage coupling is

$$K = \frac{Z_{o1}'}{Z_{o1}' + h_{ie2} + h_{fe2} R_F} \tag{14c}$$

where $Z_{o1}'$ is the parallel combination of $R_2$ and the output impedance of Q1. The loop gain then is approximately

$$\left(\frac{h_{fe1} h_{fe2} K R_F}{R_E}\right) \left(\frac{R_5}{h_{ie1} + R_5}\right) \tag{14d}$$




$Q_1 = Q_2$ = G.E. 2N335, 4C30, 4C31, OR 2N336

$$\frac{i_o}{i_{in}} \approx \frac{R_E}{R_F} \text{ FOR } \frac{R_L}{R_4} << 1.$$

**400 CYCLE PREAMPLIFIER FOR OPERATION IN AMBIENTS OF −55 TO 125°C**

**Figure 14.4**

Because the feedback remains a current, the input impedance of this circuit is quite low; less than 100 ohms in most cases. This preamplifier will work well where current addition of signals is desired and "cross-talk" is to be kept to a minimum.

### Bias Design Procedure for Stage Pair

(Reference Figure 14.5)

1. The values of $E_{BB}$, $I_{E1}$, $I_{E2}$, $V_{CE1}$, and $V_{CE2}$ are selected by the designer to be compatible with the constraints imposed by the circuit and component specifications. Thus, $I_{E2}$ and $E_{BB}$ must be large enough to prevent clipping at the output under

conditions of maximum input. For designs which must operate in wide temperature environment, the bias currents and voltages ($I_E$ and $V_{CE}$) of Q1 and Q2 should be approximately equal to those used by the manufacturer for specifying the "h" parameters. (For the 2N335, $I_{E1} = I_{E2} = 1$ ma and $V_{CE} = 5$ to 10 volts.)

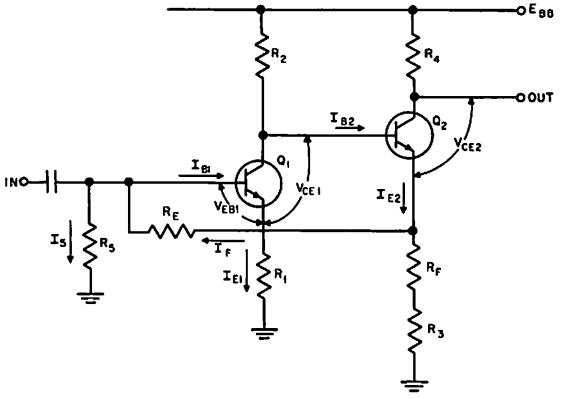



**Figure 14.5**

2. For good bias stability, $I_{E1}$ $R_1$ should be five to ten times $V_{EB1}$, i.e., 3 to 5 volts; thus, knowing $I_{E1}$, $R_1$ can be found. $I_5$ should also be five to ten times larger than $I_{B1}$.

3. $$R_2 = \frac{E_{bb} - V_{CE1} - I_{E1} R_1}{I_{E1} + I_{B1}} \tag{14e}$$

where

$$I_{B2} = \frac{I_{E2}}{h_{FE2}} + I_{CBO2},\ I_{B1} = \frac{I_{E1}}{h_{FE1}} + I_{CBO1}, \tag{14f}$$

and where $h_{FE1}$ and $h_{FE2}$ are the typical D.C. current gains at the particular bias conditions. $I_{CBO}$ is the collector-base leakage current at the temperature and collector-base voltage being used.

4. $$R_5 = \frac{I_{E1} R_1 + V_{EB1}}{I_5} \tag{14g}$$

where $I_5$ is selected to be 5 to 10 times larger than $I_{B1}$.

5. $$R_E = \frac{V_{CE1} - V_{EB1} - V_{EB2}}{I_5 + I_{B1}} \tag{14h}$$

6. $$R_3 = \frac{I_{E1} R_1 + V_{CE1} - V_{EB2}}{I_{E2} - (I_5 + I_{B1})} \tag{14i}$$

7. $$R_4 = \frac{E_{BB} - I_{E2} R_3}{2\, I_{E2}} \tag{14j}$$

8. $$R_F = \frac{R_E}{G_1} \tag{14k}$$

where $G_1$ is the desired closed loop a.c. current gain. (The emitter by-pass capacitors are selected to present essentially a short circuit impedance at the lowest frequency of interest.)

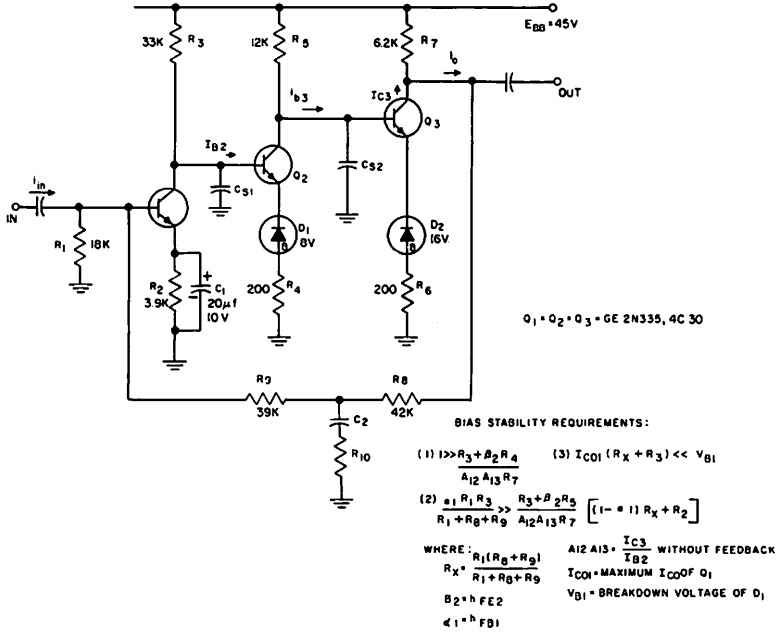
Figure 14.6 shows a three stage, 400 cycle direct-coupled preamplifier with good bias stability from −55 to 125°C. If the dc conditions shown in the figure are met, the collector voltage of Q3 is approximately

$$V_{C3} \approx \frac{[(R_1 + R_8 + R_9)\, R_2]\,(E_C - V_{B1})}{\alpha_1 R_1 R_3} + \frac{(R_1 + R_8 + R_9)\, V_{B1}}{R_1} \qquad (14l)$$

where $V_{B1}$ is the breakdown voltage of the first avalanche diode. The various ac gains and impedances can be calculated from the equations of Figure 14.1 with the exception that the ac feedback is now approximately

$$\left(\frac{R_L'}{R_8}\right)\left(\frac{R_{10}}{R_9}\right) \qquad (14m)$$

where $1/R_L' = 1/R_L + 1/R_{o3} + 1/R_7$, and $R_{o3}$ is the output impedance of Q3. This assumes that the input impedance of Q1 is much less than $R_1$ and $R_9$. The value of $R_{10}$ determines the closed loop gain, while the values of $C_{s1}$, $C_{s2}$, $R_4$, and $R_6$ are used to bring the magnitude of the loop gain to unity before the phase shift reaches 180°. The values required for these capacitors and resistors are dependent upon the maximum expected loop gain.



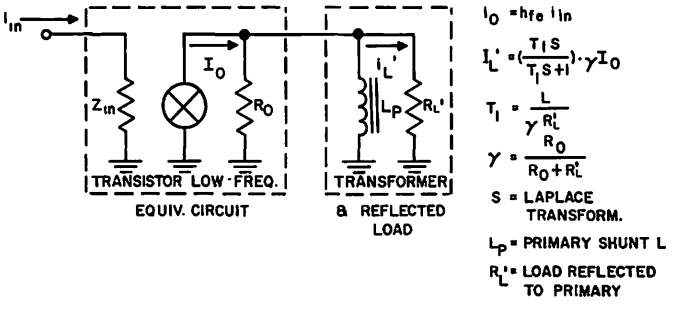

**THREE STAGE DIRECT COUPLED 400 ~ PREAMPLIFIER**

**Figure 14.6**

## DRIVER STAGE

Because the output stages of servo amplifiers are usually operated either Class B or a modified Class B, the driver must provide phase inversion of the signal. In most cases, this is accomplished by transformer coupling the driver to the output stage. The phase shift of the carrier signal in passing through the transformer must be kept small.

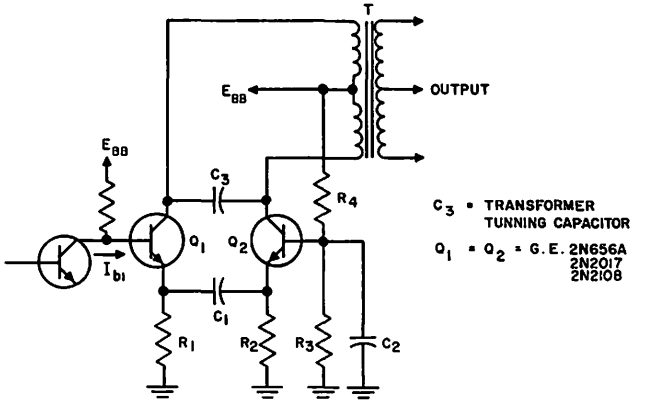
However, since the output impedance of the transistor can be quite large, the phase shift can be large if the transformer shunt inductance is small, or if the load resistance is large as shown in Figure 14.7. The inductance of most small transformers decreases very rapidly if a dc current flows in the transformer. Therefore in transformer coupling, the phase shift of the carrier is reduced to a minimum if the dc current through the coupling transformer is zero, or feedback is used to lower the output impedance of the driver.




**CARRIER PHASE SHIFT DUE TO TRANSFORMER COUPLING**

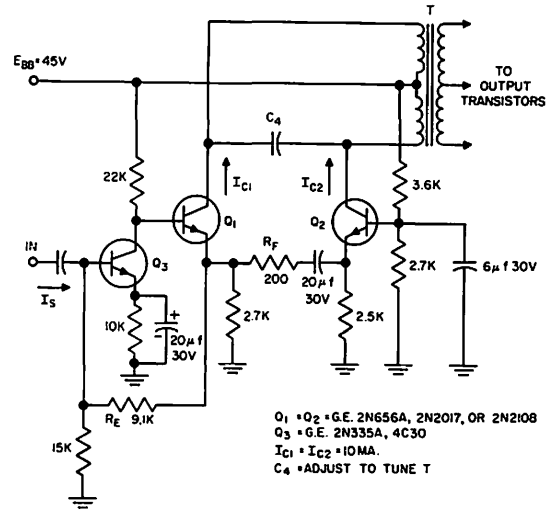
**Figure 14.7**

Figure 14.8 shows a modified "long tail pair" driver. In this case Q1 and Q2 operate Class A, and the quiescent collector current of Q1 and Q2 cancel magnetically in the transformer. Transistor Q1 operates grounded emitter, while Q2 operates grounded base. Separate emitter resistors $R_1$ and $R_2$ are used rather than a common emitter resistor in order to improve the bias stability. The collector current of Q1 is approximately $h_{fe1}\, i_{b1}$, while the emitter current of Q2 is $(h_{fe1} + 1)\, i_{b1}$. Since Q2 operates grounded base, the collector current of Q2 is $-h_{fb2}/(h_{fe1} + 1)\, i_{b1}$ or $-h_{fe}\, i_{b1}$ if the current gain of Q1 and Q2 are equal. Thus push-pull operation is obtained.




**TWO STAGE CLASS "A" PUSH-PULL DRIVER**

**Figure 14.8**




**"STABLE" 400 CYCLE DRIVER**
**Figure 14.9**

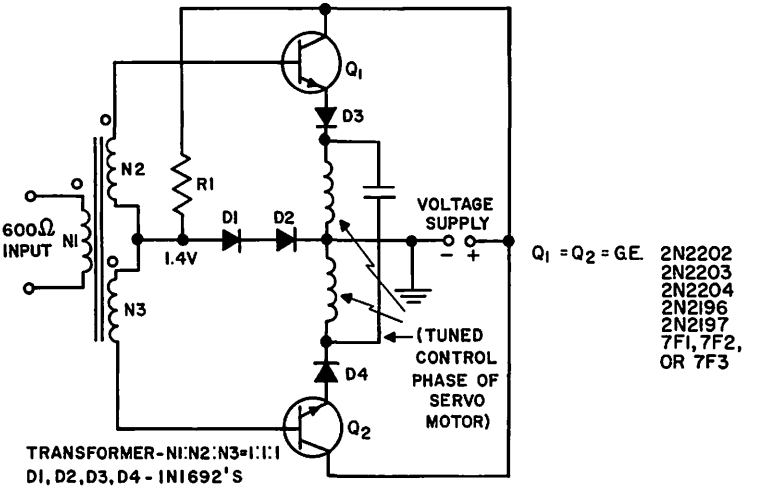
In order to stabilize the driver gain for variations in temperature and interchangeability of transistors, another transistor can be added to form a stage pair with Q1 as shown in Figure 14.9. The gain of the driver is then very stable and is given approximately by

$$\frac{i_{c1}}{i_s} \cong \frac{-i_{c2}}{i_s} \cong \frac{R_E}{R_F} \qquad (14n)$$

## OUTPUT STAGE

The output stages for servo amplifiers can be grounded emitter, grounded collector or grounded base. Output transformers are generally not required because most servo motors can be supplied with split control phase windings. Feedback of the motor control phase voltage to the driver or preamplifier is very difficult if transformer coupling is used between the driver and output stages. If a high loop gain is desired, the motor and transformer phase shifts make stabilization of the amplifier very difficult. One technique which can be used to stabilize the output stage gain is to use a grounded emitter configuration where small resistors are added in series with the emitter and the feedback is derived from these resistors. The motor time constants are thus eliminated and stabilization of the amplifier becomes more practical.

A second technique which results in a stable output stage gain and does not require matched transistor characteristics is the emitter follower (common collector) push-pull amplifier as shown in Figure 14.10. Also it offers the advantage of a low impedance drive to the motor. A forward bias voltage of about 1.4 volts is developed across D1 and D2, and this bias on the output transistors gives approximately 20 ma of no signal current. At lower levels of current the cross-over distortion increases and the current gain of the 2N2202 decreases. D3 and D4 protect the 2N656A's from the inductive load generated voltages that exceed the emitter-base breakdown. The efficiency of this circuit exceeds 60% with a filtered DC voltage supply and can be increased further




**SERVO MOTOR DRIVE CIRCUIT**
**(1 TO 4 WATTS)**

**Figure 14.10**

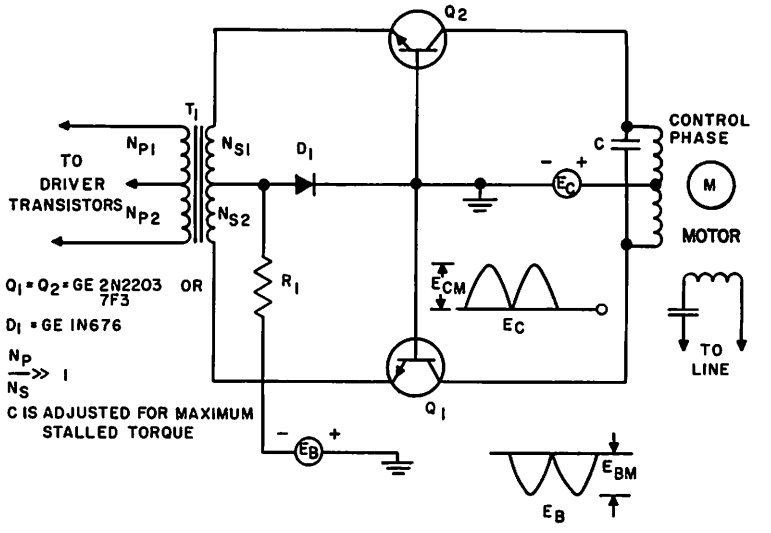
by using an unfiltered rectified ac supply. This unfiltered supply results in lower operating junction temperatures for the 2N2202's, and in turn permits operation at a higher ambient temperature. The maximum ambient operating temperature varies with the power requirements of the servo motor and the type of heat radiator used with the 2N2202. It is practical to attain operation in ambients to 125°C.

Another technique which results in a stable output amplifier gain over wide ambient temperature extremes and which is compatible with low gain transistors is shown in Figure 14.11. In this case, a grounded base configuration and a split control phase motor winding are used. The driver is coupled to the output stage by means of a step-down transformer, and the current gain occurs in the transformer since the current gain of the transistors is less than one. The current gain is $2\alpha N_{P1}/N_{S1}$ if the drivers are operated Class A such as shown in Figures 14.8 or 14.9. The negative unfiltered dc supply and diode D1 are used to operate the transistor Class AB and eliminate cross-over distortion. As the signal increases the diode D1 becomes conductive and shunts the bias supply. The operation of the output stage thus goes from Class A to Class B.

An unfiltered dc is used for the collector supply to reduce transistor dissipation. If saturation resistance and leakage currents are neglected, 100% efficiency is possible under full load conditions with an unfiltered supply. The transistor dissipation is given by

$$P \approx \frac{E_{CM}^2}{4 R_L}\left[a - a^2\left(1 + \frac{R_s}{R_L}\right)\right] + P_L \qquad (14o)$$

where $P_L$ is the dissipation due to leakage current during the half-cycle when the transistor is turned off, a is the fraction of maximum signal present and varies from 0 to 1, $R_s$ is the saturation resistance, $R_L$ is the load resistance, and $E_{CM}$ is the peak value of the unfiltered collector supply voltage. If $P_L$ is negligible and $R_s/R_L \ll 1$, then maximum dissipation occurs at $a = 1/2$ or when the signal is at 50% of its maximum. Thus for amplifiers which are used for position servos, the signal under steady-state conditions is either zero or maximum which are the points of least dissipation.




**GROUNDED BASE SERVO OUTPUT STAGE**

**Figure 14.11**

The peak current which each transistor must supply in Figure 14.11 is given by

$$i_m = \frac{2W}{E_{CM}} \tag{14p}$$

where W is the required control phase power. The transistor dissipation can then be written in terms of the control phase power

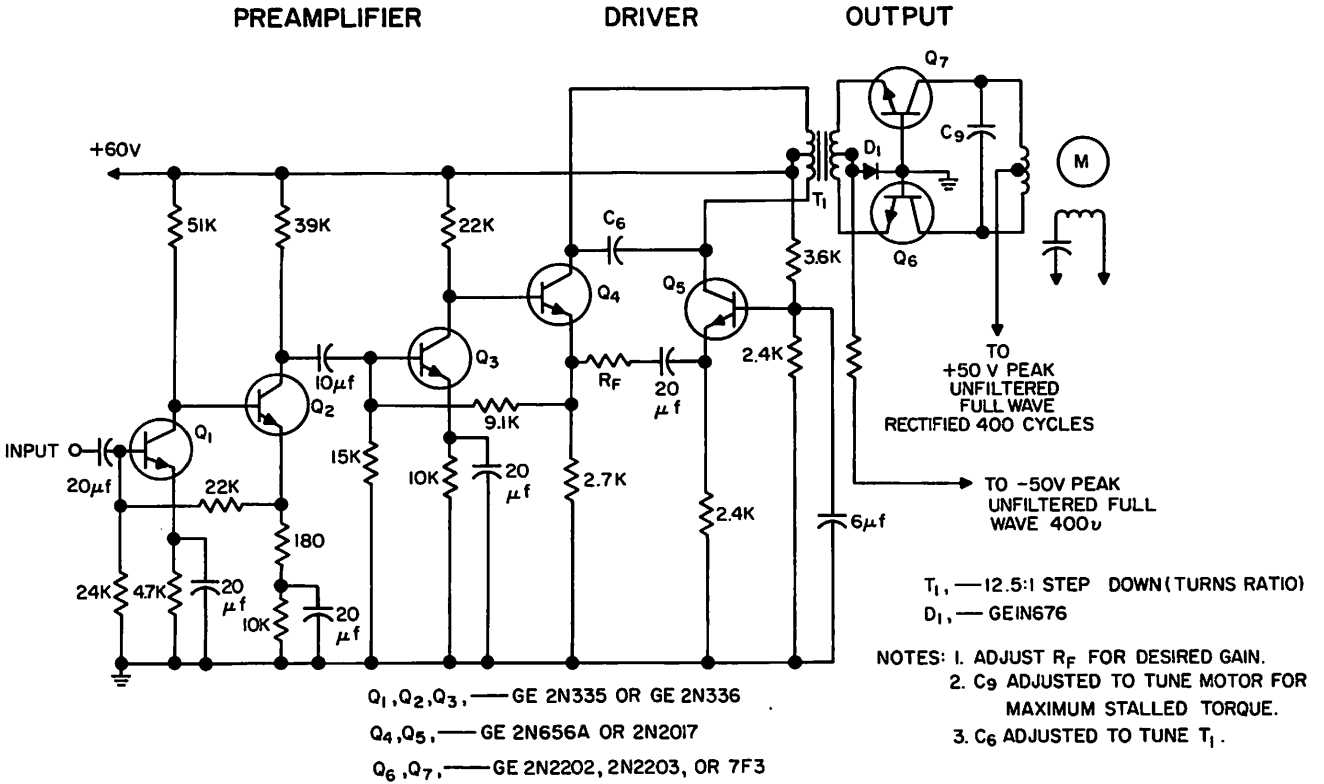
$$P = \frac{W}{2}\left[ a - a^2\left(1 + \frac{R_s}{R_L}\right)\right] + P_T \tag{14q}$$

The driver must be capable of supplying a peak current of

$$\frac{i_m}{\alpha}\left(\frac{N_{S1}}{N_{P1}}\right) \tag{14r}$$

where $\alpha$ is the grounded base current gain of the output transistor.

Figure 14.12 shows a complete servo amplifier capable of driving a 3 watt servo motor in an ambient of −55 to 125°C (if capacitors capable of operation to 125°C are used). The gain can be adjusted from 20,000 to 80,000 amperes/ampere by adjusting $R_F$ in the driver circuit. The variation of gain for typical servo amplifiers of this design is less than 10% from −55 to 25°C, and the variation in gain from 25 to 125°C is within measurement error. The variation in gain at low temperature can be reduced if solid tantalum capacitors are used instead of wet tantalum capacitors. The reason is that the effective series resistance of wet tantalum capacitors increases quite rapidly at low temperatures thus changing the amount of preamplifier and driver feedback. The effective series resistance of solid tantalum capacitors is quite constant with temperature. Many 85°C solid tantalum capacitors can be operated at 125°C if they are derated in voltage.

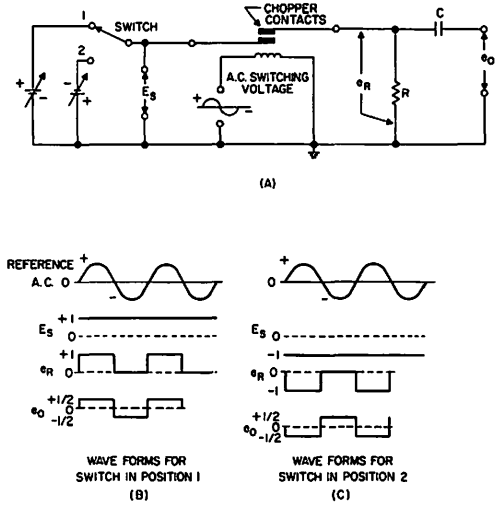



**3 WATT 400 CYCLE SERVO AMPLIFIER FOR −55 TO 125°C OPERATION**

**Figure 14.12**

## JUNCTION TRANSISTOR CHOPPERS

Transistor choppers are used in the amplification of low level d.c. signals, as well as in the conversion of d.c. signals to a synchronous a.c. voltage for driving the control phase of two phase servo motors. The chopper converts the d.c. signal to a synchronous a.c. voltage whose magnitude is proportional to that of the d.c. signal, and whose phase relationship to the reference a.c. voltage is either zero or 180°, depending upon the polarity of the d.c. voltage. This can best be seen by referring to Figure 14.13(A). The chopper contacts close during the positive half cycle of the a.c. reference and open during the negative half cycle. With the switch in position 1, the positive voltage $E_s$ is tied to the resistor R as shown in Figure 14.13(B) during the positive half cycle of the reference. During the negative half cycle of the reference, the chopper contacts are open and the voltage across R is zero. The capacitor removes the d.c. level such that $e_o$ is now an a.c. square wave which in phase with the reference a.c. If the switch is in position 2, the negative voltage $E_s$ is applied to R during the positive half cycle of the reference voltage, and as can be seen in Figure 14.13(C), the output is 180° out of phase with the reference a.c.

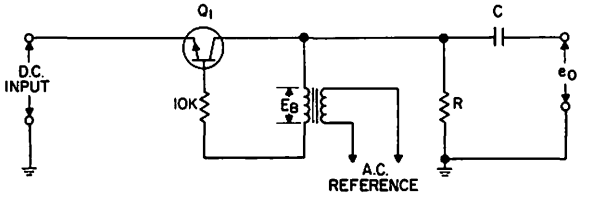



**HALF-WAVE CHOPPER**
**Figure 14.13**

Figure 14.14 shows a single transistor replacing the mechanical chopper. When the base voltage is made positive with respect to the collector (NPN transistor), the transistor behaves as a closed switch, and the d.c. input voltage is connected to R. During the half cycle of the reference voltage when the base is made negative with the supply, the transistor behaves as an open switch, and the voltage across R is zero. However, the transistor is not a perfect switch, and an error voltage and current are respectively superimposed on the d.c. source. During the half cycle that the switch is closed, the error voltage introduced by the transistor is

$$V_{EC} = .026 \ln \alpha N + I_B R_C' \qquad (14s)$$

where $\alpha_N$ is the normal alpha as defined in Chapter 5, and $R_c'$ is the collector bulk or




$Q_1$ = G.E. 2N2193
OR 2N2195
$E_B$ = 5 VOLTS PEAK
SINE OR SQUARE WAVE.

**SIMPLE SERIES TRANSISTOR CHOPPER**

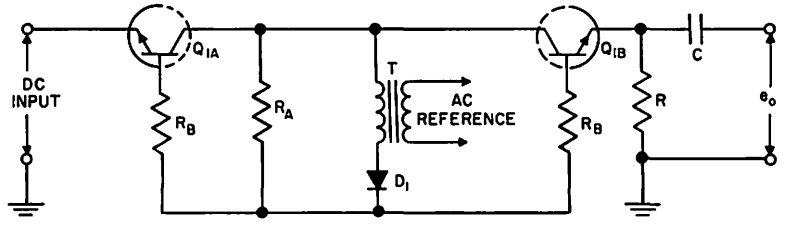
**Figure 14.14**

body resistance. The error current which is introduced when the transistor is an open switch is

$$I_{P1} = \frac{I_{CBO}\,\alpha_I\,(1 - \alpha_N)}{\alpha_N\,(1 - \alpha_N\,\alpha_I)} \qquad (14t)$$

where $\alpha_I$ is the inverse alpha and $I_{CBO}$ the leakage current as defined in Chapter 5.

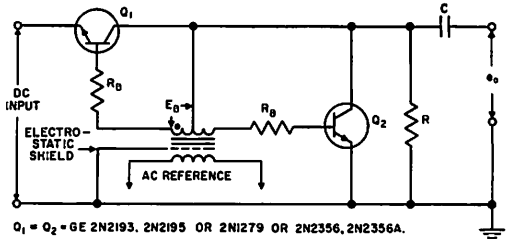
The error voltage introduced by the transistor during the "on" half cycle can be minimized by using two transistors whose offset voltages cancel one another as shown in Figure 14.15. The transistors must not only be matched at room temperature but must track over the required ambient temperature extremes. This is no problem with the G-E 2N2356 planar epitaxial transistor where two transistor pellets are both mounted in the same TO-5 package. Initial offset voltage matches of 50 microvolts or less, and drifts of less than ±100 microvolts over an ambient of −55 to 125°C are easily obtainable. For the G-E 2N2356A the maximum offset between −55°C and 125°C is 50μv. For many applications the drift due to leakage current can be eliminated by using diode $D_1$ and resistor $R_A$ to prevent the collector-base junctions from being reverse biased. This will eliminate any leakage current due to the base drive from flowing in the load. As will be shown below, the emitter-collector impedance will still be quite high.




NOTE:
1. $Q_{1A}$ $Q_{1B}$ −GE 2N2356 OR 2N2356A (TWO MATCHED TRANSISTORS IN ONE TO−5 PACKAGE)
2. ELECTROSTATIC SHIELDING BETWEEN PRIMARY AND SECONDARY WINDINGS OF TRANSFORMER T MAY BE REQUIRED.
3. $R_B$ = 10K, $E_B$ = 10 VOLT PEAK (SINE OR SQUARE WAVE).

**AN IMPROVED SERIES TRANSISTOR CHOPPER**

**Figure 14.15**



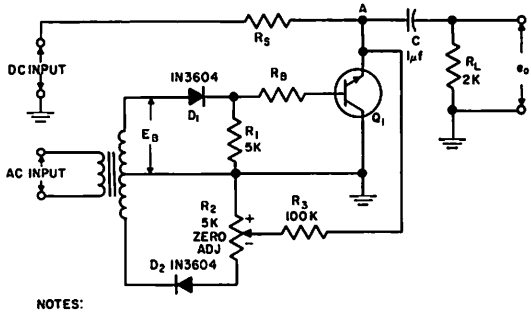

NOTES:
1. $R_B$ = 10K
2. $E_B$ = 7.5 V PEAK SINE OR SQUARE WAVE FOR 2N2193, 2N2194 OR 2N2356.
3. $E_B$ = 1.5 V PEAK SQUARE WAVE FOR 2N1279

**SERIES-SHUNT CHOPPER**

**Figure 14.16**

A chopper configuration[4, 5] which can be used to advantage for a low source impedance input is shown in Figure 14.16. During the half cycle when $Q_1$ is "on," $Q_2$ is turned "off" because its collector-base junction is reverse biased, and R is tied to the d.c. input. On the next half cycle when $Q_1$ is turned "off," $Q_2$ is turned "on," shorting R. The leakage current due to $Q_1$ does not flow through R during this half cycle since $Q_2$ essentially short circuits R. During the alternate half cycle when $Q_2$ is turned "off," its leakage current will flow primarily through $Q_1$ (its turned "on") and the input circuit if R is made much larger than the source impedance. Thus, the drift due to leakage current is minimized. In addition, the offset voltages of the two transistors effectively cancel, even though they occur on separate half cycles. The reason for this is that they form a d.c. voltage which is not chopped and which is not passed by the capacitor, C. An advantage this circuit has over the chopper circuits discussed above is that it is less sensitive to noise pickup because the load always looks back into a low impedance.

Figure 14.17 shows a transistor chopper used for high source impedance applications or those where the d.c. input cannot be loaded. Although $R_s$ is shown as part of the chopper circuit, it can be the d.c. source impedance.




NOTES:
1. $R_S$ CAN BE SOURCE IMPEDANCE OF 50K TO SEVERAL MEGOHMS.
2. $E_B$ = 10 VOLT PEAK SINE WAVE FOR GE 2N2195, $R_B$ = 10K
3. $E_B$ = 10 VOLT PEAK SQUARE WAVE FOR GE 2N1279, $R_B$ = 100K
4. $Q_1$ = GE 2N2195 OR 2N1279

**SHUNT CHOPPER FOR HIGH IMPEDANCE SOURCES**

**Figure 14.17**

Operation of this chopper is basically one of shorting node A to ground each half cycle when the base of the transistor is made positive with respect to ground (the collector). A zeroing adjustment for removing the transistor's offset voltage is provided by $D_1$, $R_2$, and $R_3$ which causes a current to flow during the half cycle from collector to emitter [see equation (5g) in Chapter 5]. In some applications where the 2N2195 is used, the offset voltage is small enough (less than a millivolt) so that the balance network can be eliminated.

On the half cycle of the supply which would normally reverse bias the collector-base junction of Q, the diode $D_1$ prevents this from occurring. The collector-base potential is then zero; however, Chaplin and Owens[6] have shown that the emitter-collector impedance is given by

$$r_{EC} = \frac{0.026}{I_{CBO}} (1 + \alpha_N/\alpha_I - 2\,\alpha_N) \tag{14u}$$

Thus the dynamic impedance is approximately 26 mv. divided by the $I_{CBO}$. For silicon transistors (even at high temperatures) this impedance can be made larger than the load impedance so that the current at node A due to the input d.c. voltage flows into the load during this half cycle. The maximum value of the load is then determined by the minimum value of $r_o$ obtained from equation (14u). Also, any drifts which normally would have been caused by the transistor leakage currents have been eliminated.

For the condition that $r_{EC} >> R_L$, the peak to peak load current is given by

$$I_{p\text{-}p} = \frac{2\,E_{D.C.}}{R_s + 2\,R_L} \tag{14v}$$

The equivalent input current drift due to drift in transistor offset voltage ($\Delta V$) is shown to be

$$I_o = \frac{\Delta V}{R_s} \text{ for } R_s >> R_L \tag{14w}$$

A second component of the chopper drift is due to transient current spikes which occur when the transistor switches "on" and "off." The net area (charge) of the transients develops a potential on the capacitor C which, to the circuit, appears as an input signal. In order to zero the output, a d.c. input current (integrated over one-half cycle) must be provided.

Temperature drift tests made using 2N2195's and 2N1279's show that with the entire chopper of Figure 14.17 exposed to temperature, the required d.c. input necessary to zero the output is less than $10^{-8}$ amperes from −55 to 125°C. This is equivalent to 1 mv of drift referred to the input for $R_s = 100$ K.

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[5] Giorgis, J., and Thompson, C.C., "Silicon Transistor Performance in a Chopper Application," *Applications and Industry*, #37, July 1958.

[6] Chaplin, G.B., and Owens, A.R., "Some Transistor Input Stages for High-Gain D.C. Amplifiers," *The Proceedings of the I.E.E.*, Vol. 105, pt. B, No. 21, May, 1958.

# TRANSISTOR MEASUREMENTS

CHAPTER 15

## INTRODUCTION

Accurate measurements demand a thorough knowledge of measurement principles and pitfalls. To simplify these measurements, such that they are non-discretionary go-no go types, requires in addition, prior information about the device characteristics and their probable distribution. Transistor measurements in particular, due to the extreme power sensitivity of *signal* transistors and the *active amplifier* nature of the device, impose great demands on the skill and ingenuity of the test-equipment designer.

To obtain precision and accuracy in transistor measurements, not only must the definition, meaning, and limits of each test be considered (as well as the actual measurement methods), but attention must also be given to the effect of the measurement upon the device. To illustrate: the transistor is a non-linear device and under normal D.C. bias conditions the Emitter-Base voltage drop in a Germanium transistor is about 250 millivolts. If linear (small-signal) measurements are to be made, it becomes obvious that the rapid curvature of the forward-biased diode characteristic precludes the usual "one order of magnitude less" argument normally applied to signal/bias relationships for small-signal measurements and demands even smaller peak-to-peak signal excursions.

In addition, the transistor is a current amplifier and the effect of the input signal on the output current must be considered. Thus, prior knowledge of probable input impedance and device current gain becomes necessary. For example, assuming an ideal transistor at low frequency and neglecting parasitics, in measuring $h_{ie}$

$$h_{ie} = \left.\frac{e_b}{i_b}\right|_{e_c = 0} \qquad \text{and } h_{fe} = \left.\frac{i_c}{i_b}\right|_{e_c = 0}$$

then,

$$i_b = \frac{e_b}{h_{ie}} \text{ and } i_c = h_{fe}\, i_b$$

from the theory (see any basic transistor text) $h_{ie} = \dfrac{r_e}{(1 - \alpha_o)} \cong h_{fe}\, r_e$

$$\left(\text{since } h_{fe} = \frac{\alpha_o}{(1 - \alpha_o)}\right) \text{ so that } i_c = \frac{e_b}{r_e};$$

also, $r_e = \dfrac{kT}{qI_E}$ (see any basic transistor text) where k = Boltzmann's Constant, T = temperature in degrees Kelvin, and q is the charge of the electron. Now, $\dfrac{kT}{q} = 26 \times 10^{-3}$ volts at room temperature; and, assuming

$$I_C = I_E \text{ (within 10\%)}$$

$$r_e = \frac{26 \times 10^{-3}}{I_C}.$$

$i_c$ is very much less than $I_C$, (say $i_c = .1\ I_C$) for small signal measurements.

Then,

$$i_c = 0.1\ I_C = \frac{e_b}{r_e} = \frac{e_b\ I_C}{26 \times 10^{-3}}$$

or,

$$\frac{e_b\ I_C}{26 \times 10^{-3}} = 0.1\ I_C \text{ whence } e_b \leqq 26 \times 10^{-4}$$

so that the maximum signal swing, $e_b$, should be in the order of 2.5 millivolts and is largely independent of gain or collector current.

However, when the transistor is driven from a current source it is seen that since

$$e_{b\ max} = i_{b\ max}\ h_{ie}, \text{ then } i_{b\ max} = \frac{e_{b\ max}}{h_{ie}}$$

or,

$$i_{b\ max} = \frac{e_{b\ max}}{h_{fe}\ r_e} \cong \frac{25 \times 10^{-4}}{h_{fe\ max} \times \dfrac{25 \times 10^{-3}}{I_C}}$$

whence,

$$i_{b\ max} = \frac{I_C}{10\ h_{fe\ max}}$$

Here a knowledge of the probable range of $h_{fe}$ expected is quite important. Thus, depending upon whether a current source or a voltage source is used in small signal measurements, care must be exercised to insure that small signal conditions truly exist.

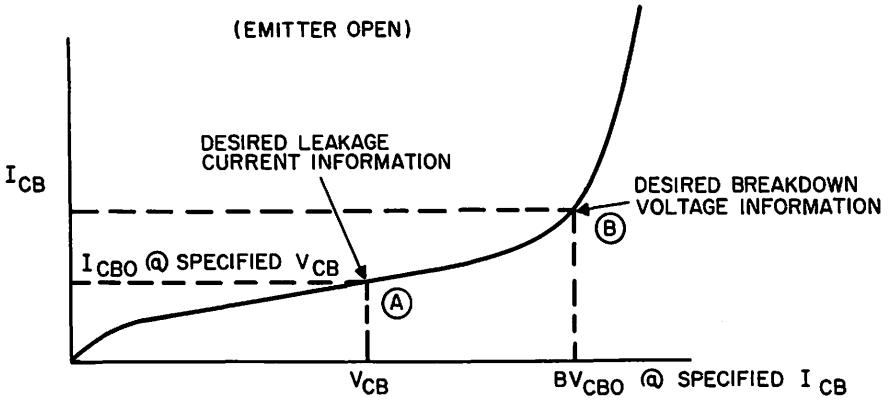
## REVERSE DIODE CHARACTERISTICS

### General

$I_{CO}$ or $I_{EO}$ are the leakage currents within the safe operating region of reverse voltage and are intended to yield comparative, evaluative information as to permissible operation, surface condition and temperature effects on operation.

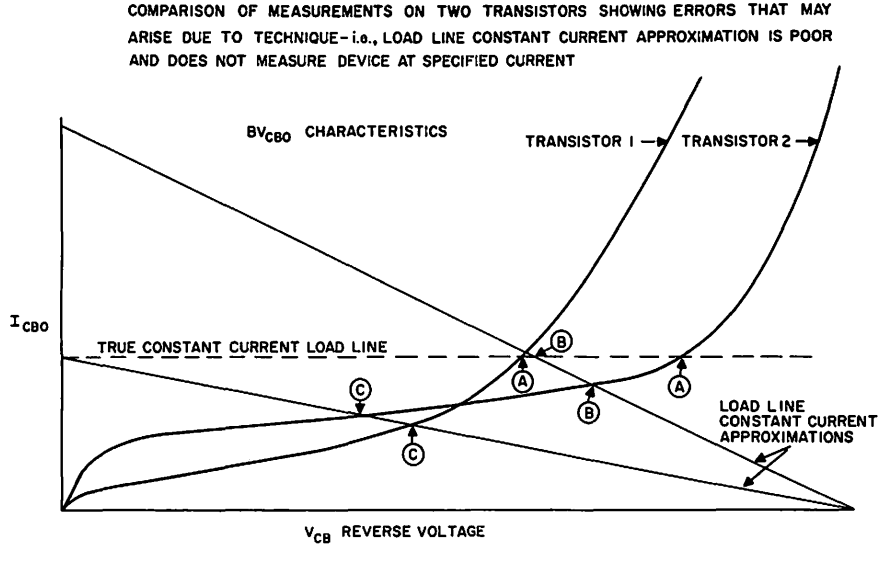
The breakdown voltage tests are indicative of the maximum voltage that can be applied to the device and serve to indicate the voltage at which "avalanche-breakdown" and "thermal-runaway" take place.

The curves of Figures 15.1 and 15.2 are arbitrary but representative ones for transistors and are included to explain what some of the reverse diode characteristic tests mean, and the points at which they are taken. In Figure 15.1, the collector to base reverse voltage of a transistor versus the leakage current is displayed; the points of interest are point A, the leakage current ($I_{CBO}$ in this case) at a specified collector to base junction voltage, and point B, the breakdown voltage ($BV_{CBO}$ in this case) at a specified leakage current. Figure 15.2 illustrates some points which must be considered when accurate breakdown voltage measurements are desired. The two transistors shown have different reverse voltage characteristics. The load line of the measuring instrument which is to approximate a constant current source may give slightly or grossly erroneous readings if care is not exercised in measurement technique. The true values of breakdown voltage are shown at points A. The slightly erroneous readings are at points B on the two characteristic curves while the grossly erroneous data is at points C.




**REPRESENTATIVE COLLECTOR-BASE JUNCTION REVERSE CHARACTERISTICS**

**Figure 15.1**



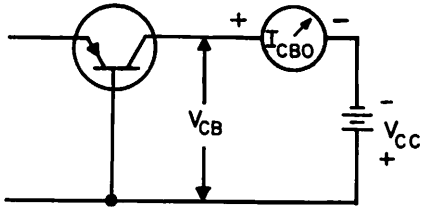

**$BV_{CBO}$ MEASUREMENT TECHNIQUES**

**Figure 15.2**

## D. C. TESTS

The following abstracts include the definitions of particular tests and the associated simplified circuits. The current measuring ($I_{CBO}$, $I_{EBO}$, etc.) circuits are discussed in more detail in the next section.

1. $I_{CBO}$, commonly called $I_{CO}$, is the dc collector current which flows when a specified voltage, $V_{CBO}$, is applied from collector to base, the emitter being left open (unconnected). The polarity of the applied voltage is such that the collector-base junction is biased in a *reverse* direction. (Collector is negative with respect to the base for a PNP transistor.)

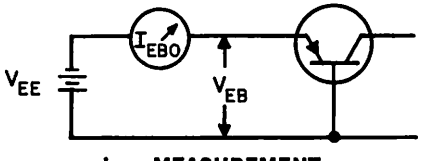



$I_{CBO}$ **MEASUREMENT**

**Figure 15.3**

$I_{CO}$ is greatly dependent on temperature and in some instances, transistors must be handled with gloves to prevent heating the transistor by contact with the operator's hand.

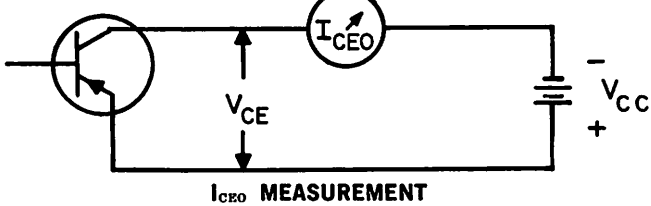
2. $I_{EBO}$, commonly called $I_{EO}$, is the dc current which flows when a specified voltage is applied from emitter to base, the collector being left open (unconnected). The polarity of the applied voltage is such that the emitter-base junction is biased in a reverse direction. (Emitter is negative with respect to the base for a PNP transistor). $I_{EO}$ also is greatly dependent on the temperature and the same precautions apply as for $I_{CO}$ determination.




$I_{EBO}$ **MEASUREMENT**

**Figure 15.4**

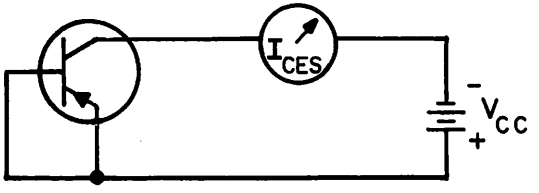
3. $I_{CEO}$ is the dc collector current which flows when a specified voltage is applied from collector to emitter, the base being left open (unconnected). The polarity of the applied voltage is such that the collector-base junction is biased in a reverse direction. (Collector is negative with respect to the emitter for a PNP transistor.) $I_{CEO}$ is greatly dependent on temperature and the operator should use gloves when handling transistor before measuring.




$I_{CEO}$ **MEASUREMENT**

**Figure 15.5**

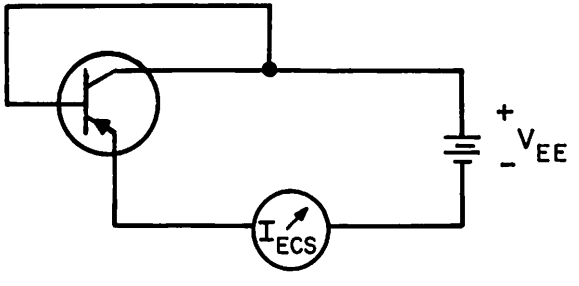
4. $I_{CES}$ is the dc collector current which flows when a specified voltage is applied from collector to emitter, the base being shorted to the emitter. The polarity of the applied voltage is such that the collector-base junction is biased in a reverse direction. (Collector is negative with respect to the emitter for a PNP transistor.)




$I_{CES}$ MEASUREMENT

**Figure 15.6**

5. $I_{ECS}$ is the dc emitter current which flows when a specified voltage is applied from emitter to collector, the base being shorted to the collector. The polarity of the applied voltage is such that the emitter-base junction is biased in a reverse direction. (Emitter is negative with respect to the collector for a PNP transistor.)




$I_{ECS}$ MEASUREMENT

**Figure 15.7**

6. $BV_{CE}$ Tests—$BV_{CEO}$, $BV_{CER}$, $BV_{CES}$, $BV_{CEV}$

A $BV_{CE}$ test is a measurement of the breakdown voltage of a transistor in the common emitter configuration. For the measurement to be meaningful, a collector current *must* be specified.

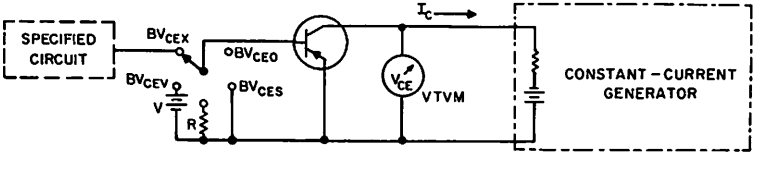



**Figure 15.8**

In measuring $BV_{CE}$ breakdown voltages, a constant value of collector current, $I_C$, is caused to flow in the reverse direction (collector is negative with respect to the emitter for a PNP transistor) and the collector to emitter voltage, $V_{CE}$, is read on the meter. This voltage reading is the $BV_{CE}$ breakdown voltage required.

In addition to a collector current specification, the condition of the base lead must be specified.

a. $BV_{CEO}$ is the common emitter breakdown voltage (for a specified collector current, $I_C$) when the base is left open (unconnected).

b. $BV_{CER}$ is the common emitter breakdown voltage (for a specified collector current, $I_C$) when a resistor of a *specified* value, R, is connected from the base to the emitter.

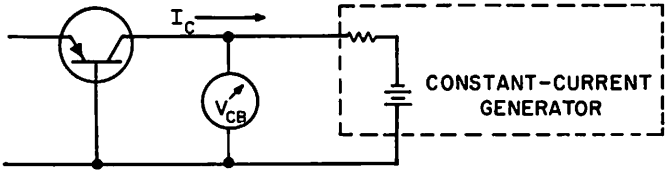
c. $BV_{CES}$ is the common emitter breakdown voltage (for a specified collector current, $I_C$) when the base is shorted to the emitter.

d. $BV_{CEV}$ is the common emitter breakdown voltage (for a specified collector current, $I_C$) when the base is biased with a voltage with respect to the emitter.

e. $BV_{CEX}$ is the common emitter breakdown voltage (for a specified collector current, $I_C$) when the base is terminated through a specified circuit to the emitter.

It should be strongly emphasized that $BV_{CE}$, by itself, is meaningless unless (1) a collector current is specified, (2) the condition of the base lead is specified (by the use of a third subscript), (3) and, if the measurement is for $BV_{CER}$ or $BV_{CEV}$, a definite resistor, R, or a definite voltage, V, are specified, or for $BV_{CEX}$ a definite circuit is specified.

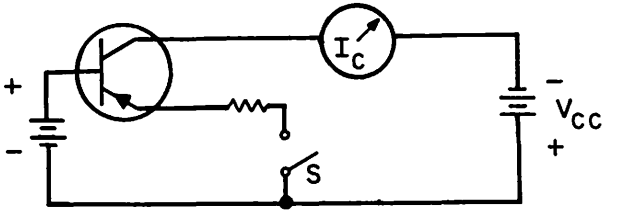
7. $BV_{CBO}$ is a measurement of the breakdown of the collector-base junction with the emitter open. A collector current, $I_C$, must be specified.




**$BV_{CBO}$ MEASUREMENT**
**Figure 15.9**

The emitter is left open (unconnected) as specified by the third subscript. A collector current, $I_C$, is caused to flow through the collector-base junction and the voltage drop $V_{CB}$ is the breakdown voltage, $BV_{CBO}$. Polarity is such that the collector-base junction is biased in a reverse direction (collector is negative with respect to the base for a PNP transistor).

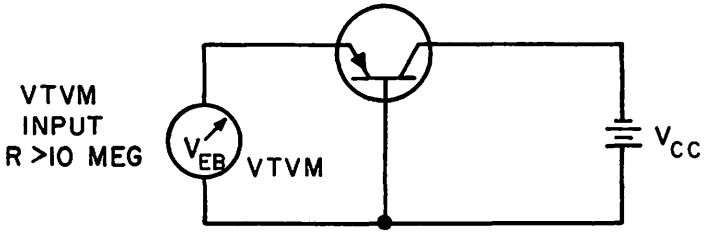
8. $V_{RT}$ (reach through). Reach through voltage is that voltage which, when applied from the collector to base, causes the collector space charge layer to expand into the emitter junction.




**SIMPLE GO-NO GO $V_{RT}$ MEASUREMENT**

**Figure 15.10**

In Figure 15.10, if, when switch "S" is closed, $I_C$ does not increase, the punch through voltage is greater than $V_{CC}$. Punch through may also be measured by the use of the circuit shown in Figure 15.11.

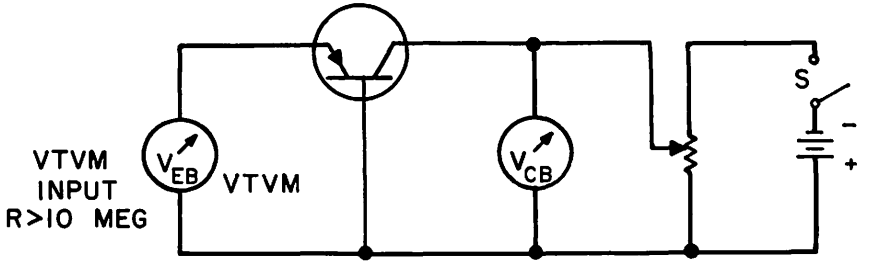



**ALTERNATE GO-NO GO $V_{RT}$ MEASUREMENT**

**Figure 15.11**

If $V_{EB}$ is less than 1 volt, then $V_{RT} > (V_{CC} - 1)$ volts.

The above $V_{RT}$ tests are go-no go in character. By making $V_{CC}$ variable actual values may be determined; for example, in the circuit shown in Figure 15.12 one can adjust $V_{CC}$ until the VTVM reads 1.0 volt, then $V_{RT}$ equals $V_{CB} - 1$ volts.




**$V_{RT}$ MEASUREMENT**

**Figure 15.12**

## CURRENT MEASUREMENTS

1. General

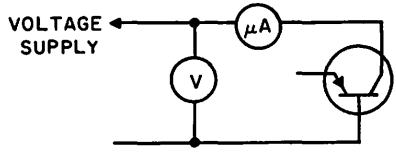
In this section the elaboration of the basic circuit into actual test equipment (both qualitative and quantitative) is delineated. The necessity of saving time in measurement is considered of importance; and means that *constant* voltage and *constant* current techniques will be used. (Constant within the accuracy requirements desired.)

Certain problems arise concommitant with *constancy*. A voltage source, by definition, makes it difficult to limit the current through the ammeter in the event of device failure; and current sources have large open-circuit voltages prior to test, which can be damaging to the operator; and, due to circuit capacity, if the device has an extremely short thermal time constant, the unit under test may be damaged from the large instantaneous currents that can flow.

For the above reasons voltage and current "clamps" are resorted to in order to have the required constancy and are discussed, with their limitations, in conjunction with each class of test.

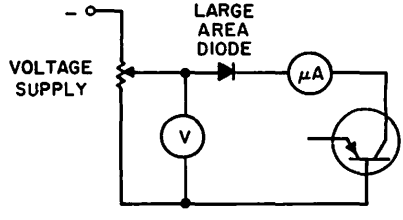
2. Clamp Circuits

In the circuits shown in Figures 15.13 through 15.16, the measurement of $I_{CBO}$ is accomplished. In Figure 15.13, the basic form of the circuit is shown. There is some error in this simple arrangement in establishing the test voltage conditions since there is a small voltage drop across the meter. Also, if a unit is shorted or has an excessively high leakage current, the microammeter may be damaged. For meter protection the circuit of Figure 15.14 is used. The diode used here is a large area diode which has a reverse leakage current greater than that which is intended to be measured. If a 1N91 is used the maximum leakage current which could be measured would be approximately 10 $\mu$a since this is the maximum reverse current which the 1N91 will conduct when a small reverse voltage is impressed across it. To avoid this current limitation and still protect the microammeter the circuit shown in Figure 15.15 is used. This circuit is basically a form of bridge so that if the drop through the limiting resistor is not enough to bring the reference point (the collector) below the clamp voltage, current flows through the diode and the voltage at the reference is that of the clamp supply less the forward drop in the diode.




**BASIC $I_{CBO}$ CIRCUIT**

**Figure 15.13**




**$I_{CBO}$ CIRCUIT WITH METER PROTECTION**

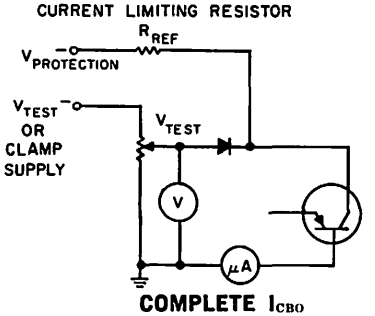
**Figure 15.14**

When the drop through the limiting resistor exceeds the allowed value, the current through the diode tries to reverse; thereupon, the diode becomes back biased and the reference point is driven by a current source, where $I_{limit} = \frac{V_{protection}}{R_{reference}}$ (which is considered a fault condition, but meter protection is accomplished by this current limiting).

Since the current under fault conditions is greater than the desired limit (and it is desired to keep the overload on the ammeter as small as possible) it is desirable to make the protection voltage much larger than the clamp voltage; preferably 10 times larger. The reverse current of the clamp diode at the clamp voltage must be considered, for it adds to the meter overload, and must have a breakdown voltage much greater than the clamp supply. When the currents that are being measured are appreciable (in the order of milliamps) the additional currents flowing through the reference (clamp) supply must be considered. Thus if 1 MA is the limiting current allowed, the clamp bleeder should carry much greater currents (>10 MA) so that the clamp voltage does not change. Where the test voltage is fairly low the drop through the ammeter or reading resistor must be considered for this subtracts from the supply to the tested device.

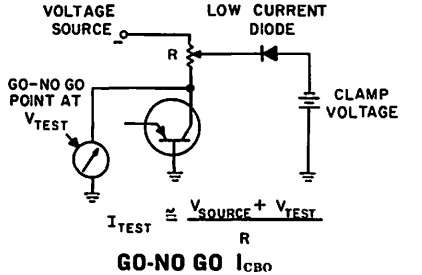
The go-no go test equipment of Figure 15.16 is designed to indicate only that the device possesses specified, or better, characteristics. Generally this type of equipment is designed individually for each requirement and has only limited flexibility.

From the Figure 15.16 circuit go-no go $BV_{CBO}$ tests can be made by using a current source whose value is that at which $BV_{CBO}$ is defined. In this case the $V_{CB}$ voltmeter will indicate that the voltage is less than ($I_{CBO}$ is excessive), equal to, or greater than the required test $BV_{CBO}$ voltage ($I_{CBO}$ is less than the allowed current limit). The current for the voltmeter must be considered, and its accuracy at the limit point ($V_T$) must be checked to put the reject-line on the meter at the correct point. Once this has been done the readings are as accurate as the initial calibration and the stability of the power supply. To prevent overloading the voltmeter and to avoid the large open-circuit voltages at the test point, the current source is often voltage-clamped where the desired test voltage is less than that of the clamp. When this is done the circuit bears a close resemblance to the $I_{CBO}$ test circuit of Figure 15.16.




**COMPLETE $I_{CBO}$ TEST CIRCUIT**

**Figure 15.15**



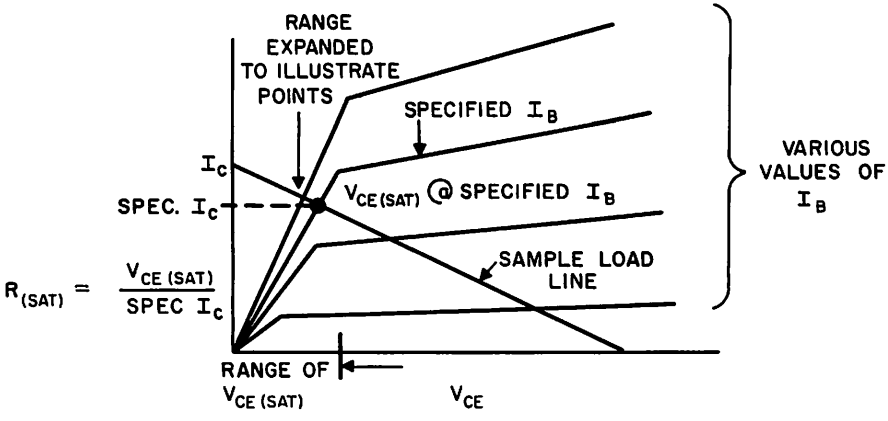

**GO-NO GO $I_{CBO}$ TEST CIRCUIT**

**Figure 15.16**

## LARGE-SIGNAL (DC) TRANSISTOR CHARACTERISTICS

The large-signal transistor characteristics may be divided into two categories with the line of demarcation being the difference between high-frequency pulse response and the DC parameters useful in control-circuit and some computer applications. The pulse response characteristics are discussed in a later section.

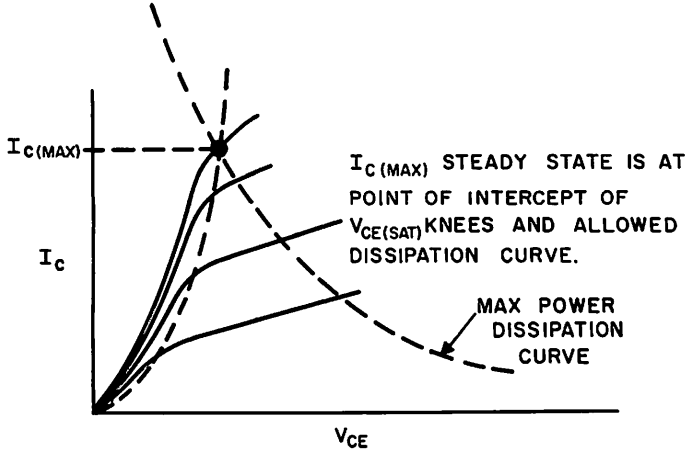
In the following curves Figures 15.17 and 15.18, the significant points of interest are described on the transistor family of curves where $I_C$ vs. $V_{CE}$ is plotted for various $I_B$ values.




KNEES IN $I_B$ FAMILY WILL APPROXIMATELY DESCRIBE A FORWARD DIODE CURVE.

$V_{CE(SAT)}$ AND $R_{(SAT)}$ — FUNCTIONS OF $I_B$ AND $I_C$

**Figure 15.17**

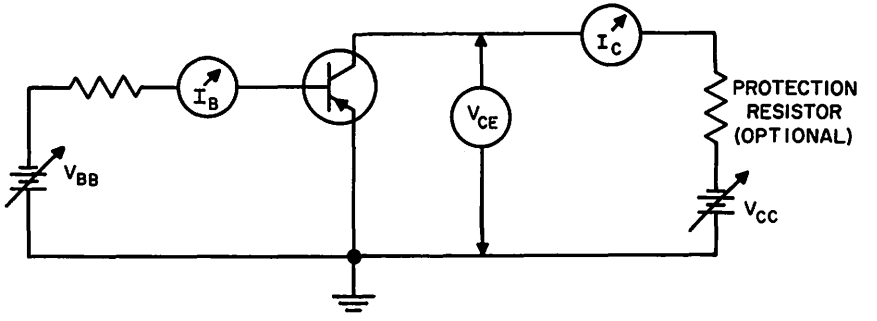



$I_{C(MAX)}$ STEADY STATE

**Figure 15.18**

## LARGE SIGNAL DEFINITIONS AND BASIC TEST CIRCUITS

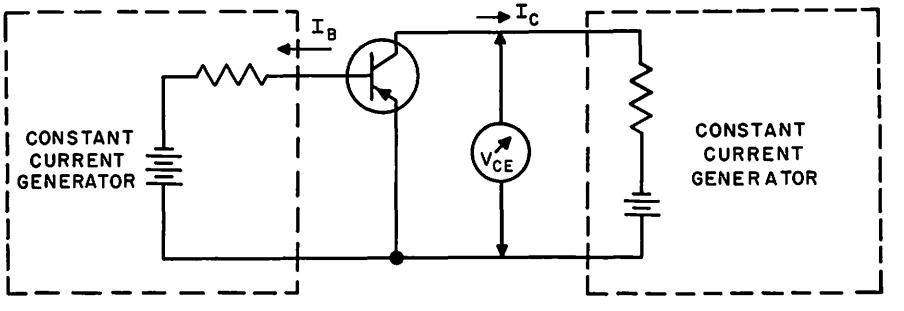
1. $h_{FE}$ is the static value of the forward transfer current gain in the common emitter configuration and is measured as shown in Figure 15.19. It is the DC collector current, $I_C$, divided by the DC base current, $I_B$; $h_{FE} = \frac{I_C}{I_B}$.




**$h_{FE}$ MEASUREMENT**

**Figure 15.19**

The collector voltage, $V_{CE}$, and the collector current, $I_C$, must be specified. A Go-No Go test for $h_{FE}$ may be used, as shown in Figure 15.20.




**GO-NO GO $h_{FE}$ CIRCUIT**

**Figure 15.20**

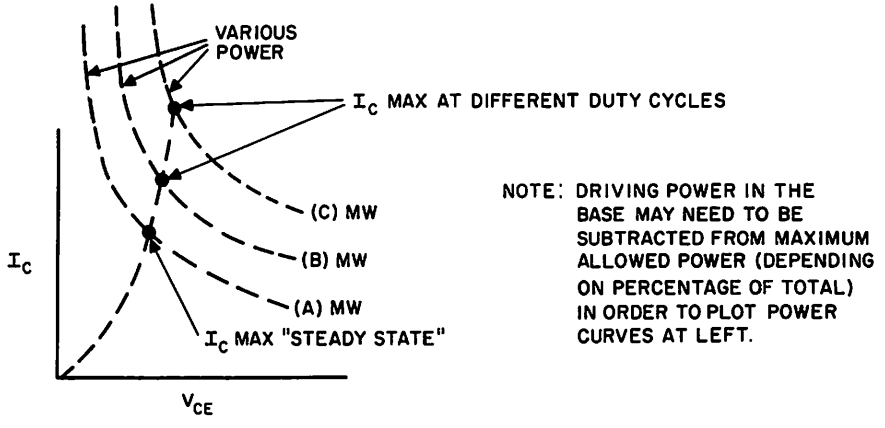
In the method shown in Figure 15.20, $I_B$ is adjusted to give the base current required for an $h_{FE}$ of the required value, $I_C$ is adjusted to the specified value:

$$I_B = \frac{I_C}{h_{FE}}$$

If $V_{CE}$ as read on the meter is less than that given in the test specifications, then the $h_{FE}$ for the transistor is greater than that required. If $V_{CE}$ is greater than the value specified, then $h_{FE}$ is less than the required value.

2. $V_{CE\,(SAT)}$ is the voltage from collector to the emitter, $V_{CE}$, for a given $I_C$ and $I_B$ while biased in the collector saturation region. The test is very similar to that for $h_{FE}$ in Figure 15.20. $I_C$ and $I_B$ are adjusted to their specified values and $V_{CE}$ as read on the meter connected from collector to emitter is $V_{CE\,(SAT)}$.

3. $V_{BE}$ is a measurement of the base to emitter voltage, $V_{BE}$, when in the common emitter configuration and biased according to instructions given in the test specifications. A circuit similar to Figure 15.20 for $h_{FE}$ may be used with the addition of a voltmeter (VTVM) between base and emitter.
4. $h_{IE}$ is the equivalent (slope intercept) resistance equal to $\frac{V_{BE}}{I_B}$. This test is generally made at a specific $I_B$ which is sufficient to saturate the device when it is driven by a specified $I_C$. This information finds maximum applicability in switching and computer applications.
5. $h_{IB}$ is equivalent to $h_{IE}$ except with the transistor operated in a grounded-base configuration. This resistance is an indication of the forward drop in the emitter, and finds application in some power transistor considerations, in bias requirements for some small-signal transistors, and in some regulated power supply applications.
6. $I_{C\,MAX}$ must be considered for two different applications,
   a. Steady state—$I_C$ max. is determined by the intercept of the curve of the "Knees" of the collector saturation points with the maximum allowable power dissipation curve.
   b. The second consideration of $I_C$ max. involves the duty-cycle of the *on* times for switching applications and is dependent on the duty cycle of the circuit being used.



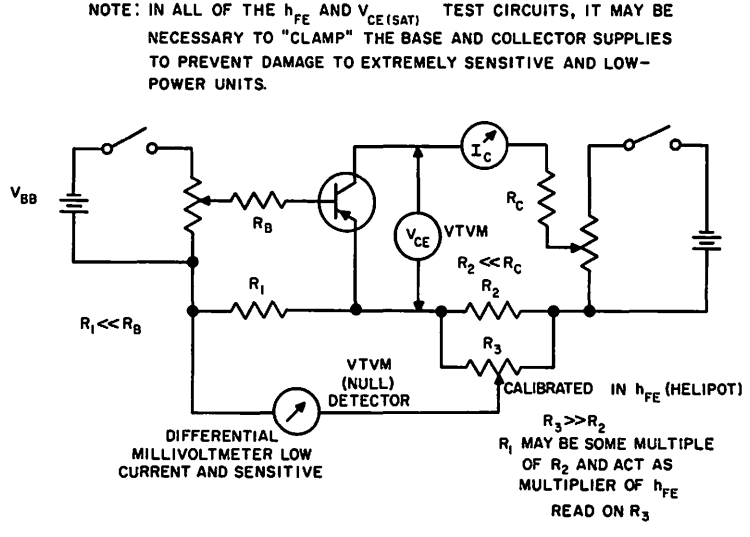

**$I_{C\,MAX}$ CHARACTERISTICS**

**Figure 15.21**

## SOME TEST CIRCUITS

Methods of test and equipment for almost all parameters may be divided into two basic categories: (a) quantitative and evaluative equipment for engineering, and (b) Go-No Go equipment for use when the limits of allowed variance of a particular parameter have been determined and specified. The equipment required for the engineering measurements of DC parameters consist primarily of precise power (current and voltage) supplies, and reliable and precise (as well as often very sensitive) voltmeters and ammeters. The following section will be devoted to both quantitative and Go-No Go equipments and circuits in use.

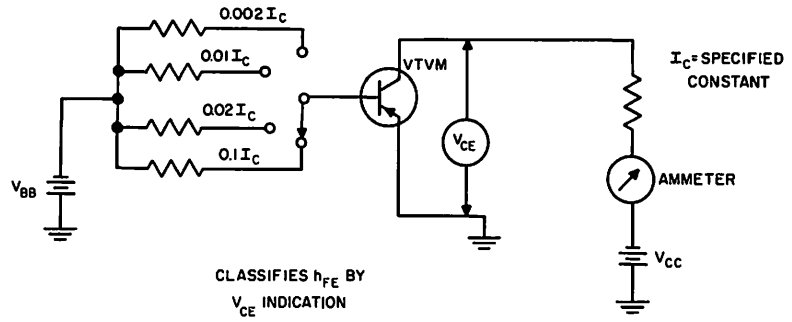
1. $h_{FE}$ measurement is accomplished in the circuit of Figure 15.22. The potentiometers are adjusted in the base and collector circuits to establish the proper measurement conditions; namely, since $h_{FE}$ is a function of both $V_{CE}$ and $I_C$, these two quantities must be specified. When the desired $I_C$ and $V_{CE}$ conditions are established the $h_{FE}$ can be determined. As has been stated $h_{FE} = \frac{I_C}{I_B}$; thus two current reading resistors, $R_1$ and $R_2$, are inserted into the base and collector circuitry respectively. $R_1$ is made very much smaller than $R_B$, and $R_2$ is made very much smaller than $R_C$. Using a Helipot, $R_3$, whose resistance is much larger than $R_2$, the voltage drops across $R_1$ and $R_2$ can be compared. When $R_1$ is equal to $R_2$, for example, and a null is established on the VTVM when the Helipot reads twenty thousandths $\left(\frac{20}{1000}\right)$ of full scale then the $h_{FE} = \frac{1000}{20}$ or 50. If $R_1 = 10\ R_2$, a greater range of the Helipot can be used and, in the example above, a null would be established at two hundred thousandths $\left(\frac{200}{1000}\right)$ on the Helipot indicating $h_{FE} = \frac{1000}{200} \times 10 = 50$. On the physical test equipment the Helipot could be calibrated in $h_{FE}$ for direct reading.




**QUANTITATIVE $h_{FE}$ MEASUREMENT**

**Figure 15.22**

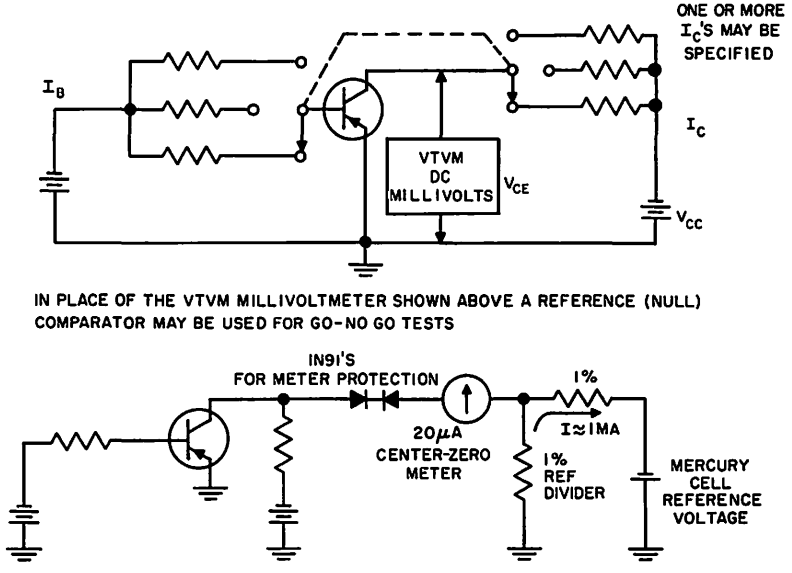
2. $h_{FE}$ Go-No Go equipment is normally built using a constant collector current and classifying $h_{FE}$ according to required base current as shown in Figure 15.23. When the desired $V_{CE}$ and $I_C$ measurement conditions are known, a circuit can be built as shown to classify the devices. If $V_{CE}$ reads below the specified measurement condition, the $h_{FE}$ is greater than that established by the fixed resistors and supplies; if the $V_{CE}$ reads higher than that established as a measurement condition, the $h_{FE}$ is lower than that established by the circuit.




**$h_{FE}$ CLASSIFIER**

**Figure 15.23**

3. The $V_{CE\ (SAT)}$ measurement, Figure 15.24, is often made by applying a specified $I_C$ to the transistor and increasing $I_B$ until an abrupt change in $V_{CE}$ indicates that the collector voltage has dropped below the knee of the collector curve; however, in specifications both $I_C$ and $I_B$ are specified. $I_B$ is usually sufficient to saturate the device; and, in Go-No Go testing, noting that $V_{CE}$ is below some specified voltage, or that it is within certain specified limits is normal procedure. The latter being of particular importance in computer applications where maximum and minimum $V_{CE\ (SAT)}$ values are relied upon. Two circuits in which measurements can be performed are shown in Figure 15.24.




**$V_{CE\ (SAT)}$ MEASUREMENT**

**Figure 15.24**

## JUNCTION TEMPERATURE MEASUREMENTS

### JUNCTION TEMPERATURE ($T_J$)

The measurement of junction temperature, depends on one of two temperature-sensitive mechanisms inherent in the junction device. These are the exponential rise of the reverse diode saturation current, and forward diode voltage decrease with temperature. In most instances experience has shown that calculated theoretical changes of $I_{CO}$ and $V_F$ are too gross (due to rather large "second-order" effects) to be sufficiently accurate indices of junction temperature; and the test device must, in fact, *be calibrated.* This requires that the unit be temperature cycled in an oven (allowing sufficient time for the device to stabilize at each temperature or using a large, high thermal-conductivity heat sink) and a plot of the desired index vs. temperature be made. Power is applied to the device in the forward direction, or through the application of bias current. This power is then momentarily switched off and the built-in *thermometer* checked by a suitably *gated* meter. The *off* time is either kept negligibly small when possible, or else considered in determining the average input power.

Both the $I_{CO}$ and $V_F$ methods are alike in having a large possible error due to the thermal response-time of the device. If the temperature at the junction declines rapidly, the resultant apparent value of $T_J$ will be lower and fall somewhere between the true $T_J$ and that of the thermal mass.

The reverse-current method suffers the additional handicap of charge-storage in the junction when the forward current is reversed. This charge must be swept out by the reverse voltage before a true indication of $I_{CBO}$ can be obtained, a race between charge and thermal decays results. In the large area device of relatively small effective lifetime, the error will probably not be large, but the current metering system must be gated to prevent the charge-decay currents from registering. No peak-reading detectors can be used; although if the charge decays rapidly enough compared to the measuring time, and $T_J$ is reasonably constant during this interval; an average reading metering system is sufficiently accurate, if suitably calibrated.

In the case of the small-area, long lifetime device the problem is more difficult. The masking effect here precludes reverse measurements and only forward measurements are feasible; there are still storage problems, but switching presents the major difficulty. Fast-acting mercury relays are generally used to prevent contact bounce and carry the required currents without large contact drops.

There are decided advantages to using forward voltage drop as the $T_J$ index from the point of view of the circuit requirements. Since the detector (meter) circuit is driven by a voltage source the system is less liable to pick up extraneous hum that can plague the reverse-current measurements. (Particularly when $I_{CBO}$ is low, as in silicon devices, where the current reading resistor is necessarily large.) Unfortunately, however, the change of $V_F$ is comparatively small and the "thermometer" is therefore relatively insensitive. This may require differential amplifier techniques in the detector circuit for precise measurements of $T_J$.

### THERMAL IMPEDANCE

Once a means of measuring $T_J$ has been developed, the measurement of thermal impedance is readily accomplished. The simplest means of measuring the case temperature – such as a thermocouple or large heat sink – may be used, and different powers are fed into the transistor while measuring $T_J$. By defining thermal resistance as the input power required to raise $T_J$ to some arbitrary temperature, (say 70°C) and

measuring this power at different ambients, sink or case temperatures, we may write the following definition:

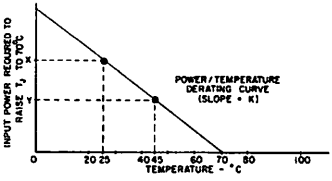
if $x$ watts = 70°C $T_J$ from 25°C $T_{sink}$

and $y$ watts = 70°C $T_J$ from 45°C $T_{sink}$

Then,

$$R_{thermal} = \frac{45° - 25°}{x\text{-}y \text{ watts}} = \frac{20}{x\text{-}y} \text{ °C per watt}$$

we can draw a derating curve through these intercepts as shown in Figure 15.25



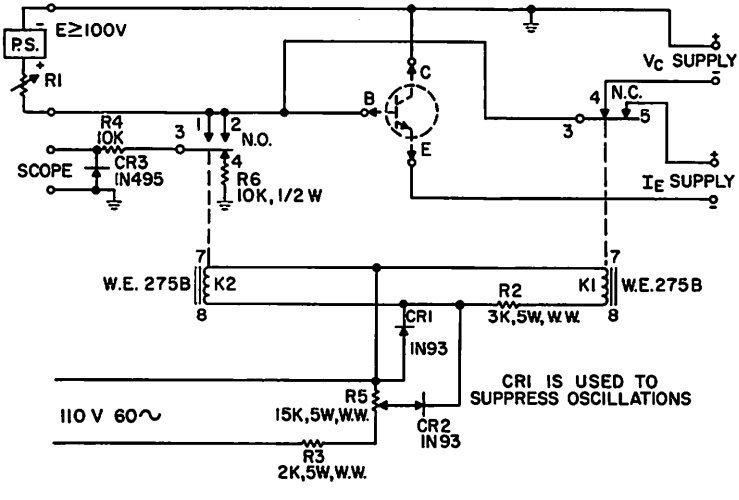

**POWER VS. TEMPERATURE DERATING CURVE**

**Figure 15.25**

## TEST CIRCUIT FOR JUNCTION TEMPERATURE MEASUREMENTS

1. Description of Operation:

Under certain conditions, the forward drop of a semiconductor junction varies linearly with temperature. By setting up these conditions and using a test circuit similar to that of Figure 15.26, it is possible to determine the temperature of a transistor collector junction for various power dissipations in the transistor.

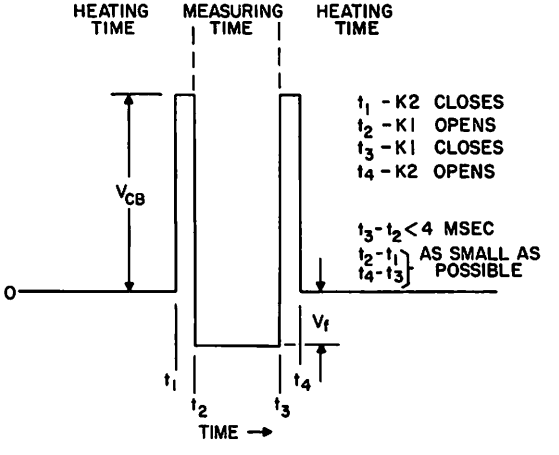



NOTE: POLARITIES SHOWN FOR NPN. TO USE FOR PNP, REVERSE POLARITY OF POWER SUPPLIES AND DIODE CR3.

**THERMAL MEASUREMENTS TEST CIRCUIT**

**Figure 15.26**

The circuit shown is one of several variations which can be used. K1 is a mercury relay (W. E. 275 B type) which interrupts the circuit in which the transistor is heated. K2 is another relay of the same type that puts the transistor in a temperature measuring circuit when it is not in the heating circuit. The relays operate at 60 cps. The transistor under test is heated for about 80% of the time and its forward drop (temperature) measured during the other 20%. If the scope were put directly on contact No. 3 of K2, the presentation would be similar to that shown in Figure 15.27.




**OSCILLOSCOPE PATTERN**

**Figure 15.27**

In this presentation, $V_f$ is the forward drop of the collector junction while it is in the measuring circuit, and $V_{CB}$ is the collector to base voltage while in the heating circuit. The scope vertical amplifier is normally set to the range that will best show the variations in $V_f$. Under this condition, $V_{CB}$ is of such magnitude that it would overdrive the scope and cause distortion of the $V_f$ presentation. To prevent this situation, a clamp consisting of R4 and CR3, is inserted between the scope and contact No. 3 of K2. This minimizes the possibility of overdriving, but still allows the monitoring of $V_f$. Since $V_f$ varies linearly with temperature, the changes in junction temperature can be determined by measuring the changes in $V_f$.

Now, back to the conditions mentioned earlier. The first of these is that the measuring current ($I_f$) through the junction during the measurement must be held constant. This requirement is met by using a power supply (PS) with $V = 100$ volts and a high resistance (R1).

Another condition is that $I_f$ be set to such a value that $dV_f/dT$ will be a constant over a wide range of temperature T. Based primarily on calibration tests of several types of transistors, $I_f$ should be adjusted to give a $V_f \approx 500$ mv at 27°C for silicon junctions and a $V_f \approx 200$ mv at 27°C for germanium junctions. This is accomplished by adjusting the value of R1. Once the conditions are met, the final requirement is that the value of $dV_f/dT$ be known.

$dV_f/dT$ for different transistors can be determined by placing the units in an oven, adjusting $I_f$ to the value specified in above paragraph and then measuring $V_f$ at different oven temperatures. Sufficient time must be allowed for the junction temperature to reach that of the oven as mentioned earlier. This would be the most accurate value of $dV_f/dT$ to use since it is determined for each transistor on an individual basis. A more convenient, but less accurate method, would be to take the average value of several transistors of the same type. Here the accuracy of the value of $dV_f/dT$ would be dependent on the spread, but in general would be within the accuracy of the temperature measuring circuit described.

2. Procedure for Determining Junction Temperature
   a. Determine $dV_f/dT$ for the transistor collector junction.
   b. With $V_C = 0$, and $I_E = 0$ connect transistor to terminals CBE of test circuit. Handle transistor in such a manner that its temperature is not raised above ambient (use gloves, etc.). Adjust R5 for time relationships shown in Figure 15.27.
   c. Adjust R1 for a reading of $V_f$ on the scope equal to 500 mv + (27° — T amb.) × $dV_f/dT$.
   d. Set $V_C$ and $I_E$ to desired bias conditions.
   e. Note change in $V_f$. $T_{junc} = T_{amb} + \frac{(\Delta V_f)}{dV_f/dT}$
3. Procedure for Determining Thermal Resistance from Junction to Ambient
   a. Determine junction temperature as above.
   b. Measure power input to the transistor to give this temperature rise. ($P_{in} = V_{CE}$ max. × $I_E$ max. × duty cycle).
   c. Thermal Resistance from junction to ambient ($\theta_{JA}$) is then computed,

$$\theta_{JA} = \frac{T_J - T_{ambient}}{P_{in}}$$

EXAMPLE:

A 2N657 transistor (a silicon NPN mesa with pellet mounted directly on flat metal header) is calibrated in an oven with $I_f$ adjusted to give a $V_f$ ($V_{CB}$) of 500 mv at 27°C. The slope $dV_f/dT$ was found to be 2.50 mv/°C. It was desired to find what power was required to raise the junction 125°C above ambient and to determine the thermal resistance from junction to ambient at 149°C; room temperature = 24°C.

1. The transistor was connected to the terminals provided on test set up. $V_C = 0$ and $I_E = 0$.
2. R1 was adjusted to give a $V_f$ of 500 + 3° (2.5 mv/°C) or 507 mv. (This took a resistance of nearly 20 megohms.)
3. For the junction temperature to rise 125°C, the voltage $V_f$ in step 2 would have to drop by 313 mv (125 × 2.5). $V_{CB}$ supply was set at 25v. $I_E$ was then increased slowly until $V_f$ dropped to (507 - 313) or 194 mv.
4. The voltage from C to E read with a Weston analyzer was found to be 20.0 volts. (This is an average voltage). The current in the emitter, read with a Weston analyzer in the emitter current lead, was found to be 33.3 ma. (Average value.)

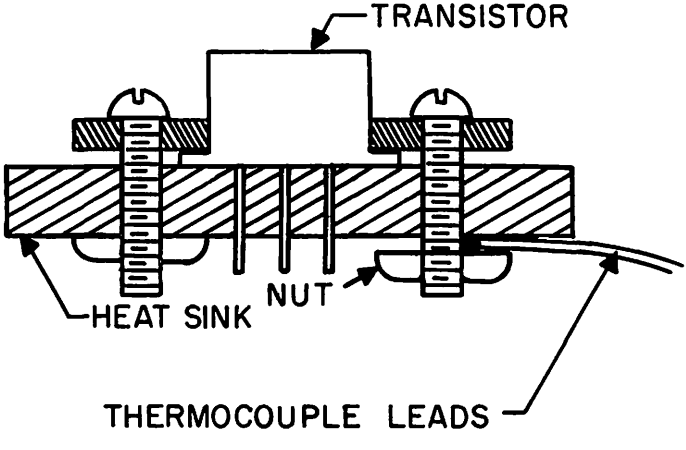
Thus the power dissipated in the transistor was approximately equal to $\frac{20.0 \times 33}{.8}$ or 834 mw. $P_{in} = \frac{I_{av} \times E_{av}}{\text{duty cycle}}$

5. Since $\Theta_{JA} = \frac{T_J - T_A}{P_{in}}$

then $\Theta_{JA} = \frac{149 - 24}{834} = .149°C/mw$

4. Procedure for Determining Thermal Resistance from Junction to Sink

The thermal resistance from junction to sink is a useful parameter for computing operating junction temperature of a sink mounted transistor from the input power and sink temperature. Junction to sink thermal resistance can be calculated using the same procedure as used for $\Theta_{JA}$ with the exception that sink temperature is now used instead of ambient temperature. The heat sink will be more efficient if it is placed in contact with the surface on which the pellet is mounted. For instance, units which have the pellet mounted on the header (such as the 2N657) should have the heat sink placed in contact with the header, giving an excellent thermal path. The contact between the sink and the transistor header could be achieved by holding the unit tightly against a 2" x 2" x ⅝" piece of copper by a steel washer clamped down on the transistor flange. Holes are only large enough so that the insulated transistor leads can pass through. Silicone grease is spread over all contact surfaces to provide a better thermal path between the transistor header and the copper. The sink temperature can now be measured by placing the thermocouple between the bottom of the copper fin and the nut as indicated in Figure 15.28




**THERMOCOUPLE PLACEMENT**
**Figure 15.28**

Once case temperature is established, $\Theta_{JS}$ can readily be obtained by using the same procedure as used to find $\Theta_{JA}$.

## SMALL SIGNAL MEASUREMENTS (AUDIO) OF TRANSISTOR PARAMETERS

The two most familiar matrices (the Z and Y) proved to be difficult to apply to transistors in practice, for driving the collector of a transistor with a current, in measuring $Z_{22B}$, required large source impedances; and driving the input to the transistor with a voltage source, as in measuring $Y_{11e}$, could produce large errors due to the current sensitivity of the device. (Base currents when multiplied by $h_{fe}$ could cause current clipping in the collector.)

To overcome these disadvantages the *h* or hybrid matrix was proposed and became commonly used. The device characteristics that make the *h* matrix most useful at audio and low R.F. frequencies change appreciably as the frequency is increased. Above 30 MCS the terminal requirements become increasingly difficult to obtain; measurements at these higher frequencies will be discussed in next section, (High Frequency Small Signal Measurements of Transistor Parameters).

Consider the terminal requirements of the *h* matrix, and how they may be obtained in practice. The matrix is described as follows:

$h_{11} = e_1/i_1$ when $e_2 = 0$ (Input impedance, short circuit output)

$h_{12} = e_1/e_2$ when $i_1 = 0$ (Reverse voltage ratio, open circuit input)

$h_{21} = i_2/i_1$ when $e_2 = 0$ (Forward current gain, short circuit output)

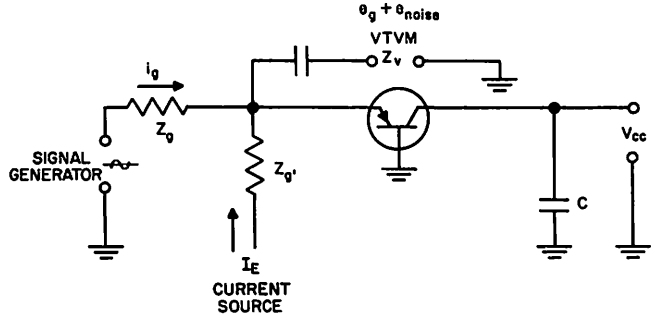
$h_{22} = i_2/e_2$ when $i_1 = 0$ (Output admittance, open circuit input)

These matrix quantities are defined for either common base, common emitter or common collector configuration. Originally 270 cps was the audio frequency used in parameter determination, but today 1 Kc is used more frequently although both are still common.

In establishing the correct a.c. conditions several considerations are of importance. In establishing these conditions, the desired percentage of accuracy will be used as the factor which will determine how well the ideal measurement conditions are realized. 1/(Desired Percentage of Accuracy) will be called $(DPA)^{-1}$; thus, if the desired accuracy is 5% then $\frac{1}{.05} = 20$ or $(DPA)^{-1} = 20$. The following notes on each measurement show where errors may be introduced and indicate what conditions must be established for measurements to be of desired accuracy.

### COMMON BASE CONFIGURATION

1. $h_{1b}$ ($h_{11b}$) $\qquad h_{1b} = \frac{e_g}{i_g}$




$h_{1b}$ MEASUREMENT
**Figure 15.29**

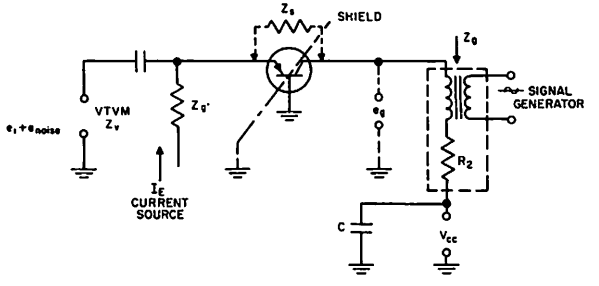
For desired accuracy,

$$\frac{Z_v Z_g Z_g'}{Z_v Z_g + Z_v Z_g' + Z_g Z_g'} \geqq (DPA)^{-1} h_{ib\ (MAX)}$$

$$\omega C \geqq (DPA)^{-1} h_{ob\ MAX} \text{ (for all tests)}$$

$$e_{noise} << e_g h_{ib\ MIN}$$

2. $h_{rb}$ ($h_{12b}$) $\quad h_{rb} = \dfrac{e_i}{e_g}$




**$h_{rb}$ MEASUREMENT**

**Figure 15.30**

$Z_s$ = effective leakage impedance

For desired accuracy,

$$e_g << V_{cb}$$

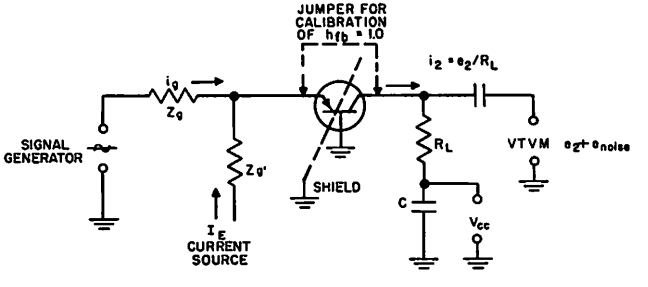
$$I_C R_2 << V_{cb}$$

$$Z_s >> \frac{Z_v Z_g'}{Z_v + Z_g'} \geqq (DPA)^{-1} h_{ib\ MAX}$$

$$e_{noise} << 10^{-4} e_g$$

$$\frac{1}{Z_g} \geqq (DPA)^{-1} h_{ob\ MAX}$$

3. $h_{fb}$ ($h_{21b}$) $\quad h_{fb} = \dfrac{i_2}{i_g}$




**$h_{fb}$ MEASUREMENT**

**Figure 15.31**

$$i_2 = \frac{V_2}{R_L}$$

For the desired accuracy use the same considerations as for $h_{ib}$ and,

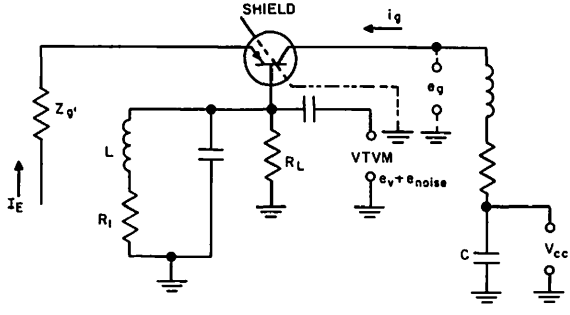
$$\omega C >> \frac{1}{R_L} >> h_{ob\ MAX}$$

($R_L$ is normally less than or equal to 100Ω average)

$$\frac{Z_g Z_g'}{Z_g + Z_g'} \geqq (DPA)^{-1} R_L$$

$$i_g << I_C$$

4. $h_{ob}$ ($h_{22b}$) $\quad h_{ob} = \frac{i_g}{e_g}$ ; $i_g \cong \frac{e_v}{R_L}$ since $i_e$ is small.




**$h_{ob}$ MEASUREMENT**

**Figure 15.32**

For the desired accuracy use the same considerations as for $h_{rb}$ and,

$$e_g\, h_{ob\ MIN}\, R_L >> e_{noise}$$

$$Z_s >> \frac{1}{h_{ob\ MIN}} \geqq (DPA)^{-1} R_L$$

$$[I_{CBO} + (1 + h_{FB})\, I_E]\, R_L << V_{CC}$$

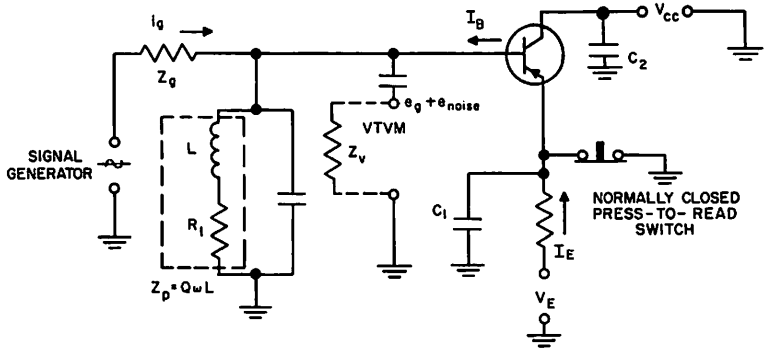
$$Q\omega L \geqq (DPA)^{-1} R_L \text{ at measuring frequency}$$

To satisfy some of the above $R_L$ requirements and yet have $Z_L$ large enough to have sufficient sensitivity; a parallel resonant circuit of low series R is bridged across $R_L$ to reduce the D.C. drop.

## COMMON EMITTER CONFIGURATION

When considering practical measurements of grounded emitter parameters it is also necessary to consider the D.C. bias requirements. It immediately becomes apparent that each transistor will require base bias adjustments to obtain specified base conditions. Since it would be preferable to avoid this time consuming operation and particularly so when many units must be measured, a *Quasi* grounded emitter circuit is used. Through the use of high Q, parallel resonant circuits, the device sees a grounded base bias supply and an A.C. grounded-emitter configuration. Of course this technique is applicable to fixed-frequency measurements only. It is also necessary to consider the current multiplication of input measuring currents appearing in the collector circuit. To maintain *small signal* requirements steps are taken to insure that these collector signal currents will be much less than the D.C. bias currents. (See Introduction, to this chapter.)

1. $h_{ie}$ ($h_{11e}$) $\quad h_{ie} = \frac{e_g}{i_g}$




**$h_{ie}$ MEASUREMENT**

**Figure 15.33**

Coils used are high Q toroids in which D.C. saturation must be considered when certain bias conditions are used.

For the desired accuracy,

$$i_g << \frac{I_c}{h_{fe\ MAX}}$$

$$I_B R_1 << V_{cc}$$

$$\frac{Z_v Z_p Z_g}{Z_v Z_g + Z_v Z_g + Z_p Z_g} \geqq (DPA)^{-1} h_{ie\ MAX}$$

$$\frac{1}{\omega C_1} << r_e \text{ at specified } I_E$$

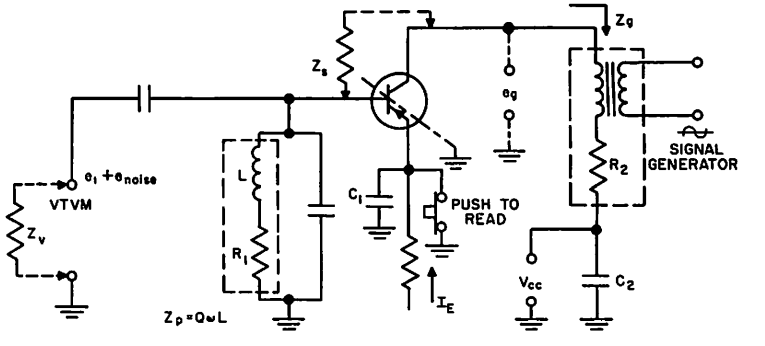
where $r_e \cong \frac{kT}{qI_E} \cong 26\ \Omega$ at $I_E = 1$ ma (see Introduction this chapter)

$$\omega C_2 >> h_{oe}$$

$$e_{noise} << h_{ie\ MIN}\, i_g$$

The press-to-read switch is incorporated to prevent charging $C_1$ to $V_E$ when no transistor is in the socket. Otherwise, the discharge of the capacitor may destroy a unit as it is inserted into the socket for test.

2. $h_{re}$ ($h_{12e}$) $\qquad h_{re} = \frac{e_i}{e_g}$




**$h_{re}$ MEASUREMENT**

**Figure 15.34**

$C_1$, $C_2$, and $R_1$ are the same as for $h_{ie}$

For desired accuracy,

$$I_c R_2 << V_{cc}$$

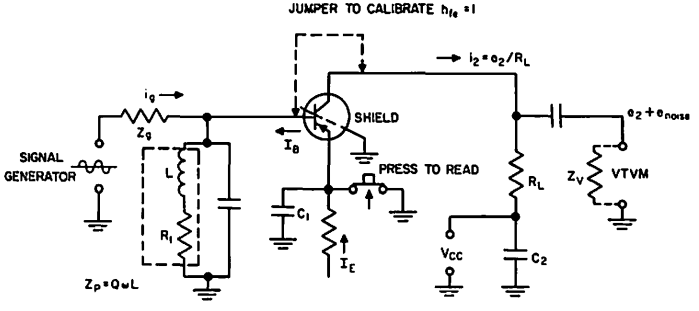
$$e_g << V_{cc}$$

$$Z_s >> \frac{Z_p Z_v}{Z_p + Z_v} \geqq (DPA)^{-1} h_{ie\ MAX}$$

$$e_{noise} << h_{re\ MIN}\, e_g$$

$$\frac{1}{Z_g} \geqq (DPA)^{-1} h_{oe\ MAX}$$

3. $h_{fe}$ ($h_{21e}$) $\qquad h_{fe} = \dfrac{i_2}{i_g}\ ;\ i_2 = \dfrac{e_2}{R_L}$




$h_{fe}$ **MEASUREMENT**

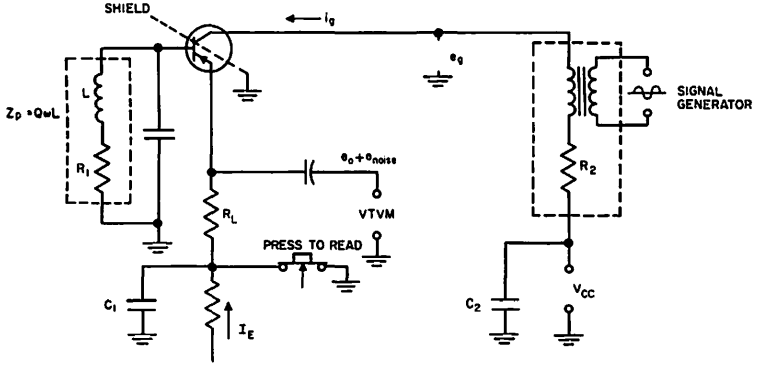
**Figure 15.35**

For the desired accuracy, use the same considerations as for $h_{ie}$ and,

$$e_{noise} << i_g R_L$$

$$R_L << \frac{1}{h_{oe\ MAX}}, \qquad R_L \text{ is generally about } 50\ \Omega$$

4. $h_{oe}$ ($h_{22e}$) $\qquad h_{oe} = \dfrac{i_g}{e_g}\ ;\ i_g \cong \dfrac{e_o}{R_L}$




$h_{oe}$ **MEASUREMENT**

**Figure 15.36**

$Z_g$, $R_1$, $R_2$, $C_1$, and $C_2$ same as for $h_{re}$

For the desired accuracy,

$Z_p >> h_{fe\ MAX} (R_e + R_L)$

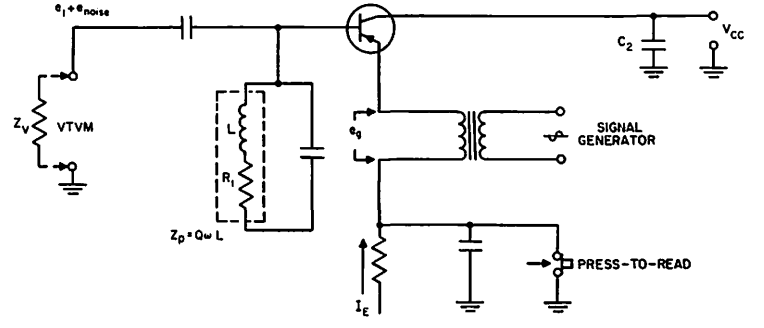
$e_{noise} << h_{oe\ MIN} R_L e_g$

$e_g << V_{cc}$

## COMMON COLLECTOR CONFIGURATION

Common Collector Parameters may be calculated from measurements of common base and common emitter. Notice that the two parameters not identical to those in common emitter configuration are in one case almost equal to $h_{fe}$ and in the other almost equal to 1.

1. $h_{1c} = h_{1e}$
2. $h_{rc}\ (h_{12c})$ $\qquad h_{rc} = \dfrac{e_1}{e_g}$

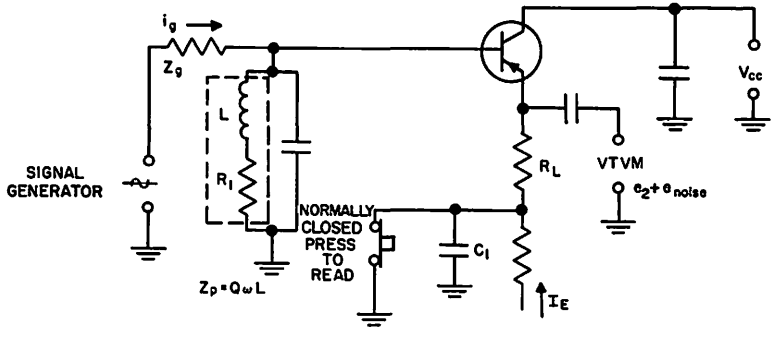



**$h_{re}$ MEASUREMENT**

**Figure 15.37**

Driving conditions are the same as for $h_{re}$; however, $e_g << V_{EB}$, also $h_{re} \cong 1.0$ and deviations from unity are difficult to measure.

3. $h_{fc}\ (h_{21c})$ $\qquad h_{fc} = \dfrac{i_2}{i_g}$ ; $i_2 = \dfrac{e_2}{R_L}$




**$h_{fc}$ MEASUREMENT**

**Figure 15.38**

Driving considerations are the same as for $h_{fe}$ if $R_L$ is kept small; otherwise,

$$Z_p \geqq (DPA)^{-1}(R_e + R_L)$$

$$h_{fc} \cong h_{fe}$$

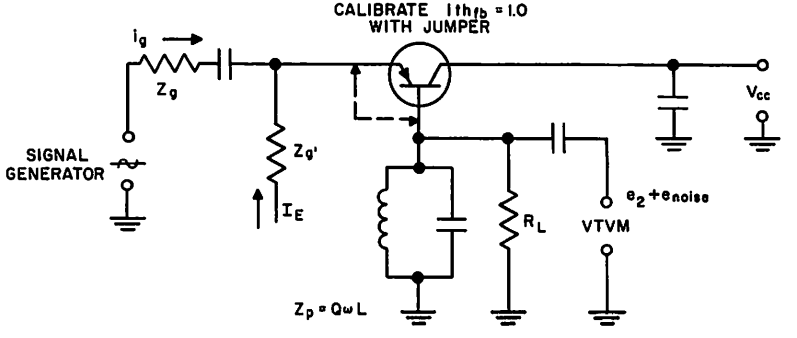
$$h_{fc} = \frac{1}{1 + h_{fb}}$$

4. $$h_{oc} = h_{oe}$$

## GENERAL

Some of the parameters mentioned are particularly difficult to measure, the terminal requirements difficult to obtain, or particularly sensitive to temperature. When measuring $h_{fb}$ it is found that as this parameter approaches unity, the difference is increasingly hard to detect. Instead, $h_{fe}$ could be measured and $h_{fb}$ calculated; or an attempt to measure $1 + h_{fb}$ could be made instead. A circuit for measuring $1 + h_{fb}$ is shown in Figure 15.39.

$$1 + h_{fb} = \frac{i_1}{i_g}, \qquad i_1 = \frac{e_2}{R_L}$$




$1 + h_{fb}$ MEASUREMENT

**Figure 15.39**

Considerations for obtaining accuracy are,

$$\frac{Z_g Z_g'}{Z_g + Z_g'} \geqq (DPA)^{-1}(h_{ib} + R_L)$$

$$Z_p \geqq (DPA)^{-1} R_L$$

$$e_{noise} << (1 + h_{fb\,MAX})\, R_L\, i_g$$

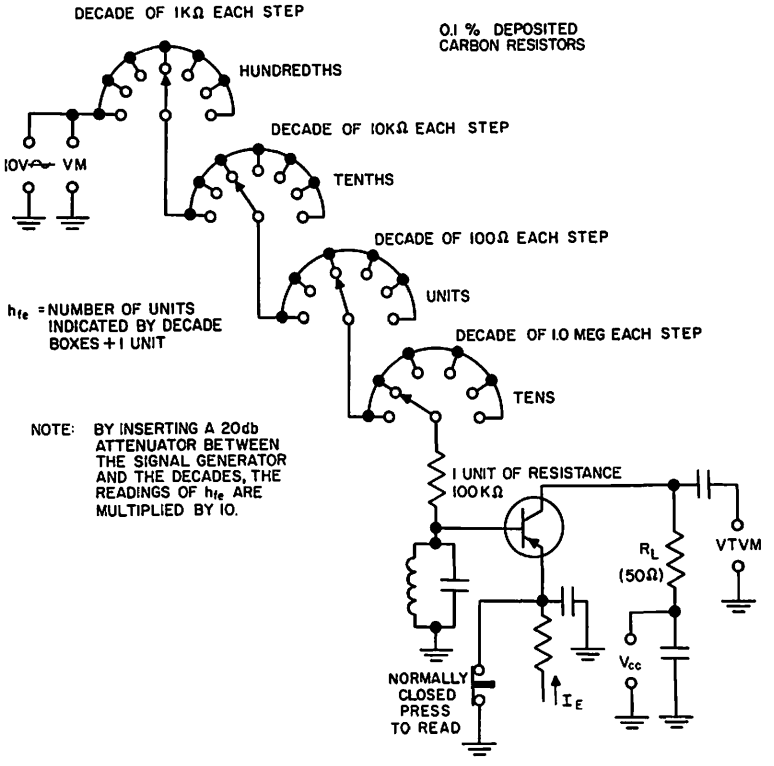
$$\omega C_2 >> h_{oe\,MAX}$$

However, since $R_L$ appears in the collector loop, the collector is not really short circuited, and $R_L$ must therefore be kept quite small. On the other hand, it must be insured that $i_g << I_E$ (in the order of 0.1 ma RMS for 1.0 ma $I_E$). Now the maximum current that will flow through $R_L$ will be $i_g$ when $h_{fb} = 0$, therefore in practice $i_g R_L = 10^{-4} \times 10^2$ or about 10 MV at most. Since, too, it is preferable to measure up to $h_{fb} = .999$, the ability to measure $1 + h_{fb}$ max. $\times$ $i_g R_L$ = about 10 microvolts is necessary. Some available VTVM's do not have sufficient sensitivity for this measurement and either selective VTVM's or pre-amplifiers must be used; at this point, noise and "pick-up" become important considerations.

Similar important considerations also arise in measuring $h_{fe}$. In order to maintain the collector signal current within the required small signal level, one must start with $10^{-4}$ amps and a reading resistor of 50Ω max, assuming 1.0 ma D.C. collector current. This output signal of 5 mv is the maximum signal level in the collector. To measure $h_{fe}$

up to 1000, one would have to insert a base signal current of $10^{-7}$ amps; and calibrating by inserting this signal into the 50Ω resistor, it develops that only 5μv of signal are available and the permissible noise background is less than 0.5 μv.

To illustrate a method whereby most of these difficulties may be eliminated by a different technique of measuring, the circuit of Figure 15.40 is considered.




**ALTERNATE $h_{fe}$ MEASUREMENT**

**Figure 15.40**

In this instance a constant signal voltage (say 10V) and a *Unit* of resistance are used that will limit the signal current to that permissible in the collector circuit. At 50Ω and 0.1 ma a *reference* signal of 5 MV exists, which is readily measurable. The *Unit* of resistance is 100 K. Now *units* of resistance are inserted in the base circuit (AC) until the collector current returns to the Reference level. The number and fractions thereof of Units of resistance will read $h_{fe}$ directly; and the result is that a calibrated decade resistance box is used to read $h_{fe}$. At 1 KC accuracy is not limited by the resistors, but rather by the ½ to 1% resetability of the VTVM pointer. By using a selective VTVM with an expanded scale, such as the Hewlett-Packard 415B, (V.S.W.R. indicator) resetability and accuracy can be improved to better than 0.2%. The limitation now is the accuracy with which the temperature of the unit under test can be maintained since $h_{fe}$ is temperature sensitive.

# HIGH FREQUENCY SMALL SIGNAL MEASUREMENTS OF TRANSISTOR PARAMETERS

## GENERAL

The subject of high frequency *h* parameter measurements is considered in this section. Measurements from 100 kc to above 300 Mc are considered.

1. Common Base - Common Emitter:

   Several considerations must enter into making a small signal measurement other than the high frequency techniques. Of importance is the time required and, in common emitter measurements, the effect of the DC shunt paths. For both of these reasons, all of the common emitter measurements are made in the *Pseudo* grounded emitter configuration where, to D.C., the circuit appears common-base. This was described in the last section. All of the considerations described there are equally applicable at high frequencies.

2. Broad-Band Measurements:

   Common base broad-band measurements are feasible up to 100 mcs with care in circuit layout and due attention to socket capacity, etc. Common emitter measurements are broad-band in a very limited sense. By picking a sufficient number of spot frequencies data are obtained to draw a curve of parameter vs. frequency. The spot-frequency approach results directly from the circuits which will be described.

## INPUT IMPEDANCE: ($h_{ib}$, $h_{ie}$)

1. 200 kc to 5 mcs:

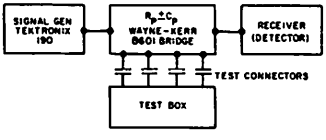
   For this measurement the British Wayne-Kerr Model B601 Bridge was found to be the most suitable. By using suitable multiplier taps it will measure from a few ohms to more than one megohm of R parallel and reactances of $\pm$ several hundred $\mu\mu$f with reasonable accuracy. However, some reactance errors arise in measuring low parallel R values, due to inductance inside the bridge.

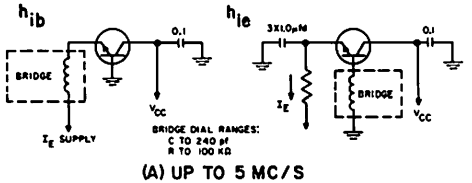
   A receiver is used as the bridge detector. A unit with a few $\mu$v sensitivity and a frequency range of 200 kc to 5 mcs. This detector sensitivity is mandatory, since the maximum signal voltage the bridge applies to the input of the transistor must be less than 5 mv, if overdriving the unit and distortion are to be avoided. Since small-signal conditions are to be maintained, the AC currents permissible should be at most 10% of the DC bias currents. Assuming 1.0 ma $I_E$ and 50 ohms of $h_{ib}$ then the maximum input signal voltage is $10^{-4} \times 50 = 5$ mv. Now for common-emitter operation, (assuming $1 + h_{rb}$ of .01), the base current is $10^{-6}$ amps. For 500 ohm of $h_{ie}$ the maximum signal swing is $10^{-6} \times 5 \times 10^{2} = 5$ mv. These figures are arbitrary, but realizable, and show the need for care. A suitable substitute is to incorporate means of reading the AC current in the collector; and, abiding by the 10% rule, the input signal is adjusted to the maximum permissible. The signal generator used is a Tektronix 190 with the attenuator fixed to limit the input signal to the bridge. Since the Tektronix 190 starts at 375 kc this is the lowest frequency measured. Another generator, such as the Hewlett-Packard 650-A will extend the low frequency range. Test circuits are in plug-in boxes, for connecting to the bridge and are shown in Figure 15.41(A).

2. 1 to 100 mcs:

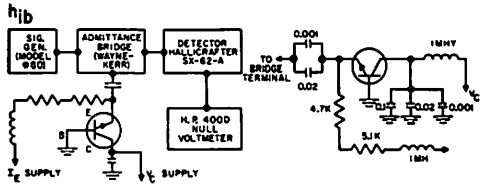
At higher frequency the small signal terminal requirements of $h$ parameters (viz. *Open* and *Short* circuits) are progressively more difficult to obtain. In general, the input impedances are lower due to decreasing current gain and shunt reactance effects. The requirements of low driving signal voltage and the detector sensitivity demanded are even more stringent.

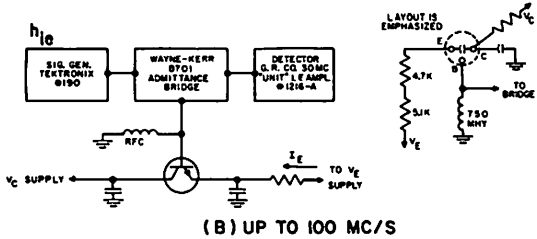
The Wayne-Kerr Model 701B Admittance Meter is used with a Hallicrafter SX-62A receiver as the null detector. Mathematical conversion from the parallel admittances to the required series $R_s \pm jX_s$ will be necessary. The generator used here is a Measurements Corp. Model 80 with a 2 mc to 420 mc frequency range. Since the Wayne-Kerr Model 701-B bridge has a 3:1 step-down transformer built in, the signal input to the bridge is limited to 10 mv maximum. The circuits used in measurements are shown in Figure 15.41(B).




(A) UP TO 5 MC/S




(B) UP TO 100 MC/S

**$h_{ib}$ AND $h_{ie}$ MEASUREMENT**

**Figure 15.41**

3. 30 Mcs and Higher:

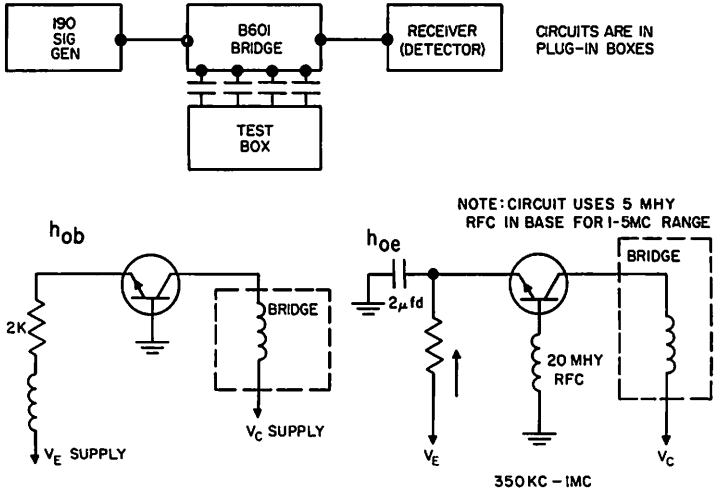
Two different Rohde and Schwartz Diagraphs are being used above 30 Mc. One, Model ZDV, BN3561 operates from 30 to 300 Mc; another, Model ZDD, BN3562 operates from 300 to 2400 Mc. These diagraphs measure the impedance or admittance of an unknown by measuring the reflection coefficient between a reference and an unknown transmission line. All shorts and opens at advanced frequencies can be established by using transmission lines of the appropriate length; that is, an open quarter-wave line is an a.c. short and an open half-wave line is an a.c. open. The system used is basically a 50Ω system and measurement of $h_{ib}$ or $h_{ie}$ may be read directly from the Smith chart display of the diagraph.

## OUTPUT ADMITTANCE ($h_{ob}$, $h_{oe}$)

1. 200 kc to 5 mcs:

The same equipment is used here as for the $h_{ib}$ measurements. However, as much as 1.0 volts rms (although less is preferable) can be applied at the collector. The slope of the characteristic is reasonably constant over a large range of $V_{cc}$.

A conversion from $R_p \pm jX_p$ to $G \pm jB$ is necessary. Circuits are in plug-in boxes.




**$h_{ob}$ AND $h_{oe}$ MEASUREMENT UP TO 5 MC**

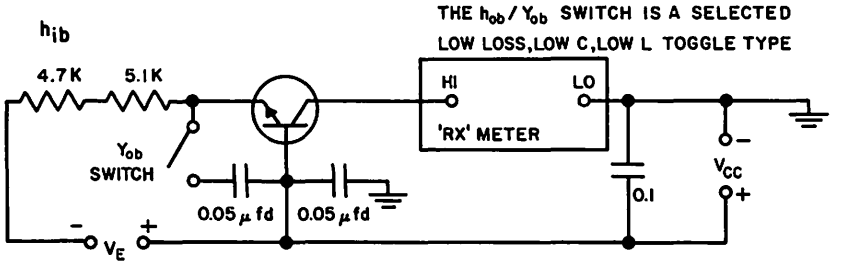
**Figure 15.42**

2. 500 kc to 200 mcs:

The Boonton Radio Corp. Model 250 RX meter is used to make these measurements. The bridge measures $R_p \pm C_p$ and has a built-in signal generator and heterodyne detector. The "RX" meter measures $R_p$ from 15Ω to over 100 kΩ and −80 pf to +20 pf (with means of extending this range by adding external reactance).

Since D.C. currents of up to 50 ma may flow through the bridge, the

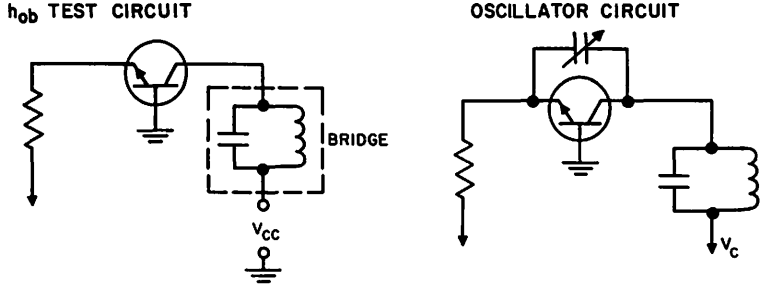
shunt-feed problems are alleviated somewhat, and the entire bias supply is "floated" with respect to the bridge as follows:




**$h_{ob}$ AND $h_{oe}$ MEASUREMENT UP TO 200 MCS**

**Figure 15.43**

The built-in positive feed-back in the common base configuration, due to "overlap" capacity, etc., will often make the resistance term appear negative. The bridge, of course, is not designed to measure —R. Yet by balancing the bridge at R = 10k, for example, and rebalancing with the unit inserted one can calculate the effective —R term. The built-in capacity is sufficient to warrant great care to prevent any more from being added by the external circuit, and a shield between emitter and collector should be included in the physical circuit. A comparison of the measuring circuit of Figure 15.44, and that of an oscillator clarifies the above requirement for minimum capacitance. Also note that $h_{ob}$ may not be measurable at some frequencies, and an a.c. by-pass may be switched in, in order to measure the parallel equivalent of $y_{ob}$, which is also useful in determining $h_{rb}$ at high frequencies.




**COMPARISON OF $h_{ob}$ TEST CIRCUIT WITH THAT OF AN OSCILLATOR**

**Figure 15.44**

3. 30 Mcs and Up:

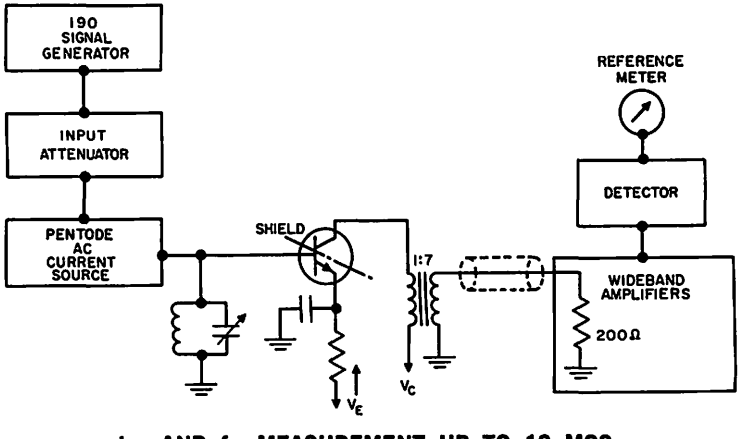
The Rohde and Schwartz Diagraph is also used on output measurements at higher frequencies. However, since the diagraph is a 50Ω system, the resolution above 2.5 kΩ is difficult; thus, on some devices the real part of $h_{ob}$ and $h_{oe}$ may be difficult to determine except to say that it is less than $\frac{1}{2500\Omega}$ or .4 millimhos.

## FORWARD CURRENT RATIO ($h_{fb}$, $h_{fe}$ AND $f_{hfb}$)

Maintaining a high impedance, broad band current source in the presence of capacity is difficult. The problem arises in determining what signal current is being injected into the transistor, i.e., in calibrating the *unity* input current. It is convenient to assume that when the current is jumpered into the collector reading resistor to calibrate the set, this current will then flow into the transistor too. However, even 5 $\mu\mu$f of capacity of the emitter socket has a capacitive reactance of only 1.5 k ohms at 20 mcs, which is not a good current source if $R_L = 25$ ohms and $h_{ib} = 200\Omega$. This can cause a 10% current change, and much larger errors in frequency when measuring $f_{hfb}$, (the slope of $h_{fb}$ with frequency is relatively small) since $\alpha \approx \frac{\alpha_o}{1 + j\frac{f}{f_{hfb}}}$.

Another factor rises which must be considered. The input impedance of the transistor looks inductive below $f_{hfb}$, and at some point becomes resonant with the terminal capacity. If the real part of $h_{ib}$ is larger than the reactive part, then the Q of the circuit exceeds unity and more current flows in the emitter. At this juncture, the current gain appears to exceed unity. It is the nature of $h_{fb}$ to return to unity at high enough frequency, as an examination of the equivalent circuit will show. Of course, $h_{fb}$ could be measured at many frequencies while resonating out the terminal capacity for each step. This is done for $h_{fe}$ and $f_{hfb}$, but is time-consuming. Time consuming, too, is the recalibration operation in $f_{hfb}$ measurements, but this time has been reduced as much as possible in the circuit shown in Figure 15.46. The switching is made automatic, and the gain is changed to correct for the difference between $h_{fb-o}$ (low frequency) and unity. This too is automatically switched between *calibrate* and *measure* positions. With a flat 3 db pad (General Radio type), the detector becomes a reference indicator. Now the frequency is found where both readings are equal.

The phase of $h_{fb}$ at any frequency may be found by using a parallel (and as nearly identical as possible – but without the transistor) channel as a reference. The two channels are amplitude and phase balanced without the transistor. The transistor is then inserted, amplitudes rebalanced, and the peak vector voltage between the




$h_{fe}$ AND $f_{\alpha o}$ MEASUREMENT UP TO 10 MCS

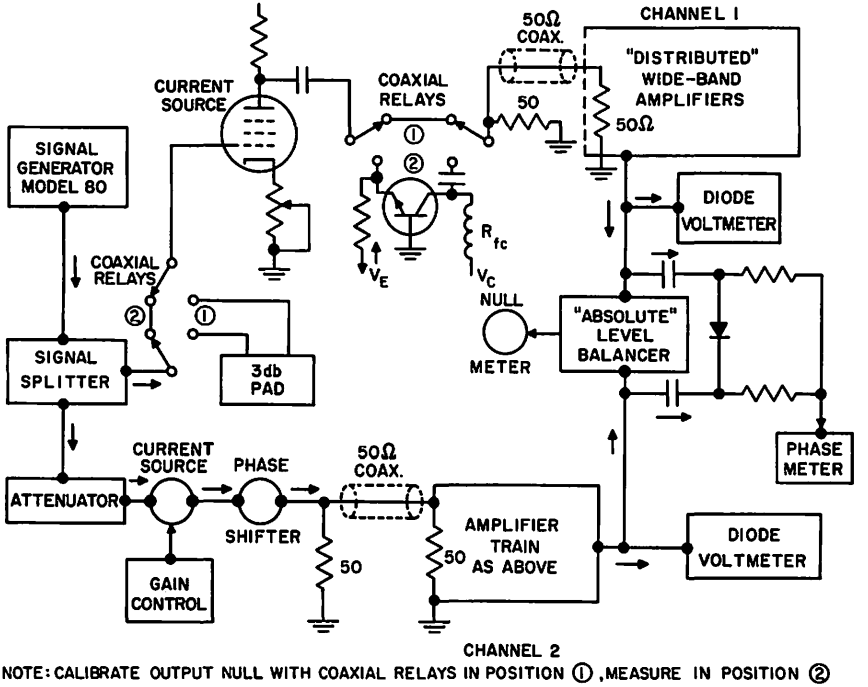
**Figure 15.45**

channels measured. An Advance Electronics Corporation "Vectrolizer" is used. This consists of a peak reading diode differential detector and D.C. amplifier/voltmeter.

The usual considerations of signal currents in the collector still apply. Lead-length is critical in this equipment and *disc* type by-pass capacitors are preferable.

1. $h_{fe}$ and $f_{\alpha e}$ to 10 mcs is measured in the arrangement shown in Figure 15.45.
2. $h_{fb}$, $f_{hfb}$ and phase of $\alpha$ to 100 mcs is measured as shown in Figure 15.46.

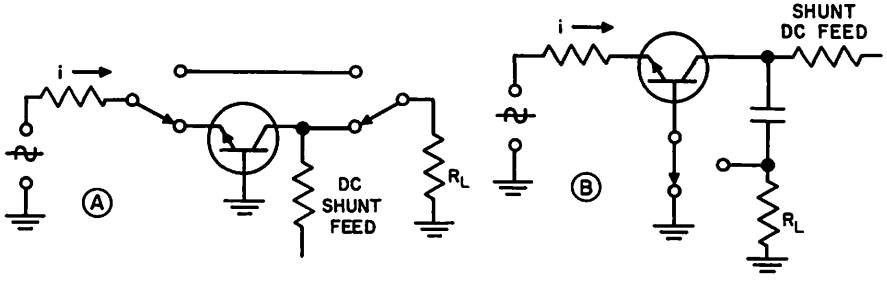
Two basic methods of calibrating *unity* current are shown in Figure 15.47.




NOTE: CALIBRATE OUTPUT NULL WITH COAXIAL RELAYS IN POSITION ①, MEASURE IN POSITION ②

**$h_{fb}$, $f_{hfb}$, AND PHASE OF $\alpha$ MEASUREMENT UP TO 100 MCS**

**Figure 15.46**




**METHODS OF CALIBRATING UNITY CURRENT**

**Figure 15.47**

Signal generators used are either the Tektronix Model 190, up to 50 mcs, or the Measurement Corporation Model 80 up to 100 mcs, and beyond. The distributed amplifiers used are the Hewlett-Packard Model 460A or the Spencer-Kennedy Model 201, the latter having a 200 mcs cut-off frequency. Detectors are the Hewlett-Packard Model 401-B or the Boonton Electronics Company Model 91-B. The "Vectrolizer" has already been described.

Finite termination transfer constants can be measured on the diagraph which when coupled with a knowledge of the other h parameters measured will yield the $h_{rb}$, $h_{rb}$, $h_{fe}$ or $h_{re}$. The computation involved is somewhat long and tedious and with any large number of measurements would almost require a computer. In the measurement of $h_{fe}$ at high frequencies another test facility has been developed which will perform this measurement at certain fixed frequencies. 20, 40, 100, and 200 mcs are currently used. This measurement is essentially used to determine the $f_t$ of a device where $f_t$ is equal to $h_{fe}$ times the frequency of measurement if the $h_{fe}$ vs. frequency characteristic is decreasing at 6 db/octave at the frequency of measurement. $f_t$ is defined as the frequency at which $h_{fe} = 1$.

a. $f_t$ Measurement

In a high frequency mesa transistor, the $f_t$ point or the frequency where $h_{fe} = 1$, usually occurs at a frequency in the order of several hundred megacycles which makes measurement of this quantity quite difficult. This is in addition to the device parasitics interfering with the measurement. To avoid such difficulties, $h_{fe}$, (the short circuit current gain of a transistor), is measured at a fixed frequency somewhat below the $h_{fe} = 1$ value. The $f_t$ point can then be very closely approximated by applying the relationship of $f_t = (h_{fe})(f_{measured})$ as mentioned. In the particular test set described provisions were made to check $h_{fe}$ at two fixed frequencies an octave apart. This, in effect, tells:

1. If the particular transistor under test has any useful gain at these frequencies.
2. If the transistor is following the theoretical 6 db/octave slope.
3. If the second condition holds, what the value of $f_t$ is.

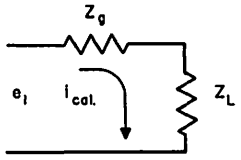
For example, two sets of similar design will be described for two different types of mesa transistors. The fixed frequencies of one are 100 and 200 mcs, and the other, 20 and 40 mcs.

Problems which must be avoided in the measurement of $f_t$ are:

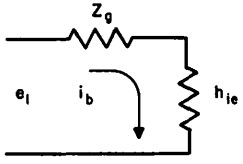
1. The signal level applied to the base must not be too high for a small signal measurement.
2. The signal fed into the base must be a suitable current source.
3. The output reading load must be well defined.

To illustrate where these problems arise, consider the errors in calibration in the input circuit of Figure 15.48, and in the output circuit of Figure 15.49 when the transistor is inserted. Combining these two terms results in Figure 15.50 where the total relationship of *measured* $h_{fe}$ as compared to *actual* $h_{fe}$ is shown.

The object of this measurement is to get the *measured* value of $h_{fe}$ to equal or to approximately equal the *actual* $h_{fe}$ value. Therefore, both the input and output error terms must be minimized; i.e., the variation of the input loop impedance when changing from the calibrating load to the input impedance




$$i_{cal} = \frac{e_1}{|Z_g + Z_L|}$$




$$i_b = \frac{e_1}{|Z_g + h_{ie}|}$$

$$\frac{i_b}{i_{cal}} = \frac{|Z_g + Z_L|}{|Z_g + h_{ie}|} = \frac{\left|1 + \frac{Z_L}{Z_g}\right|}{\left|1 + \frac{h_{ie}}{Z_g}\right|}$$

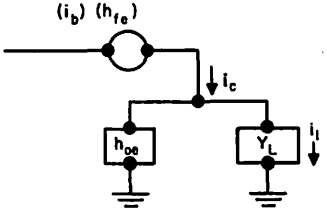
**BASE ERROR TERMS**

**Figure 15.48**

$$i_b = i_{cal}\left(\frac{\left|1 + \frac{Z_L}{Z_g}\right|}{\left|1 + \frac{h_{ie}}{Z_g}\right|}\right)$$

IF $h_{fe} = \frac{i_c}{i_b}$

$$i_c = (i_b)(h_{fe}) = (i_{cal})\left(\frac{\left|1 + \frac{Z_L}{Z_g}\right|}{\left|1 + \frac{h_{ie}}{Z_g}\right|}\right) h_{fe}$$




$$i_1 = i_c\left(\frac{Y_L}{Y_L + h_{oe}}\right)$$

$$i_1 = i_c\left(\frac{1}{\left|1 + \frac{h_{oe}}{Y_L}\right|}\right)$$

$$i_1 = i_{cal}\left(\frac{\left|1 + \frac{Z_L}{Z_g}\right|}{\left|1 + \frac{h_{ie}}{Z_g}\right|}\right)\left(\frac{1}{\left|1 + \frac{h_{oe}}{Y_L}\right|}\right) h_{fe}\ (ACT.)$$

**COLLECTOR ERROR TERMS**

**Figure 15.49**

$$h_{fe}\ (MEAS.) = \frac{i_1}{i_{cal}}$$

$h_{fe}$ (MEAS.) SHOULD = $h_{fe}$ (ACT.)

$$\frac{i_1}{i_{cal}} = h_{fe}\ (MEAS.) = \left(\frac{\left|1 + \frac{Z_L}{Z_g}\right|}{\left|1 + \frac{h_{ie}}{Z_g}\right|}\right)\left(\frac{1}{\left|1 + \frac{h_{oe}}{Y_L}\right|}\right) h_{fe}\ (ACT.)$$

$$h_{fe}\,(\text{MEAS.}) = \left(\frac{\left|1 + \frac{Z_L}{Z_g}\right|}{\left|1 + \frac{h_{ie}}{Z_g}\right|}\right)\left(\frac{1}{\left|1 + \frac{h_{oe}}{Y_L}\right|}\right) h_{fe}\,(\text{ACT.})$$

**ERROR TERMS IN $h_{fe}$ MEASUREMENT**

**Figure 15.50**

of the transistor under test must be minimized and the magnitude of the output admittance, $h_{oe}$, as compared to the load must be minimized. In other words,

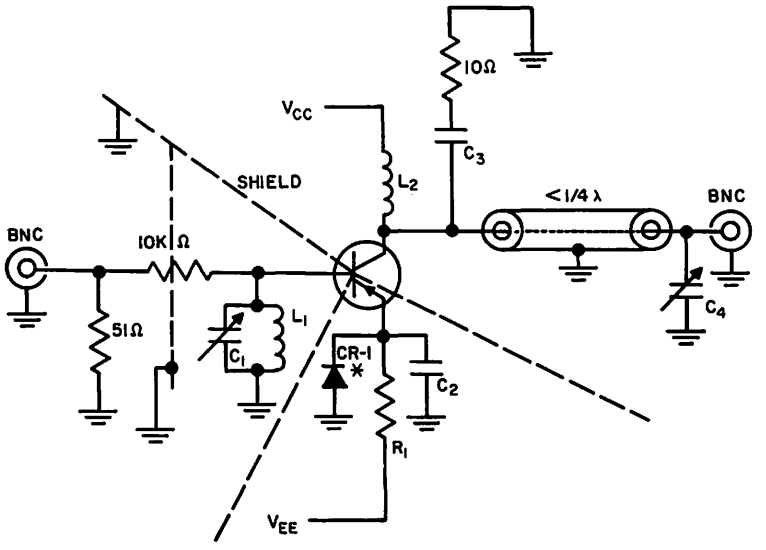
$$\frac{h_{ie}}{Z_g} \text{ and } \frac{h_{oe}}{Y_L} \text{ must be} < 1.$$

The signal current generator uses a 10 K ohm series resistor to the base of the transistor and is placed through a double sided copper clad shield which tends to reduce the shunt capacitance across the resistor since at high frequencies shunt or stray capacities lower the impedance of a current source. To compensate for the residual capacitance in the test set described and therefore raise the current source's effective impedance at the base of the transistor socket, a high Q parallel resonant circuit is placed to ground. (One of the methods which can be used to tune the resonant circuit is to install it physically in the test circuit and then connect an RX Bridge as closely as possible to the base terminal of the transistor socket. Set the $C_p$ dial on the RX meter to 0 pf. Tune the capacitor in the test set and the $R_p$ dial on the RX meter until the meter on the RX bridge nulls. Then read the $R_p$ dial. This is the effective impedance which normally is from 4 to 8 K ohms depending upon the frequency of the test set.)

Some mesa transistors tend to exhibit an output impedance, $1/h_{oe}$, in the order of from 50 to 100 ohms at high frequency. Therefore, in order to measure this type of transistor with accuracy the magnitude of the load admittance terms, $Y_L$, must be greater than 100 millimho (or $R_L < 10\Omega$). In order to realize this condition, transmission line techniques are applied. Not only does the transmission line transform the 3 K Ω resistance of the R.F. millivoltmeter used as a detector to approximately 1 ohm, but the standing wave voltage transformation permits operation at lower signal levels. Effectively a quarter wave transmission line is placed from the collector of the transistor socket to the R.F. millivoltmeter. In practice, it is found much easier to cut a piece of cable shorter than the actual quarter wave length and use a variable ceramic capacitor at the R.F. voltmeter end of the cable to ground. When adjusted, this capacitor electrically extends the line to exactly a quarter wave length.

With mesa transistors in a psuedo-grounded emitter configuration which is used in this circuit, a mesa transistor may break into oscillation. Therefore, a series RC circuit, using a 10 ohm resistor, is placed from collector to ground. This effectively lowers the collector impedance at frequencies other than the frequency of interest and discourages unwanted oscillations.

Figure 15.51 is the diagram of the test set. High frequency construction techniques are used. Shielding is of utmost importance, and the input circuit must be isolated from the output circuit to avoid leakage of signal which could cause a calibration error. (In this case, the base from the collector.) In

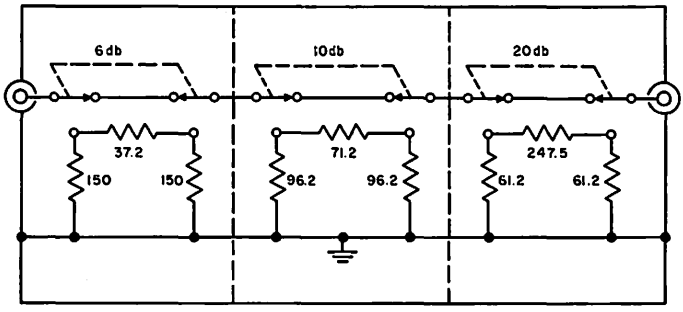



| | 20 MC | 40 MC | 100 MC | 200 MC |
|---|---|---|---|---|
| $C_1$ | 3-12 pf | 3-12 pf | 1.5-7 pf | 1.5-7 pf |
| $C_2$ | 0.1 μf | 0.1 μf | 0.01 μf | 0.01 μf |
| $C_3$ | 0.1 μf | 0.1 μf | 0.01 μf | 0.01 μf |
| $C_4$ | 3-12 pf | 3-12 pf | 1.5-7 pf | 1.5-7 pf |
| $L_1$ | 10 μh | 2.2 μh | 0.68 μh | 0.15 μh |
| $L_2$ | 82 μh | 47 μh | 4.7 μh | 4.7 μh |
| $R_1$ | 2-500Ω IN SERIES | 2-500Ω IN SERIES | 2.2 K | 2.2 K |

*CR1 SHOWN FOR PNP OPERATION OF CIRCUIT (3-IN540'S IN SERIES)

**DIAGRAM OF $h_{fe}$ TEST SET**
**Figure 15.51**

constructing this test circuit, double sided copper-clad board is used. Components are physically placed such that lead length is kept to a minimum. To eliminate lead inductance of the transistor under test, a socket is used which allows close connection of the circuit to the transistor header. A rectifier, CR-1, is connected from emitter to ground to insure that C-2 does not charge-up when the test socket is empty. This prevents destroying the next transistor to be tested. In Figure 15.51 the circuit is connected for PNP operation of the test set. A switchable attenuator box is used instead of the range switch of the R.F. millivoltmeter. The R.F. millivoltmeter used in this test set has about a 1 db non-linearity from scale to scale and within a scale. To avoid this error and still use the instrument, an alternate method is required using a single point on the voltmeter (say full scale on the 3 mv scale) and working around that level with a switchable attenuator.




**ATTENUATOR BOX**
**Figure 15.52**

Figure 15.52 shows the attenuator box. Three switchable pads are incorporated enabling any combination of the three pads to be used. This in effect keeps the R.F. millivoltmeter on the same scale (3 mv scale) and within that scale, the pointer is always no less than ⅔ of full scale. The design formulas for these pads were taken from *Reference Data for Radio Engineers* using unbalanced $\pi$ networks keeping the input and output impedances equal to 50 ohms.

## POWER GAIN MEASUREMENT

### GENERAL

In a practical and useful amplifying device there is one question of paramount importance, how much will it amplify at the frequency (or band of frequencies) of interest? In short, what is the power gain? Obviously where the amplifier has insufficient gain to fulfill the minimum requirements, the device is of only passing interest. Other important considerations may include flat frequency response, amplifier stability with temperature variation and other environmental changes, effective operating life of the device and total power consumption. Power gain, however, is still of primary interest and will be discussed in this section.

From the standpoint of the circuit designer the power amplifier should, among other things, be a *unilateral* device with no internal feedback of any sort, and have equal input and output driving point impedances. It should contribute no noise of its own to the signal being amplified, have a perfectly flat gain/frequency response, and a large gain-bandwidth product. Transistors, however, are not unilateral devices. Depending upon the circuit configuration being used (common base or common emitter) and the particular frequency, the internal feedback may be either negative or positive, and may even shift phase from one to the other. This effect is not unique to transistors, of course, but these internal aspects do necessitate some thought in defining Power Gain. Consider the case of an amplifier with positive feedback. When the feedback power is great enough to overcome the associated circuit losses, the device will oscillate. Describing the power gain of an oscillator is, of course, meaningless. With no signal applied and any signal at all out of the device, its apparent gain, according to the usual definitions, is infinite! This suggests the need for additional constraints in the definition of gain. Gain may be described under *neutralized* or *unilateralized* conditions, with attendant problems of defining measurement of the

degree of *unilaterality*. Gain may also be defined with certain boundary conditions, or stability criteria, for example, when gain is measured with only that feedback required to make the output driving-point impedance appear infinite. This will be discussed later.

Problems of gain measurement break down into three specific phases:

a. Means of measuring input and output powers of the transistor.

b. Determining the effects of the circuit on the device.

c. Determining the effects of the device upon the circuit.

To be still more specific: in (a.) the generator and load impedances are adjusted to match (either resistively or complex conjugate) the transistor for maximum power gain. It must also be insured that the device is not over-driven either current or voltage-wise. In other words, assurance must be maintained that small signal conditions apply. Due to the extreme signal sensitivity of the usual low-power transistor, the measuring of A.C. powers in the order of 1 to 10 microwatts (A.C. currents in the order of microamperes and A.C. voltages of a few millivolts) is of concern. As a result the measurement problem is more complex than may be immediately apparent.

In (b.) spurious paths or parasitic strays can introduce unwanted feedback, and the particular terminations used must not permit the transistor to operate in a region where internal feedback can cause potential unstability. This is the "gain" of an oscillator paradox. The ideal way to guarantee that the above conditions do not exist is to measure the two port impedances when terminated at the other end by the apparent required match, to see that no signs of negative-resistance exist. This latter condition leads to (c.).

In any circuit with R, L, and C components, a basic loaded Q is present. Assume that this circuit is the complex conjugate match for a transistor. When this transistor is inserted, its output conductance appears across the circuit and the circuit Q should decrease to half the original value. Now consider what would happen were the device to have positive feedback. With enough feedback the output of the transistor has a negative resistance component which absorbs some of the circuit losses and the Active Q now increases. Even if this feedback is internal, rather than caused by unknown and uncontrolled strays, it is difficult to state with confidence the true gain of the transistor. However, a means of using the bandwidth of the circuit as a criterion of stability is available. Thus, the Active Q may be made less than that of the circuit Q alone. This approach will not suffice for negative feedback where the solution relies on the neutralizing techniques which are to be discussed shortly.

## MEASURING POWER GAIN

Power Gain depends on the particular definitions used and the frequency or band of frequencies being considered. These definitions are as follows:

1. $G = \left(\frac{i_2}{i_1}\right)^2 \frac{R_L}{R_1}$ or $G = \frac{P_{out}}{P_{in}}$; where $\frac{i_2}{i_1}$ = current amplification gain

   This is the low frequency case and is the actual gain between $R_{gen}$ and $R_{load}$ and is maximum when $R_{gen} = R_{input}$ and $R_L = R_{output}$, $P_{available} = \frac{(E_o)}{4\,R_{gen}}$ where $E_o$ = open circuit generator voltage.

2. $G_{Transducer}$: (circuit gain or available power)

   $G_{Transducer}$ is the output to available power ratio. The closeness of matching conditions to the two-port impedances of the amplifier will determine how closely $G_T$ approaches $G_{max\ available}$.

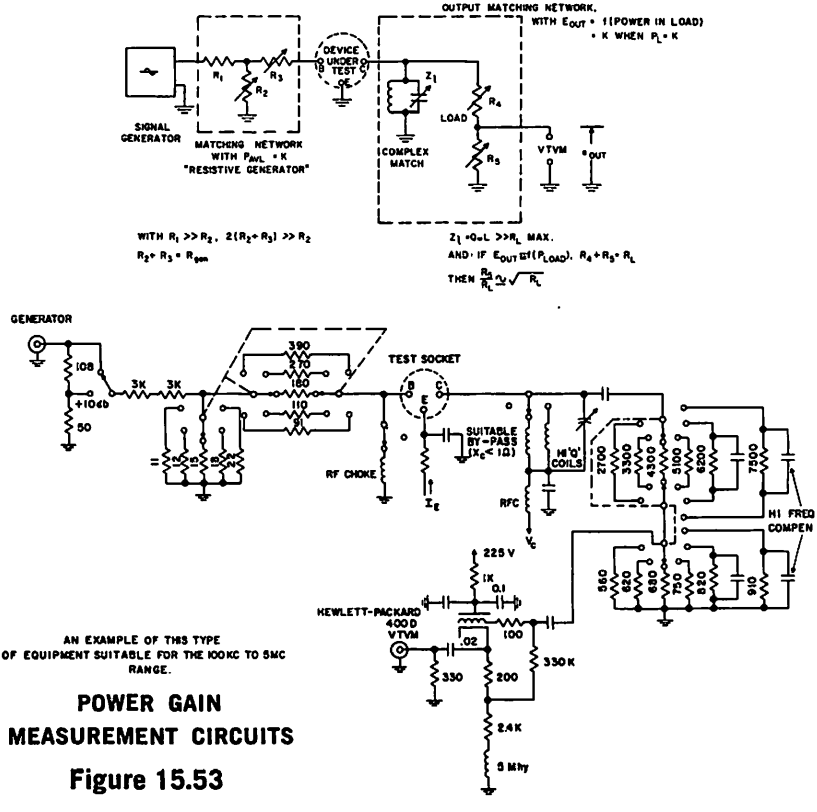
3. $G_{available}$:

   This is the gain of the transistor with only the real part of its input and output impedances matched to the load and generator.

4. $G_{maximum\ available}$:

   The real parts are matched and the reactances are tuned out, that is, the same impedance but of opposite phase. This is the complex-conjugate match and is the most true gain obtainable. Close attention is required to distinguish between this and Pseudo gains which may appear larger due to positive feedback.

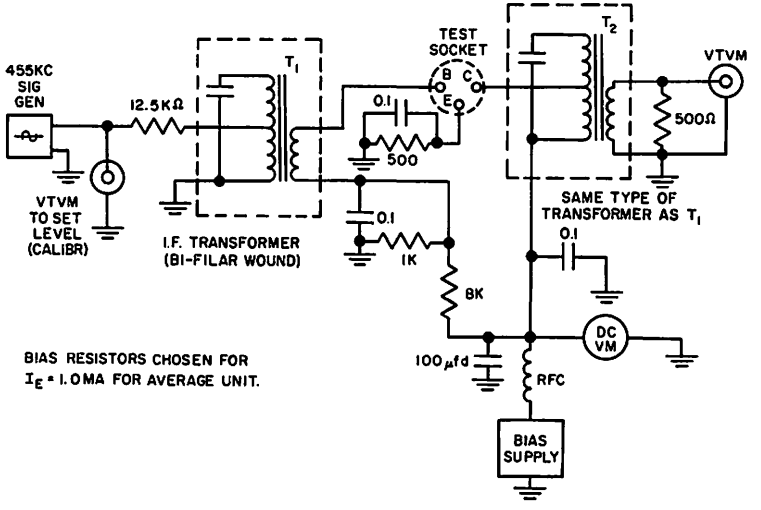
All of the above definitions, with the possible exception of (1) may be considered as classes and are often divided into sub-classes as determined by the considerations mentioned earlier when discussing the phases of the measurement problem. As to the particulars of each measurement set: while it may be possible to measure the current amplification gain in (1) and (3), it is usually easier to have switchable $R_G$ and $R_L$ so arranged that the available generator power is kept constant and an output voltage is obtained proportional to the power in the load. It should be noted that this circuit is also applicable to (2) as long as a resistive generator is desired or necessary. The device, potentially unstable if complex-conjugate matched, may be usably stable if only one terminal is complex matched and the other resistively terminated. For practical reasons the generator is usually the resistive match as shown in Figure 15.53.




**POWER GAIN MEASUREMENT CIRCUITS**

**Figure 15.53**

Measurement of (2) often takes the form of the circuit shown in Figure 15.54. This is a *Functional* I.F. Test.




**FUNCTIONAL I.F. POWER TEST**
**Figure 15.54**

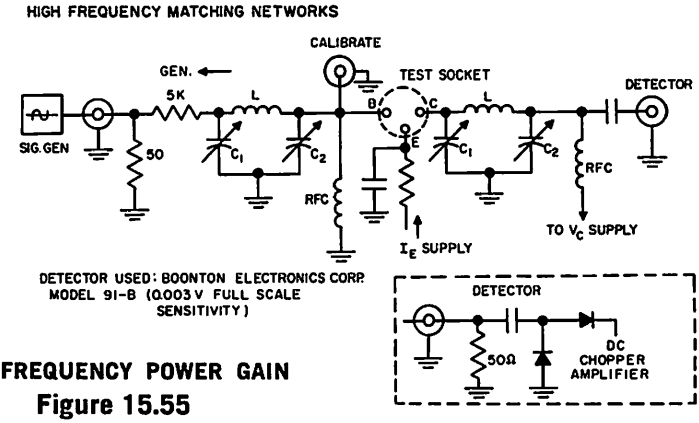
To reproduce the measurements from set to set, the transformer loaded impedances, losses, and bandwidth must be specified. The layout is standardized and precision resistors and meters are used to establish the D.C. bias conditions. Since gain varies with temperature, means of controlling or at least monitoring temperature should be included. The use of attenuators to set relative levels on the VTVM is encouraged, rather than relying on the linearity and accuracy of the VTVM.

For complex-conjugate matching, and also for a simple method of measuring high-frequency gain, the $\pi$ network has proven very useful as an impedance transformer. With care, the losses in the network can be kept low (in the order of 1 db). It should be remembered that this network acts as a filter, and bandwidth measurements should not be made. Where bandwidth is important the use of variable link coupling networks will prove more satisfactory.

In the following circuit, Figure 15.55, the detector is coupled into the generator at the calibrate jack. The network is then adjusted for a maximum reading. Assuming the losses of the input network are constant with small variations of match, and the input impedance of the transistor is close to the 50 ohms of the detector, the output will be the zero db reference setting, and only the losses in the output network are important. By keeping these losses small with proper network design, the losses can then be considered as part of the transistor's gain.

## NEUTRALIZATION

The need for neutralization arises when internal feedback exists. The device is not unilateral and variations of load affect the input impedance. This fact enables one to devise methods of determining when neutralization has been accomplished. There are two accurate measuring techniques. One uses a resonant load and sweeps the input

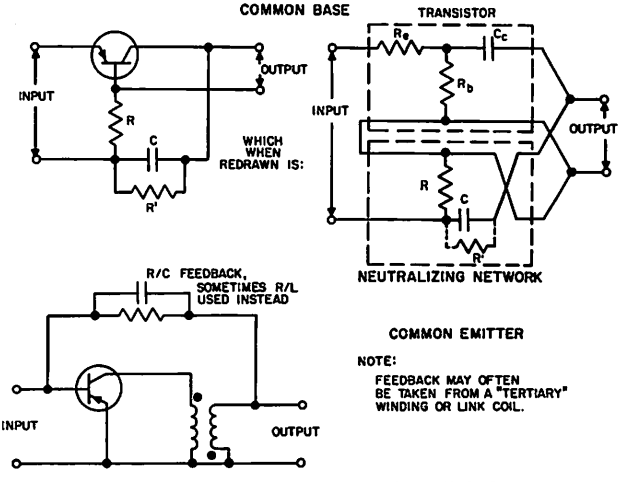



**HIGH FREQUENCY POWER GAIN**

**Figure 15.55**

with a variable frequency signal current source. As the signal goes above and below the resonant frequency, the load becomes first capacitive and then inductive. If a high impedance sensitive detector is used to look at the input voltage, the changing impedance is seen at the input due to reflected load changes. At frequencies up to 5 or 10 mcs such detectors are available, but in the VHF range a different approach is used. The second approach, applicable at most frequencies, is to measure the feedback voltage appearing at the input when a signal is applied at the output. This is precisely what is done in measuring $h_{rb}$.

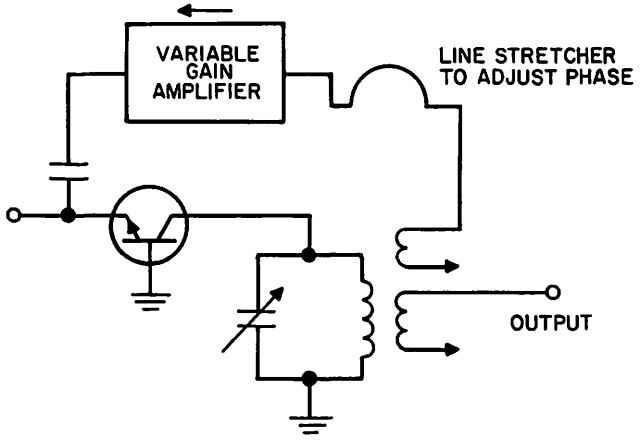
In both methods some out of phase feedback is applied in parallel with the device, so as to cancel either impedance changes or feedback voltage. Means of amplitude and phase control will need to be incorporated in the neutralizing network to avoid over-compensation. Simplified circuit diagrams are illustrated in Figure 15.56 to show some of the various feedback schemes used. The feedback networks are lumped-constant types at lower frequencies and transmission line types at VHF.




**NEUTRALIZATION MEASUREMENTS**

**Figure 15.56**

To check the true gain of a transistor, unilateral amplifiers are used in the feedback path to supply the power consumed in the feedback (neutralizing) network, thereby not loading the transistor's output, as shown in Figure 15.57.




**SCHEMATIC OF TRUE GAIN MEASUREMENT**
**Figure 15.57**

## TRANSISTOR NOISE MEASUREMENTS

### GENERAL

The noise output from an amplifier consists of two parts:

1. Output due to noise generated at the input-terminals.
2. Output due to noise generated inside the amplifier itself.

Part 1 of the noise power output is predictable since the available noise-power in any resistor is

$$P_n = kT\bar{B} \tag{15a}$$

where,

$k$ = Boltzman's constant
$T$ = Absolute temperature (°K)
$\bar{B}$ = Effective bandwidth

and this effective bandwidth is

$$\bar{B} = \frac{1}{G}\int_0^\infty G(f)\,df \tag{15b}$$

By measuring the gain with frequency, integrating and dividing by the maximum gain, the equivalent rectangular power pass-band is found. Since noise-power at the output consists of two parts, and one of these may be predicted, this may be used to specify the noisiness of an amplifier. The index used for this purpose is called the noise factor and is defined

$$F = \frac{\text{Total Noise Power Out}}{\text{Power gain} \times \text{Noise Power due to Source Resistor}} \tag{15c}$$

or,

$$F = \frac{P_N}{G \cdot P_n}$$

But since, $G = \frac{(P_S)_{out}}{(P_S)_{in}}$, where $P_S$ is signal power

$$F = \frac{P_N}{\frac{(P_S)_{out}}{(P_S)_{in}} \cdot P_n} = \frac{\frac{(P_S)_{in}}{P_n}}{\frac{(P_S)_{out}}{P_N}} = \frac{\left(\frac{\text{Signal}}{\text{Noise}}\right)_{in}}{\left(\frac{\text{Signal}}{\text{Noise}}\right)_{out}} \tag{15d}$$

Noise Figure (NF) = 10 log F

Expressed in terms of voltage and resistance, the available noise-power can be written

$$P_n = \frac{\overline{E_n^2}}{4 R_g} = kT\overline{B} \tag{15e}$$

or,

$$\overline{E_n} = \sqrt{4 kT\overline{B} R_g} \tag{15f}$$

At room temperature, $4 kT = 1.6 \times 10^{-20}$ joules.

## MEASUREMENT OF NOISE FIGURE

In equation (15f) $E_n$ is the noise voltage at the input. Now a signal is added at the input ($\gamma$ times $E_n$) such that the output level with signal is much greater than the noise output. This value $\gamma$ is the signal-to-noise ratio and "calibrates" the output level of the entire measuring system. When the signal is removed, the output level should drop to $\frac{1}{\gamma}$ of this *calibrated* level provided the amplifier is perfect. Since the amplifier contributes some noise, the level will not drop that far. The ratio between the actual level of noise background and the *ideal* case is the noise factor and the noise figure may be read on the db scales of the VTVM used. Since the noise voltage fluctuates, sufficient capacitance must be added across the meter movement of the VTVM to integrate the noise voltage with time. If an average-reading meter (calibrated in RMS of a sine wave) is used, then the meter will read 11% lower on noise than on sinusoidal signals, and the "calibration" signal must be reduced accordingly for correct measurements. If a *true RMS* meter or bolometer is used, this correction is unnecessary.

Since the unknown signal is present during the calibration process, the measured Noise Figure is not the true Noise Figure.

According to equation (15d)

$$F = \frac{\left(\frac{\text{Signal}}{\text{Noise}}\right)_{in}}{\left(\frac{\text{Signal}}{\text{Noise}}\right)_{out}} \tag{15g}$$

The input during calibration is $S'_{in} = (P_S)_{in} + P_n$

The noise input is $N'_{in} = P_n$

and,

$$\frac{S'_{in}}{N'_{in}} = 1 + \frac{(P_S)_{in}}{P_n} \tag{15h}$$

The apparent output signal $S'_{out} = G[(P_S)_{in} + P_n] + P_E$

The apparent output noise $N'_{out} = GP_n + P_E$

where $P_E$ is the noise generated in the transistor.

Therefore,

$$\frac{S'_{out}}{N'_{out}} = \frac{G[(P_S)_{in} + P_n] + P_E}{GP_n + P_E} \tag{15i}$$

The measured noise factor

$$F_M = \frac{\frac{S'_{in}}{N'_{in}}}{\frac{S'_{out}}{N'_{out}}} = \frac{1 + \frac{(P_S)_{in}}{P_n}}{\frac{G[(P_S)_{in} + P_n] + P_E}{GP_n + P_E}} = \frac{1 + \frac{S_{in}}{N_{in}}}{1 + \frac{S_{out}}{N_{out}}} \tag{15j}$$

since $G(P_S)_{in}$ is the true output signal $= S_{out}$
and $GP_n + P_E$ is the true output noise $= N_{out}$

By re-arranging equation (15j)

$$F_M = \frac{\frac{S_{in}}{N_{in}}}{\frac{S_{out}}{N_{out}}} \cdot \frac{1 + \frac{N_{out}}{S_{out}}}{1 + \frac{N_{in}}{S_{in}}} = F \frac{1 + \frac{N_{in}}{S_{in}}}{1 + \frac{N_{out}}{S_{out}}} \tag{15k}$$

or the true noise factor

$$F = F_M \frac{1 + \frac{N_{in}}{S_{in}}}{1 + \frac{N_{out}}{S_{out}}} \tag{15l}$$

From equation (15l )it is seen that if $S_{out}$ is much greater than the noise background level F approaches $F_M$ since this also implies $S_{in} >> N_{in}$.

One other complication is that the noise output of the transistor under test is far below the level of sensitivity of most commercially available meters, so that an amplifier must be used to raise the noise level to a readable level. Unfortunately, this amplifier can contribute noise of its own and degrade the readings.

It is easily shown that the total noise factor of a cascade system is

$$F_T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \tag{15m}$$

So that G should be made as high and $F_2$ as low as possible to avoid these errors. (Removing the device under test while observing the noise background will supply a quick check on post-amplifier degradation. The output level should drop 20 db or more.)

A much more convenient way to make noise factor measurement is to use a noise diode. It is known that the output noise current from such a noise diode is:

$$\overline{I_N^2} = 2q\, I_{DC}\, \overline{B} \tag{15n}$$

$q$ = electron charge
$I_{DC}$ = plate current in diode
$\overline{B}$ = effective bandwidth

If the source resistance is $R_g$, the available noise power is

$$S_1 = \frac{\overline{I_N^2} R_g}{4} = \frac{2q\, I_{DC}\, \overline{B}\, R_g}{4} \tag{15o}$$

This is the noise power generated by the diode alone. The noise power due to $R_g$ is

$$N_1 = kT\overline{B} \tag{15p}$$

and this is in addition to $S_1$.

The excess noise generated in the amplifier is $N_E$ and the power gain is G and if M is defined as the ratio of noise power output with diode turned on to noise power output with diode turned off

then,

$$M = \frac{\left(kT\overline{B} + \frac{2q\, I_{DC}\, \overline{B}\, R_g}{4} G + N_E\right)}{kT\overline{B}\, G + N_E} \tag{15q}$$

or,

$$M - 1 = \frac{\frac{2q\, I_{DC}\, \bar{B}\, R_g}{4} G}{kT\bar{B}\, G + N_E} \equiv \left(\frac{S}{N}\right)_{out} \tag{15r}$$

and since,

$$\left(\frac{S}{N}\right)_{in} = \frac{\frac{2q\, I_{DC}\, \bar{B}\, R_g}{4}}{kT\bar{B}} \tag{15s}$$

we have,

$$F = \frac{\left(\frac{S}{N}\right)_{in}}{\left(\frac{S}{N}\right)_{out}} = \frac{\frac{2q\, I_{DC}\, \bar{B}\, R_g}{4}}{M - 1} \tag{15t}$$

But at $T = 290°K$ (17°C), $\frac{2q}{4\,kT} = 20\ (\text{volts})^{-1}$

So equation (15t) can be written as

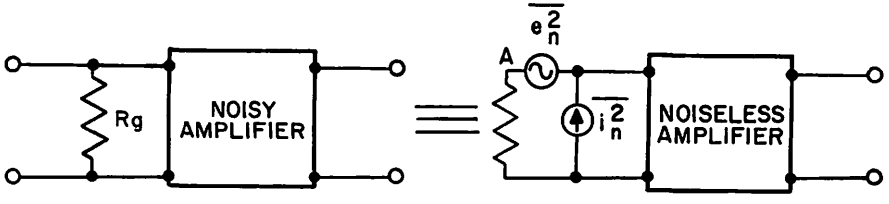
$$F = \frac{20\, I_{DC}\, R_g}{M - 1} \tag{15u}$$

Usually M is chosen to be equal to 2
therefore the noise factor is,

$$F = 20\, I_{DC}\, R_g \tag{15v}$$

## EQUIVALENT NOISE CURRENT AND NOISE VOLTAGE

Because of the internally generated noise, the output noise current is not zero when the input is open, and for the same reason the output noise voltage is not zero when the input is short-circuited. Since the noise current and noise voltage output are solely dependent on the transistor it seems that a noise specification based on those two quantities would be more generally useable. In the following derivation the relationship between open circuit noise current, short-circuit noise voltage and noise factor will be shown. A noisy amplifier may be substituted by a noise-less amplifier with equivalent noise-current and noise-voltage sources connected to the input, as shown in Figure 15.58.




**THEVENIN'S EQUIVALENT OF NOISY AMPLIFIER**

**Figure 15.58**

The total noise-power at point A is proportional to

$$\overline{i_T^2} = \frac{4\,kT\bar{B}}{R_g} + \frac{\overline{e_N^2}}{R_g^2} + \overline{i_N^2} \tag{15w}$$

The first term is the noise-current generated in $R_g$ and since the noise factor,

$$F = \frac{\text{all noise}}{\text{noise due to } R_g}$$

then,

$$F = 1 + \frac{\overline{e_N^2}}{4\,kT\overline{B}\,\overline{R_g}} + \frac{\overline{i_N^2}\,R_g}{4\,kT\overline{B}} \tag{15x}$$

$$\overline{B} = \text{effective bandwidth} = \frac{1}{G_{MAX}}\int_0^\infty G(f)df$$

where,

$G(f)$ = gain as function of frequency

$G_{MAX}$ = maximum gain

Defining,

$$\left.\begin{aligned} R_{eqv} &= \frac{\overline{e_N^2}}{4\,kT\overline{B}} \\ I_{eqv} &= \frac{\overline{i_N^2}}{2\,q\overline{B}} \end{aligned}\right\} \tag{15y}$$

equation (15x) will be,

$$F = 1 + \frac{R_{eqv}}{R_g} + \frac{2q\,I_{eqv}}{4\,kT} \tag{15z}$$

and since,

$$\frac{2q}{4\,kT} = 20\ (\text{volts})^{-1} \text{ at } T = 290°K,$$

$$F = 1 + \frac{R_{eqv}}{R_g} + 20\,I_{eqv}\,R_g \tag{15aa}$$

In Figure 15.58 the noise-voltage source may be thought of as a lossless resistor $R_{eqv}$, and the current source as a parallel shot noise generator due to an equivalent DC current $I_{eqv}$.

To find the optimum value on the noise factor the derivative of F equation (15x) is taken with respect to $R_g$, and this optimum noise factor is found to be

$$F_{opt} = 1 + \frac{\sqrt{\overline{e_N^2}\,\overline{i_N^2}}}{2\,kT\overline{B}} = 1 + 2\sqrt{20\,R_{eqv}\,I_{eqv}} \tag{15bb}$$

for,

$$R_g = R_{opt} = \sqrt{\frac{\overline{e_N^2}}{\overline{i_N^2}}} = \sqrt{\frac{R_{eqv}}{20\,I_{eqv}}} \tag{15cc}$$

From equation (15bb) it is seen that the optimum noise factor can be found analytically if $e_N^2$ and $i_N^2$ are known. This is also the noise factor which will be measured if a measurement is made with a source resistance $R_{opt}$.

Combining equations (15x) and (15bb).

$$F = 1 + \frac{F_{opt} - 1}{2}\left[\frac{R_g}{R_{opt}} + \frac{R_{opt}}{R_g}\right] \tag{15dd}$$

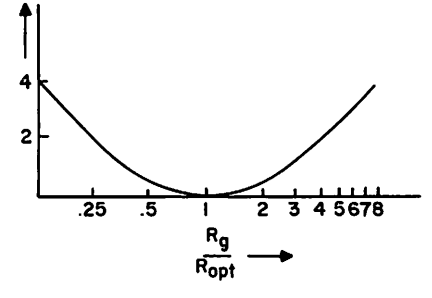
Therefore, if $F_{opt}$ and $R_{opt}$ are given, the noise factor can be found for any source resistance $R_g$.

Defining a factor k, as

$$k = \frac{1}{2}\left[\frac{R_g}{R_{opt}} + \frac{R_{opt}}{R_g}\right]$$

equation (15dd) becomes

$$F = 1 + (F_{opt} - 1)\,k \tag{15ee}$$




**FACTOR k VS. $\frac{R_g}{R_{opt}}$**

**Figure 15.59**

For example, the optimum noise figure $(NF)_{opt}$ is given as 1.5 db or $F_{opt} = 1.4$. The optimum source-resistance is 1000Ω. What is the noise factor in a circuit where $R_g = 8$ kΩ. The ratio $\frac{R_g}{R_{opt}} = 8$, and from the Figure 15.59, k is found to be 4.

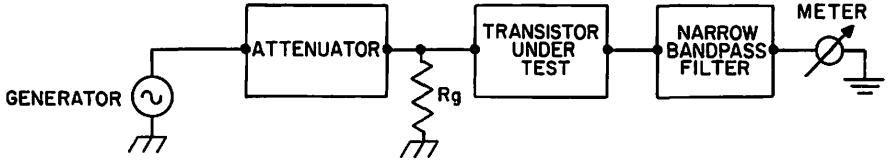
Therefore, the noise factor will be

$$F = 1 + (F_{opt} - 1)\,k = 1 + (1.4 - 1) < 4 = 2.6$$

$$NF = 4.1 \text{ db}$$

## MEASUREMENT OF $(\overline{e_N^2})^{1/2}$ AND $(\overline{i_N^2})^{1/2}$ FOR TRANSISTORS

The schematic in Figure 15.60 is used to measure $(\overline{e_N^2})^{1/2}$.




**SET UP TO MEASURE $(\overline{e_N^2})^{1/2}$**

**Figure 15.60**

$R_g$ must be chosen so as to be much smaller than the input resistance of the transistor.

It is known from transistor-analysis that

$$R_{eqv} \cong \frac{r_e}{2} + r_b'$$

To make $\frac{R_{eqv}}{R_g}$ in equation (15aa) the dominant term,

$$R_{eqv} >> R_g \text{ or } R_g << \frac{r_e}{2}$$

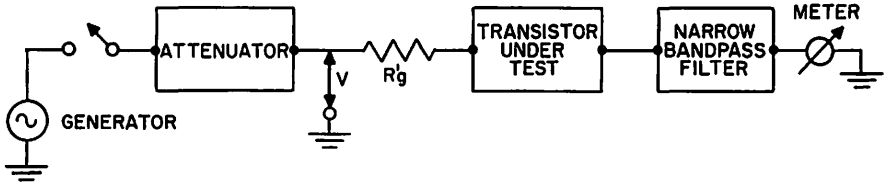
The measurement-procedure is as follows:

a. The back-ground noise-level is noted.

b. The signal generator is connected through a suitable attenuator, and the level of the generator is adjusted until the device output level is 20 db above back-ground level.

c. The required input level is measured from which $e_n$ can be determined.

To measure the equivalent noise-current, an almost identical circuit is used. The only difference being $R_g$ replaced by a high resistor inserted in series as shown in Figure 15.61.




**SET UP TO MEASURE $(\overline{i_N^2})^{1/2}$**

**Figure 15.61**

A condition which must be satisfied is

$$\sqrt{\frac{4\,kT\overline{B}}{R_g'}} << \sqrt{\overline{i_N^2}}$$

If the background noise level is $V_n$ and the input voltage V gives E volts out, then equivalent noise-current is

$$\overline{i_N} = \frac{V}{R_g} \cdot \frac{V_N}{E}$$

It should be strongly emphasized that $\overline{e_N}$ and $\overline{i_N}$ must be measured under the same operating conditions to have any practical significance, and also the necessary correction must be made for the lower meter reading on noise.

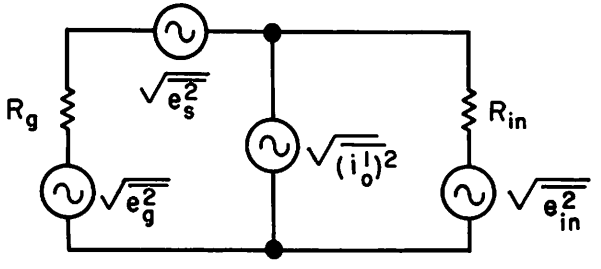
## MEASUREMENT OF NOISE FACTOR WITHOUT USING SIGNAL GENERATOR OR NOISE DIODE

The concept of equivalent noise current and equivalent noise voltage can be used to measure noise factor without a signal generator or noise diode. Since the noise factor depends on the source resistance, and every resistor is a thermal noise source by nature, the source resistance can be utilized as a noise generator.

The method is based on three measurements, from which the noise factor can be computed

1. The noise voltage at the output, input open-circuited.
2. The noise voltage at the output, input short-circuited.
3. The noise voltage at the output, the desired source resistance connected to the input.

One necessary condition in this method is that the input resistance to the device be known, or be measurable.




**EQUIVALENT NOISE CIRCUIT**

**Figure 15.62**

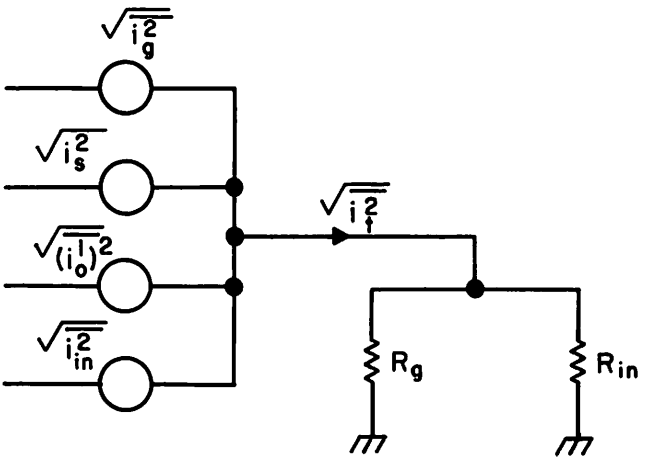
$\sqrt{\overline{e_g^2}}$ is the noise voltage generated in the source resistance $R_g$

$\sqrt{\overline{e_s^2}}$ is the equivalent noise voltage, input shorted

$\sqrt{\overline{(i_o')^2}}$ is the true equivalent noise current, input open

$\sqrt{\overline{e_{in}^2}}$ is the noise voltage generated in the input resistance

The above circuit, Figure 15.62, is re-drawn as a current equivalent in Figure 15.63.




**NOISE CURRENT EQUIVALENT CIRCUIT**
**Figure 15.63**

The relationships between currents and voltages are,

$$\overline{i_g^2} = \frac{\overline{e_g^2}}{R_g^2} \; ; \; \overline{i_s^2} = \frac{\overline{e_s^2}}{R_g^2} \; ; \; \overline{i_{in}^2} = \frac{\overline{e_{in}^2}}{R_{in}^2}$$

The total current flowing into the parallel combination of $R_g$ and $R_{in}$

$$\overline{i_T^2} = \frac{\overline{e_g^2} + \overline{e_s^2}}{R_g^2} + \overline{(i_o')^2} + \frac{\overline{e_{in}^2}}{R_{in}^2} \tag{15ff}$$

The measured open circuited equivalent noise voltage is due to

$$\overline{e_o^2} = \overline{(i_o')^2}\, R_{in}^2 + \overline{e_{in}^2} \tag{15gg}$$

Combining (15ff) and (15gg) gives

$$\overline{i_T^2} = \frac{\overline{e_g^2} + \overline{e_s^2}}{R_g^2} + \frac{\overline{e_o^2}}{R_{in}^2} \tag{15hh}$$

The noise factor

$$F = \frac{\overline{i_T^2}}{\overline{i_g^2}} = \frac{\dfrac{\overline{e_g^2} + \overline{e_s^2}}{R_g^2} + \dfrac{\overline{e_o^2}}{R_{in}^2}}{\dfrac{\overline{e_g^2}}{R_g^2}} = 1 + \frac{\overline{e_s^2}}{\overline{e_g^2}} + \frac{\overline{e_o^2}}{\overline{e_g^2}}\left(\frac{R_g}{R_{in}}\right)^2 \tag{15ii}$$

From this last equation it is seen that F can be expressed in terms of voltage ratios; and, therefore, only output voltages have to be measured.

Equation (15ii) is not too useful since we can not measure $e_g$ separately.

The noise factor may also be expressed as,

$$F = \frac{[\text{total voltage across parallel } R_g \text{ and } R_{in}]^2}{[\text{voltage across parallel } R_g \text{ and } R_{in} \text{ due to } i_g]^2}$$

$$F = \frac{\overline{e_T^2}}{\overline{i_g^2}\left[\dfrac{R_g R_{in}}{R_g + R_{in}}\right]^2} = \frac{\overline{e_T^2}}{\overline{e_g^2}\left[\dfrac{R_{in}}{R_g + R_{in}}\right]^2} \tag{15jj}$$

Multiplying both sides of (15jj) by $\overline{e_s^2}$ and solving for $\frac{\overline{e_s^2}}{\overline{e_g^2}}$

$$\frac{\overline{e_s^2}}{\overline{e_g^2}} = F \frac{R_{in}^2 \overline{e_s^2}}{(R_{in} + R_g)^2 \overline{e_T^2}} \tag{15kk}$$

Substituting the identity,

$$\frac{\overline{e_o^2}}{\overline{e_g^2}} \equiv \frac{\overline{e_o^2}}{\overline{e_s^2}} \cdot \frac{\overline{e_s^2}}{\overline{e_g^2}}$$

and equation (15kk) into equation (15ii), and solving for F,

$$F = 1 - \frac{\frac{\overline{e_T^2}}{\overline{e_s^2}}\left(1 + \frac{R_g}{R_{in}}\right)^2}{1 + \frac{\overline{e_o^2}}{\overline{e_s^2}}\left(\frac{R_g}{R_{in}}\right)^2} \tag{15ll}$$

According to equation (15cc),

$$R_{opt} = \sqrt{\frac{\overline{e_N^2}}{\overline{i_N^2}}}$$

and since,

$$\overline{e_N^2} \equiv \overline{e_s^2}$$

and,

$$i_N^2 \equiv \frac{\overline{e_o^2}}{R_{in}^2}$$

$$R_{opt} = \sqrt{\frac{\overline{e_s^2}}{\overline{e_o^2}}}\, R_{in} \tag{15mm}$$

and equation (38) becomes,

$$F = \frac{1}{1 - \frac{\overline{e_T^2}}{\overline{e_s^2}}\left(1 + \frac{R_g}{R_{in}}\right)} \tag{15nn}$$

$\sqrt{\overline{e_T^2}}$ output voltage when $R_g$ is connected to input

$\sqrt{\overline{e_s^2}}$ output voltage, input terminals shorted

$\sqrt{\overline{e_o^2}}$ output voltage, input terminals open

$$R_{opt} = R_{in} \sqrt{\frac{\overline{e_s^2}}{\overline{e_o^2}}}$$

$R_{in}$ = input resistance of transistor.

Thus, the measurement of noise factor is accomplished without the use of a noise generator or diode.

## TRANSISTOR NOISE ANALYZER

A more convenient way to measure equivalent noise voltage and current is to use the Quan Tech Transistor Noise Analyzer Model 310. This is an instrument where equivalent noise voltage and current can be read directly at three different center frequencies, namely at 100 cps, 1 Kc, and 10 Kc. The noise voltages and currents are read in volts per square root cycle ($V/\sqrt{cycle}$) and Amperes per square root cycle ($A/\sqrt{cycle}$).

Example:

Transistor 2N123

$V_{CE} = -5$ V

$I_E = 1$ mA

Equivalent short-circuited noise voltage $\overline{e_N} = 1.8 \times 10^{-9}$ V/$\sqrt{\text{cycle}}$

Equivalent open-circuited noise current $\overline{i_N} = 2.5 \times 10^{-12}$ A/$\sqrt{\text{cycle}}$ (measured at 1 Kc)

This gives

$$R_{opt} = \frac{1.8 \times 10^{-9}}{2.5 \times 10^{-12}} = 720\ \Omega$$

and

$$F_{opt} = + \frac{e_N\, i_N}{2\,kT} = + \frac{1.8 \times 2.5}{8} = 1.564$$

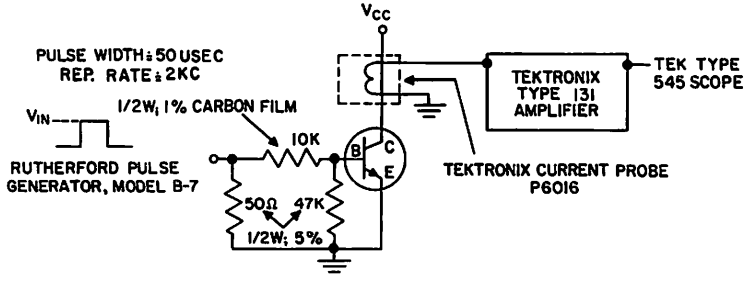
Optimum noise figure = 1.94 db.

## CHARGE CONTROL PARAMETER MEASUREMENT

The measurement of the charge parameters (described in Chapter 7) are discussed in this section. The four parameters which are currently specified on G.E. specification sheets are measured in the manner shown in the following paragraphs. NPN configuration is used for circuit layouts, but PNP measurements can be accomplished by reversing the polarity of $V_{in}$ and $V_{CC}$. One consideration which should be mentioned before the actual circuits are introduced is that of measurement accuracy. In any measurement of switching speed, determination of the pulse voltage magnitudes and the bias voltages is extremely critical. In these parameter measurements, an attempt was made to minimize the number of critical pulse and bias voltage measurements necessary.

### $\tau_a$, THE EFFECTIVE LIFETIME IN THE ACTIVE STATE

The circuit used to measure $\tau_a$ is shown in Figure 15.64. Inasmuch as the circuit contains no dissipation limiting resistor, extreme caution should be used to assure that $V_{CC} \cdot I_C$ does not exceed the dissipation limits of the device.



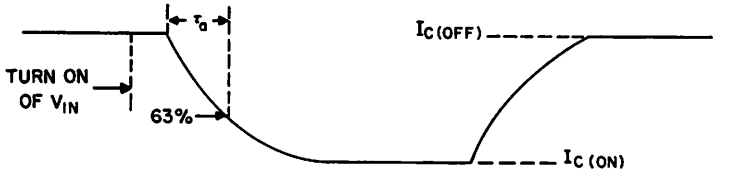

$\tau_a$ TEST CIRCUIT

**Figure 15.64**

To perform the actual measurement, the following steps are taken:

1. Before the device is inserted into the test socket, $V_{in}$ amplitude is set to below +.3 volts.
2. $V_{CC}$ is set to +4 volts. (This voltage may be lowered when dissipation is an important factor, but should not be made lower than +2 volts.)

3. A Tektronix Type 131 Amplifier and Tektronix Type 545 Oscilloscope (or equivalent) are set up so that the collector current at which measurement is desired produce a scope deflection equal to 3 cm. The current at which the measurements should be made is that $I_C$ for which the device dissipation rating is approached by the $V_{CC} \cdot I_C$ product. This point is used for the measurement so that the $\tau_a$ obtained will be the true minimum and be accurate for "worst-case" design techniques.
4. The device is now inserted into the test socket. *CAUTION:* If the base lead accidently touches the collector lead during insertion, the device may be destroyed, unless an electrically current-limited power supply is used.
5. The input voltage is now increased until the $I_C$ deflection is 3 cm (or the desired $I_C$ value).
6. $\tau_a$ is the time constant of the resulting pulse waveform as shown in Figure 15.65. It is *NOT* necessary to record the input pulse amplitude.

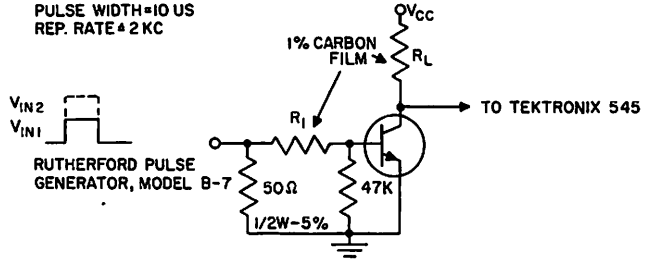



**$\tau_a$ MEASUREMENT WAVEFORM**

**Figure 15.65**

## $\tau_b$, EFFECTIVE LIFETIME IN SATURATED STATE

The test circuit for measuring $\tau_b$ is shown in Figure 15.66




**$\tau_b$ TEST CIRCUIT**

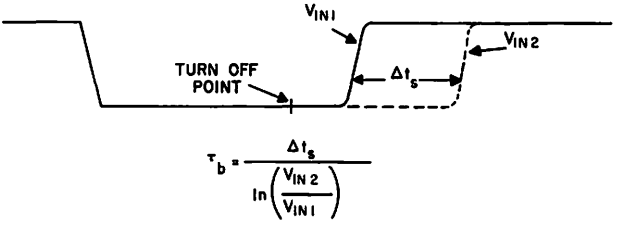
**Figure 15.66**

The following steps are taken to perform the $\tau_b$ measurement:

1. $V_{CC}$ is chosen to be approximately one-half the transistor's breakdown voltage (about 10 volts for most alloy switching transistors).
2. $R_L$ is chosen so the current flowing when the transistor is saturated is equal to a median current. (For alloy types where 100 ma is the maximum current permissible, $R_L$ could be from 200 ohms to 1K for $V_{CC} = 10$ volts. In switching transistors of the mesa type, $V_{CC} = 10$ volts and $R_L = 1K$ are common conditions.)

3. $R_1$ is normally from 2 to 5 times larger than $R_L$.
4. $V_{in}$ is the quantity varied in order to make the $\tau_b$ measurement. The transistor is saturated at two different values of $V_{in}$, and the change in storage time is measured. Ease and accuracy of the measurement may be enhanced with the use of a Rutherford Model B7 pulse generator since $V_{in}$ may be varied by the built-in decade attenuator.
5. The unit is inserted into the test circuit.
6. Two values of $V_{in}$ are chosen which fulfill the conditions that the circuit $\beta$ (forced $\beta$, forced $h_{FE}$, or $V_{CC}\ R_1/V_{in}\ R_L$) is not more than ⅓ of the device $h_{FE}$.
7. The storage time portion of the trace is observed as shown in Figure 15.67. Only $\Delta t_s$ and $V_{in2}/V_{in1}$ need be recorded. $\Delta t_s$ is observed as the $V_{in}$ value is switched between $V_{in1}$ and $V_{in2}$ by manually switching the generator's pulse amplitude.
8. $\tau_b$ is obtained by using the relationship that $\tau_b = \dfrac{\Delta t_s}{\ln\left(\dfrac{V_{in2}}{V_{in1}}\right)}$.

   (If $V_{in2} = 2.72\ V_{in1}$, then $\tau_b = \Delta t_s$.)

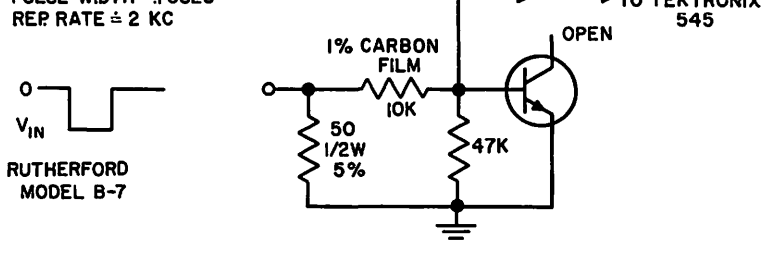



**$\tau_b$ MEASUREMENT WAVEFORM**

**Figure 15.67**

## $\overline{C_{BE}}$, THE AVERAGE EMITTER JUNCTION CAPACITANCE

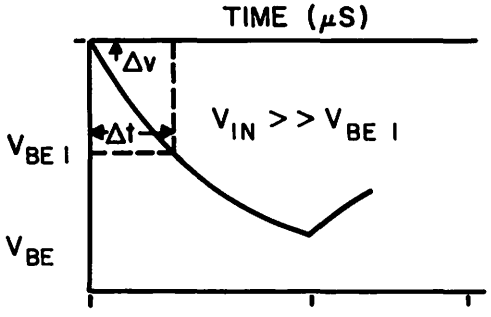
Figure 15.68 is circuit used to measure $\overline{C_{BE}}$. It should be noted that the input pulse used is to reverse bias the base emitter diode and is *not* of the polarity *which* would turn the base-emitter diode on. To obtain the actual value of $\overline{C_{BE}}$, the following steps are taken




**$\overline{C_{BE}}$ TEST CIRCUIT**

**Figure 15.68**

1. Normally, $V_{in}$ is from 10 to 20 volts and depends somewhat on junction breakdown voltage, i.e., 10 volts may be too high for a low breakdown unit.
2. Insert the transistor into the test socket.
3. $V_{BE}$ transient is observed on the oscilloscope as shown in Figure 15.69. The value of $\overline{C_{BE}}$ is obtained from the relationship shown below the curve.




$$\overline{C_{BE}} = \frac{V_{IN}}{10K} \cdot \frac{\Delta t}{\Delta v}$$

$$Q_E = \int_{V_{BE\,(OFF)}}^{0} C_{BE}\, dV$$

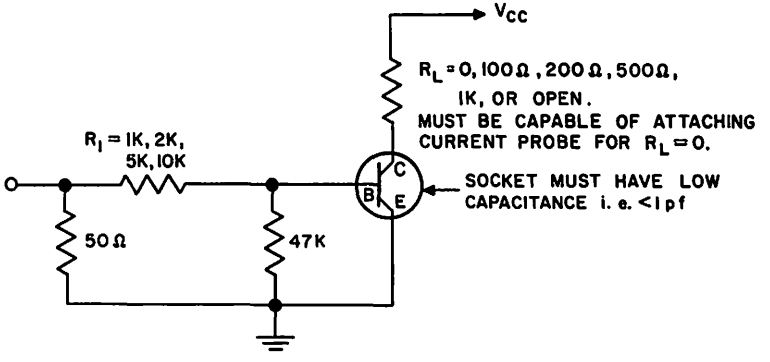
$\overline{C_{BE}}$ MEASUREMENT WAVEFORM

**Figure 15.69**

4. One measurement of capacitance is made to determine measurement gear capacity by performing the same steps with the test socket empty. Measurement gear capacitance is subtracted from the measured $\overline{C_{BE}}$ to determine the actual $\overline{C_{BE}}$.

## COMPOSITE CIRCUIT FOR $\tau_a$, $\tau_b$, $\overline{C_{BE}}$

The similarity of the $\tau_a$, $\tau_b$, and $\overline{C_{BE}}$ test circuits allow that they may be combined in one flexible test circuit as shown in Figure 15.70. The appropriate $R_1$ and $R_L$ conditions allow for the various parameter measurements.



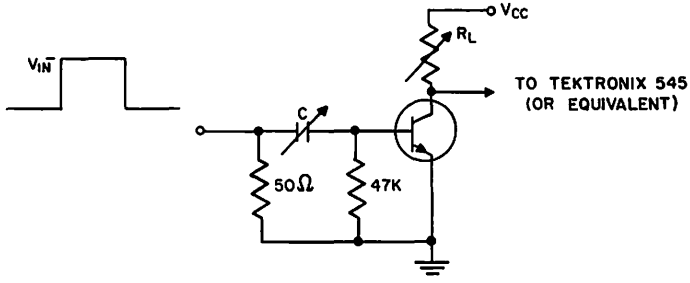

COMPOSITE CIRCUIT FOR $\tau_a$, $\tau_b$, AND $\overline{C_{BE}}$

**COMPOSITE CIRCUIT**

**Figure 15.70**

## $Q_B$*, TOTAL CHARGE TO BRING TRANSISTOR TO EDGE OF SATURATION

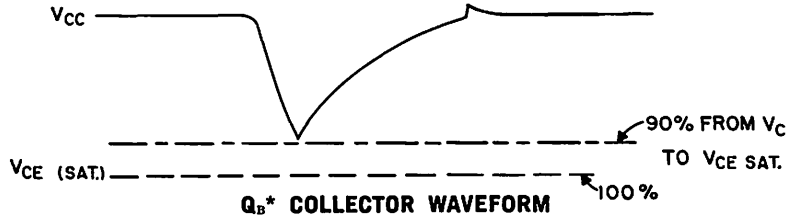
The circuit used to measure $Q_B$* is shown in Figure 15.71. Capacitor, C, is chosen to supply adequate charge to the device being tested without requiring an excessive $V_{in}$ pulse. For alloy transistors a 5 to 100 pf variable capacitor with the capability of switching in additional capacitance, in steps of 100 pf, is used. Mesa transistors require a 3 to 50 pf range. It is important that low inductance capacitors be used. General Radio precision capacitors, Hammarlund type air dielectric capacitors, or their equivalents are satisfactory. In any case, excessive capacity between the base lead and circuit ground must be avoided.




**$Q_B$* TEST CIRCUIT**
**Figure 15.71**

$Q_B$* is a function of collector voltage variation and collector current. Thus, measments are made for various $V_{CC}$ and $R_L$ combinations. The following steps are taken to obtain $Q_B$* data.

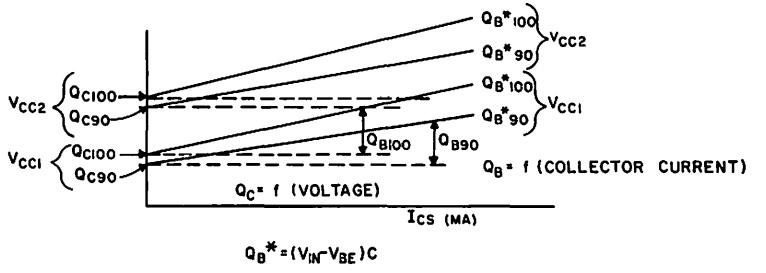
1. $V_{CC}$ is determined first. Several values of $V_{CC}$ will be necessary to determine the full $Q_B$* picture; however, data is taken for one $V_{CC}$ value and various $R_L$ values. $V_{CC}$ values of interest range from $BV_{CEO}$ value to a value of 1 or 2 volts.
2. The unit is now inserted into the test socket.
3. The product $C(V_{in} - V_{BE})$ is the charge which is placed into the transistor to bring it to the edge of saturation. A value of $V_{in}$ is chosen which is sufficient to permit enough charge to pass into the base of the transistor to bring it to the edge of saturation. This, of course, will also depend upon the range of capacitance available. $V_{in}$ is normally between 5 and 20 volts, so that $V_{in} >> V_{BE}$. The capacitor used should be carefully chosen for large variation so as to render the test set more valuable.
4. With $V_{CC}$ and $V_{in}$ adjusted, data can be taken. Record the values of $V_{CC}$ and $V_{in}$. A typical oscilloscope pattern is shown in Figure 15.72.




**$Q_B$* COLLECTOR WAVEFORM**
**Figure 15.72**

As C is increased, the peak of the waveform will approach $V_{CE(SAT)}$. $C_{90}$ is the value of capacitance necessary for the peak to reach 90% of the waveform from $V_{CC}$ to $V_{CE(SAT)}$, while $C_{100}$ is the value of capacitance necessary for the peak of the waveform to reach $V_{CE(SAT)}$.

5. $Q_B{}^*{}_{90}$ and $Q_B{}^*{}_{100}$ are the products of $C_{90}$ $(V_{in} - V_{BE})$ and $C_{100}$ $(V_{in} - V_{BE})$ respectively. $Q_B{}^*$ values are then plotted against $I_{CS}$ (i.e., $\frac{V_{CC} - V_{CE(SAT)}}{R_L}$) as shown in Figure 15.73.




**$Q_B{}^*$ PLOT VS. $I_{CS}$**

**Figure 15.73**

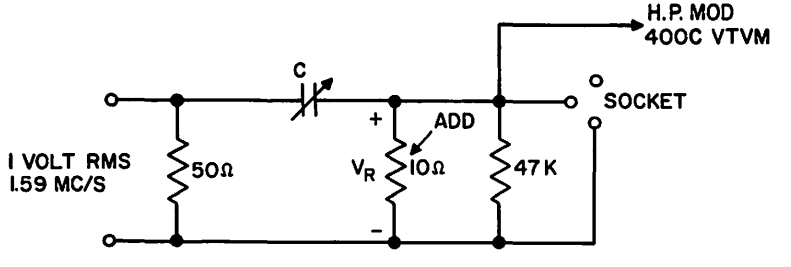
These plots are generally linear over a wide collector current and voltage range for alloy and diffused transistors. The intercept on the $Q_B{}^*$ axis is called $Q_C$ and is the part of $Q_B{}^*$ which varies with collector voltage. The part of $Q_B{}^*$ which varies with $I_{CS}$ is called $Q_B$. Thus, $Q_B{}^* = Q_B + Q_C$.
$Q_B$ and $Q_C$ can also be plotted separately if desired.

## CALIBRATION OF CAPACITOR, C, ON $Q_B{}^*$ TEST SET

A simple method of calibrating the capacitor on the $Q_B{}^*$ test set is available if the circuit in Figure 15.74 is used. The fact that the reactance of the capacitor at 1.59 mc (frequency chosen for convenience) is large compared to 10Ω, permits the 10 ohm resistor to be used as a current measuring device. Looking at the equations

$$X_C = (2\pi f C)^{-1}$$
$$V_{in} = I X_C$$

CALIBRATION OF CAPACITOR ON $Q_B{}^*$ TEST SET




**CAPACITOR CALIBRATION**

**Figure 15.74**

or,

$$C = (2\pi f X_C)^{-1}$$

$$= \frac{I}{2\pi f V_{in}}$$

If $V_{in} = 1$ volt RMS and $f = 1.59$ mc, then,

$$C = (I)\ 10^{-7}$$

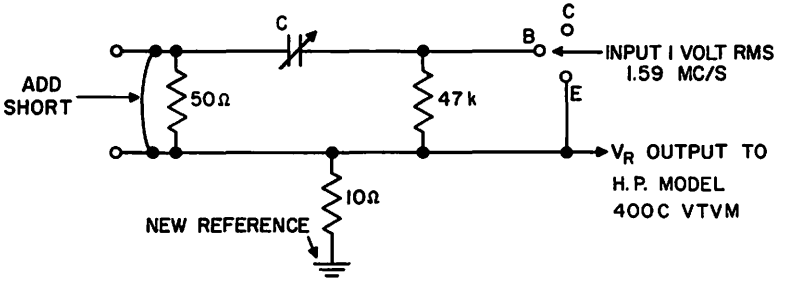
Using the 10 ohms to measure current,

$$I = V_R/10 \text{ ohms}$$

therefore,

$$C = V_R\ (10^{-6}).$$

Thus, the VTVM reading, $V_R$, is used to calibrate C, and .1 mv RMS indicates 1 pf, etc.




**STRAY CAPACITANCE MEASUREMENT**

**Figure 15.75**

If it is desirable to know the stray capacitance from the base to emitter in the test circuit, a similar measurement can be made as shown in Figure 15.75. The variable capacitor is set at a known value, say $C_1$, so

$$C_{stray} = V_R\ (10^{-6}) - C_1$$

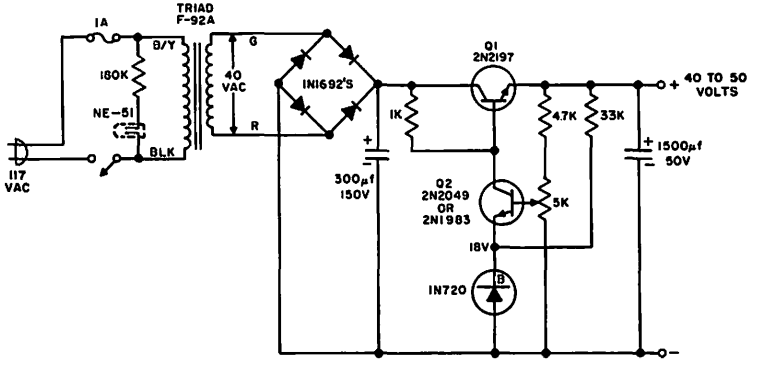
Note that in this determination of stray capacitance the normal circuit reference has been changed. Care must be taken to insure that the old reference is not shorted to the new test reference.

# REGULATED DC SUPPLY AND INVERTER CIRCUITS

CHAPTER 16

## REGULATED DC SUPPLY

The regulated supply of Figure 16.1 is a conventional circuit using a series regulating element. With Q1 mounted on a 2" x 2" x 3/32" aluminum fin the circuit can operate in an ambient temperature up to 70°C. At higher ambient temperatures a heat radiator should be used on Q2, or a higher Zener regulating voltage could be used to decrease the dissipation in Q2.



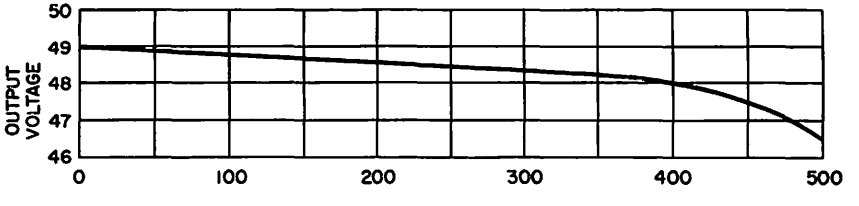

**REGULATED DC VOLTAGE SUPPLY**

**Figure 16.1**

Q1 requires a $V_{CER}$ capability equal to the unregulated output voltage of the bridge. The voltage rating for Q2 must be equal to the difference between the regulated output and the Zener voltage.

Figure 16.2 shows equal regulating ability for all load currents to 350 ma, and 2% voltage regulation at 400 ma. Improved regulation can be achieved by using a Darlington connection for either, or both, Q1 and Q2.

The peak-to-peak output ripple of the circuit in Figure 16.1 is approximately .24 volts at 400 ma load current and decreases to .01 volts at no load. The output impedance is less than 3 ohms from DC to 20 cycles and then decreases to less than ½ ohm at 200 cycles and beyond. The output voltage has no overshoot with step load functions.

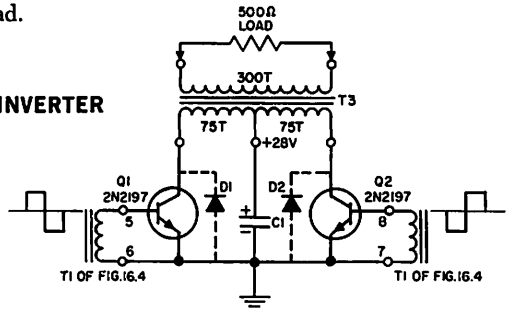



**OUTPUT VOLTAGE VS. LOAD CURRENT**

**Figure 16.2**

## PARALLEL INVERTERS

The parallel inverter configuration shown in Figure 16.3 provides an output that is essentially a square wave. By rectifying the output voltage, the circuit makes an efficient DC to DC converter in applications such as power supplies. An AC input can be rectified to provide the primary power for the inverter, in which case it will function as a frequency changer. A square wave drive to this inverter causes Q1 to conduct half the time while Q2 is blocking, and vice-versa. In this manner, the current from the supply will flow alternately through the two sides of the transformer primary and produce an AC voltage at the load.




**DC TO AC (SQUARE WAVE) INVERTER**
**Figure 16.3**

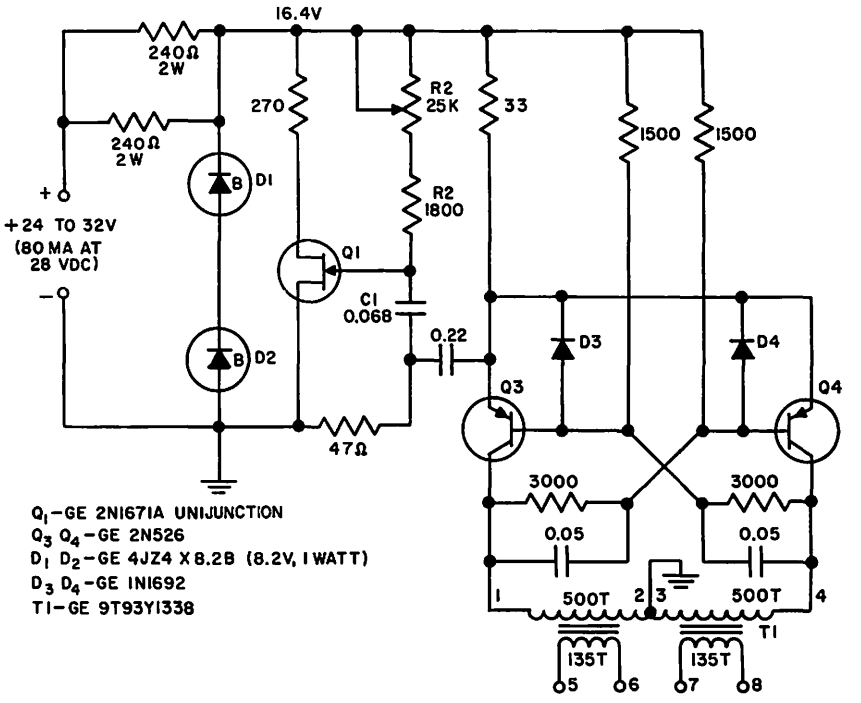
It may be desirable to incorporate the feedback diodes $D_1$ and $D_2$ if the circuit is to be lightly loaded or operated under open circuit conditions. For reactive loads these diodes can conduct to supply the out of phase portion of the load current. When the inverter switches from Q1 to Q2 an inductive load prevents the main load current from reversing instantaneously, so transformed load current must flow through $D_2$ and back into the DC supply until the load current reverses. The feedback diodes prevent the voltage across either half of the primary winding from exceeding the supply voltage. These diodes not only maintain a square wave output under all load conditions, but also decrease the voltage requirements for Q1 and Q2.

The DC source should have a low transient impedance, and a capacitor on the output of the DC supply is usually required so it can accept power as well as supply power. It is often important to have this capacitor ($C_1$) right at the inverter itself as shown in Figure 16.3 since the inductance of the supply leads of a few feet in length represents an undesirable impedance during the $\mu$sec switching intervals.

For a driven transistor inverter, it is desirable to select a transformer and core with a volt-second saturation capability that is at least two times the actual circuit requirements. The leakage inductance should be held to a minimum since the transformer will be subjected to rapidly changing currents during the switching interval. Bifilar transformer winding is usually used to obtain tight coupling between the two primary windings. Since the inverter output transformer (T3) cannot be allowed to saturate, its design must either incorporate an air gap, have a high ratio of saturation to residual flux density, or be used with predictable reset circuitry.

The inverter circuit of Figure 16.3 was operated using two stacked AJ-H12 (Arnold) C-cores (4 mil), in transformer T3. The core gap spacing was .02 inch. This gives about a 2:1 volt-second capability at 400 cycles.

The square wave inverter drive is easily obtained with a transistor multivibrator that uses a unijunction transistor to stabilize and control the frequency as in Figure 16.4.This circuit provides a symmetrical square wave drive which avoids second harmonics in the output and also a DC component in the inverter, tending to saturate the transformer.



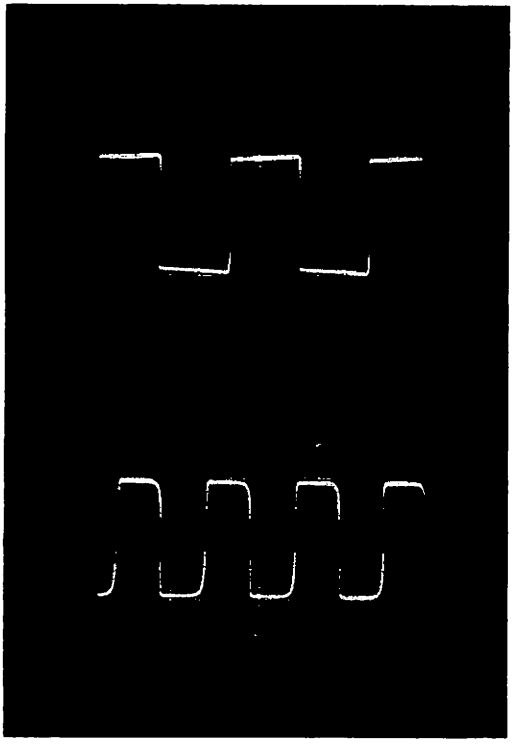

**SQUARE WAVE INVERTER DRIVE CIRCUIT**

**Figure 16.4**

The circuit of Figure 16.4 is a slightly modified "hybrid-multivibrator," described in more detail in Chapter 13. The unijunction transistor provides a source of short, precisely timed negative pulses with the period between pulses depending on the $C_1R_2$ time constant. These pulses are coupled to the common emitter resistor of a conventional transistor flip-flop (Q3 and Q4). Each pulse from the unijunction transistor will turn off the transistor which is on in the flip-flop and the resulting square wave of voltage at the collectors is coupled to the inverter by a small transformer. D3 and D4 are used to prevent the emitter-base voltage of Q3 and Q4 from exceeding ratings when a transistor is turned off.

The multivibrator free runs at about 100 cps, but is synchronized and controlled by the unijunction at the higher operating frequencies at which it is designed to operate. The Zener diodes form a simple shunt regulator to keep the collector-emitter voltage of the transistors within ratings. This circuit has good frequency stability with variations in supply voltage and ambient temperature, due to the inherent stability of the unijunction. The circuit has an operating frequency range of 400 cycles to 3200 cps in an ambient temperature up to 70°C. The output impedance of this square wave generator is about 8 ohms and the open circuit voltage is about 4 volts peak.

With the circuit of Figure 16.4 driving the inverter of Figure 16.3, the inverter output voltage waveform across the load is shown in Figure 16.5. The efficiency of the square wave inverter (Figure 16.3) is 80 to 85% in the 400 to 3200 cycle frequency range.




**INVERTER OUTPUT VOLTAGE**
**(VERTICAL SCALE 50 VOLTS/CM)**

**Figure 16.5**

## DC TO DC CONVERTER

A full wave bridge (1N538's) between the secondary and the 500 ohm load of Figure 16.3 will rectify the 3200 cycle square wave shown in Figure 16.5(b) to give 90 volts DC output. With 100 $\mu$f electrolytic capacitor across the load, the ripple is less than ½ volt peak-to-peak. The overall DC to DC efficiency is about 80% with 16 watts output.

### REFERENCES

"General Electric Silicon Controlled Rectifier Manual," 2nd Edition (1961).
"Notes on the Application of the Silicon Unijunction Transistor," G-E Application Note 90.10.

# SILICON SIGNAL DIODES

CHAPTER 17

Semiconductor diodes are used extensively in all types of electronic circuitry. The various application chapters in this manual illustrate many of the applications in which diodes are used, from detectors in radio receivers to gating and logic elements in computer circuits. The first semiconductor diodes, made before the invention of the transistor, were silicon point contact diodes used as detectors in radar receivers. Later, germanium point contact diodes and gold bonded diodes were introduced which could be used in a variety of applications. The demand for high operating temperatures and low leakage currents led to the development of the silicon alloy junction diode and the silicon diffused mesa diode. The reliability and superior electrical characteristics of the silicon diode together with declining prices has caused it to be used in place of germanium diodes in an increasing number of applications.

## PLANAR EPITAXIAL PASSIVATED SILICON DIODE

Silicon diodes can be made using any of the techniques described in Chapter 2 for transistor fabrication including alloying, growing, meltback or diffusion. On the basis of inherent reliability and overall electrical parameters, however, the *planar epitaxial passivated* (PEP) diode structure has proven superior to all others. Some of the significant advantages of the PEP silicon diode include:

1. High forward conductance due to use of epitaxial material.
2. Low, uniform, leakage currents due to passivated surfaces.
3. Low capacitance due to small planar junction.
4. Low reverse recovery time due to accurate control of lifetime with gold doping.
5. High reliability due to passivation and rugged mechanical structure.

CUT AWAY VIEW OF PEP SILICON DIODE

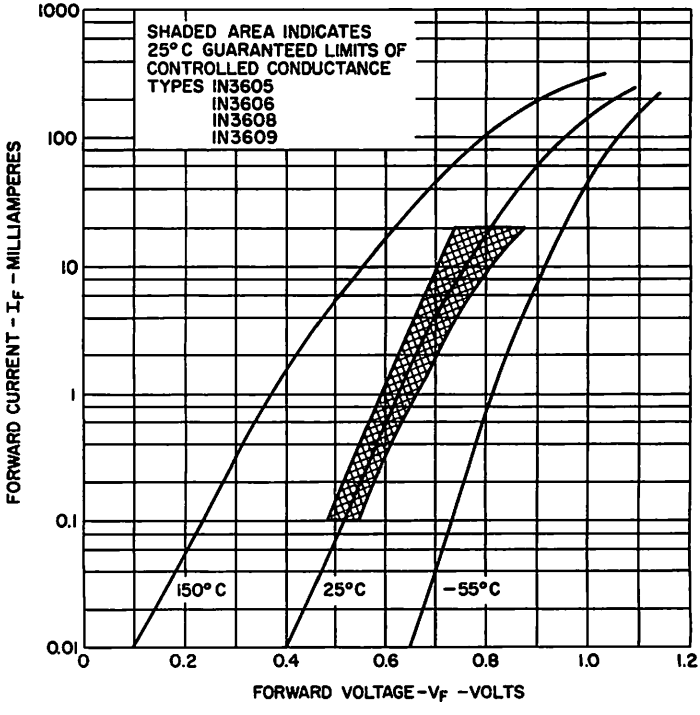
Figure 17.1

The cross-section and mechanical structure of a PEP silicon diode in a glass package is shown in Figure 17.1. Fabrication of the diode starts with a wafer of low resistivity single crystal silicon. A thin epitaxial layer of high resistivity silicon is grown on the wafer. A layer of silicon oxide is formed over the entire wafer and the oxide is removed from small circular "windows" by means of photographic techniques. The planar junctions are then diffused through the windows in the oxide. Gold is plated on the back of the wafer and diffused into the wafer at a temperature determined by the required reverse recovery time. The wafer is cut into pellets each forming a complete diode, and contacts are made to the front and back of the pellets. Each pellet is then mounted in a glass package and the package is sealed.

Formation of the junction under a stable silicon oxide layer results in a *passivated* diode which is immune to contaminants which plague other types of silicon diodes. The effectiveness of the passivation is substantiated by a tight distribution of reverse leakage current, a parameter which is usually very sensitive to surface conditions, and by the close correlation between the measured values of the electrical parameters and the theoretical values. The use of an epitaxial structure reduces the bulk resistance of the diode and thus makes it possible to achieve simultaneously a high conductance together with a low capacitance and a low reverse recovery time.

## DC CHARACTERISTICS

The characterization of the PEP silicon diode is greatly simplified by the close correlation between the theoretical and the actual parameters. The d-c characteristics are generally specified by means of the following parameters and characteristic curves.




**TYPICAL FORWARD DC CHARACTERISTICS OF PEP SILICON DIODES**

**Figure 17.2**

1. Forward Voltage. The maximum value of the forward voltage, $V_F$, is generally specified at one or more values of forward current, $I_F$. For *controlled conductance* diodes such as the 1N3605, 6, 8, and 9 both the minimum and maximum values of forward voltage are specified at six values of forward current. The relationship between the forward voltage and forward current for a typical PEP silicon diode is shown in Figure 17.2 at three values of ambient temperature. The shaded area indicates the guaranteed range of forward characteristics for the controlled conductance types at 25°C. The tight control of forward conductance is very desirable in the design of diode logic circuits where it permits greater design margins or additional logic stages (see Reference 1).

The forward d-c characteristics of the PEP silicon diodes closely follow the theoretical equation

$$I_F = I_S\left[\exp\frac{q\,(V_F - I_F\,R_S)}{\eta KT} - 1\right] \tag{17a}$$

where

$I_S$ = diode saturation current
$R_S$ = diode series ohmic resistance
$q$ = electronic charge ($1.60 \times 10^{-19}$ coulomb)
$K$ = Boltzmanns constant ($1.38 \times 10^{-23}$ watt sec/°K)
$T$ = absolute temperature (°K)

The parameter $\eta$ in the equation is dependent upon the impurity gradient in the junction and the carrier lifetime in the semiconductor material. At low values of forward current, carrier recombination in the junction depletion layer is the predominant factor in determining the relationship between forward voltage and current and $\eta \cong 2$. At high values of forward current the relationship between forward current and voltage is determined primarily by minority carrier diffusion and $\eta \cong 1$. The characteristics of the PEP silicon diode can be approximated with reasonable accuracy by assuming that $\eta = 2$ over the entire current range. At 25°C this gives $\eta KT/q = .052$ volt. The *dynamic resistance*, $r_D$, of the diode at a forward current, $I_F$, is given by the equation

$$r_D = \frac{\eta KT}{q\,I_F} + R_S \tag{17b}$$

2. Breakdown Voltage. The breakdown voltage, $B_V$, is normally specified at a reverse current of 5 $\mu$a. The breakdown voltage increases with temperature up to the point where the reverse leakage current becomes comparable with the current at which the breakdown voltage is measured.

3. Reverse Current. The reverse current, $I_R$, is specified at a voltage below the breakdown voltage. The reverse current increases exponentially with temperature as indicated by the equation.

$$I_R = I_{RO} \exp \delta\,(T - T_o) \tag{17c}$$

where $I_R$ is the reverse current at temperature T, $I_{RO}$ is the reverse current at temperature $T_o$, and $\delta$ is the fractional increase of $I_R$ with temperature. For the PEP silicon diodes $\delta \cong .055$/°C. The reverse current will increase by a factor of ten when the temperature is increased by $2.30/\delta = 42$°C. At low values of reverse voltage the reverse current is proportional to the square root of the voltage owing to the spreading of the depletion layer. At values of reverse voltage comparable to the breakdown voltage, the reverse current increases rapidly due to avalanche multiplication and localized breakdown effects.

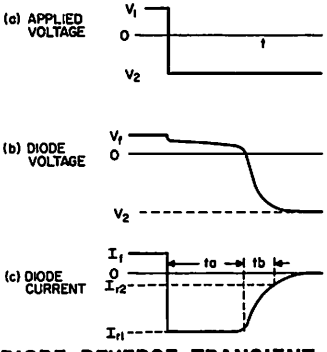
## AC CHARACTERISTICS

1. Capacitance. The capacitance normally specified for a diode is the total capacitance which is equal to the sum of the junction capacitance and the fixed capacitance of the leads and the package. The capacitance, $C_o$, is specified at a frequency of 1 mc with zero applied bias. Since the typical capacitance of the PEP silicon diode is less than 1 pf it is necessary to use a three terminal bridge configuration to achieve an accurate measurement. The junction capacitance is inversely proportional to the square root of the reverse voltage and increases linearly with temperature.

2. Rectification Efficiency. The rectification efficiency, $R_E$, is defined as the ratio of DC load voltage to peak rf input voltage to the detector circuit, measured with 2.0 volts rms, 100 mc input to the circuit. Load resistance is 5K and the load capacitance is 20 pf. The rectification efficiency is determined primarily by the conductance, reverse recovery time, and capacitance, and provides an indication of the capabilities of the diode as a high frequency detector.

3. Transient Thermal Resistance. The transient thermal resistance of a diode is presented by a curve showing the instantaneous junction temperature as a function of time with constant applied power. This curve permits a determination of the peak junction temperature under any type of pulsed operation. By means of a simple analytical procedure, described in Reference 2, this curve can be used to determine the peak junction temperature under any type of transient operation and hence provides a valuable method of insuring the reliable operation of diodes in pulse circuits.

4. Forward Recovery Time. If a large forward current is suddenly applied to a diode, the voltage across the diode will rise above its steady state value and then drop rapidly, approaching the steady state value in approximately an exponential manner. This effect is caused by the finite time required to establish the minority carrier density on both sides of the junction. The forward recovery time is the time required for the diode voltage to drop to a specified value after the application of a step of forward current. The forward recovery time increases as the lifetime or the resistivity of the semiconductor material is increased. For a given diode the forward recovery time increases as the magnitude of the forward current step is increased, and decreases as the forward current flowing prior to the current step is increased. If the amplitude of the forward current step is sufficiently small the effect of the junction capacity will predominate and prevent the diode voltage from overshooting its steady state value. For most diodes, particularly the PEP silicon diodes, the forward recovery time is much smaller than the reverse recovery time and can be neglected in most applications.

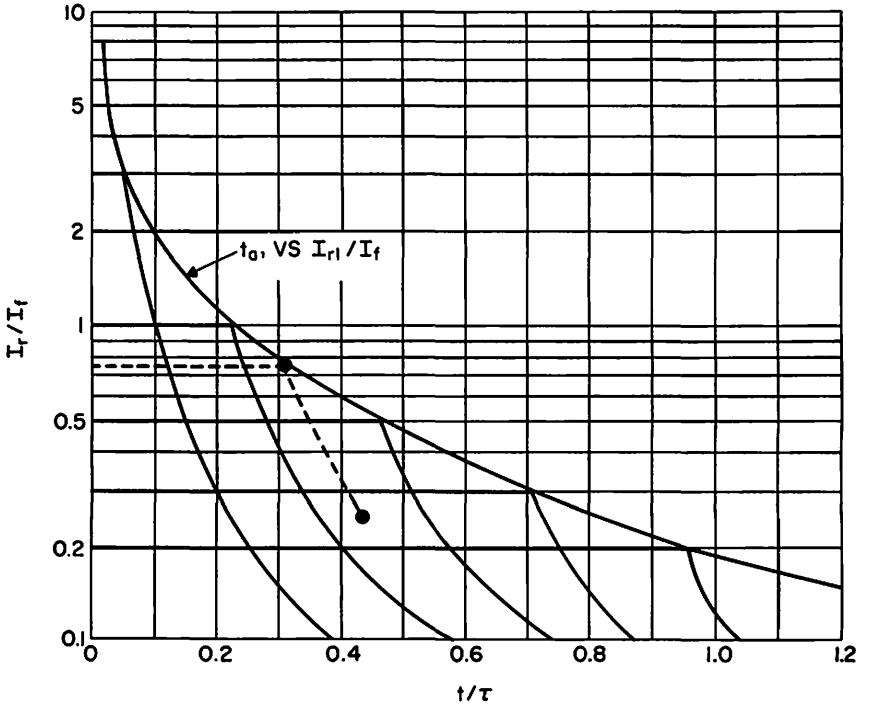



**TYPICAL DIODE REVERSE TRANSIENT WAVEFORMS**

**Figure 17.3**

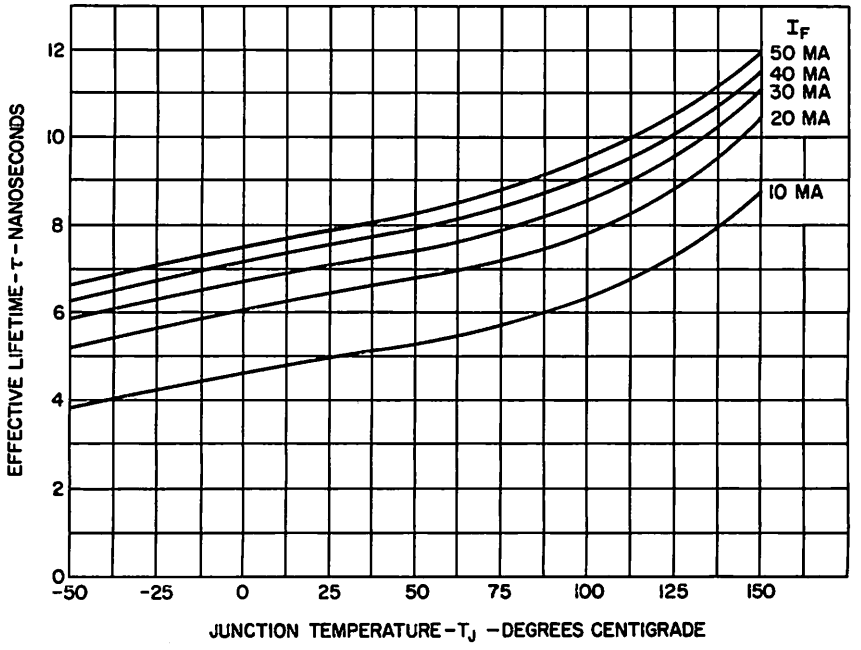
5. Reverse Recovery Time. When a forward biased diode is subjected to a reverse voltage step, a large reverse current will flow for a short time as a result of the stored charge consisting of the minority carriers on both sides of the junction. The typical voltage and current waveforms involved are shown in Figure 17.3. Initially, a current $I_F$ is flowing in the diode and a voltage $V_F$ appears across it. When the reverse voltage step occurs at $t = 0$ a reverse current $I_{r1}$ flows which is determined by the magnitude of the applied voltage and the loop impedance of the circuit. At the same time the forward voltage decreases by an amount approximately equal to $(I_F + I_{r1})\ R_S$ due to the reversal of the current through the diode. The reverse current remains constant at $I_{r1}$ for a time $t_a$ (the constant current phase) and then rapidly decreases, approaching the d-c reverse current value. At the same time the diode voltage goes negative and approaches the value of the applied reverse voltage.

The reverse recovery time of a diode, $t_{rr}$, is specified as the time between the application of reverse voltage and the point where the reverse current has dropped to a specified value, $I_{r2}$. The specification must also include the forward current, $I_F$, the initial reverse current, $I_{r1}$, and the loop impedance of the test circuit. The specification of the reverse recovery time of diodes is difficult to use for circuit design purposes because the recovery time is given only for one arbitrary test circuit and bias condition. Due to the wide variety of possible circuit arrangements and bias conditions encountered in diode applications, it is impossible for the manufacturer to control and specify the reverse recovery time corresponding to each special condition encountered.




**CURVE FOR DETERMINING REVERSE RECOVERY TIME UNDER VARIOUS DRIVE CONDITIONS**

**Figure 17.4**




**EFFECTIVE LIFETIME OF PEP SILICON DIODES VS. TEMPERATURE AND FORWARD CURRENT**

**Figure 17.5**

However, for most design requirements an accurate estimation of the reverse recovery time can be obtained by use of a quantity called the *effective lifetime*, $\tau$, and the ratio of the forward and reverse currents. Figure 17.4 can be used for this purpose together with Figure 17.5 which gives the typical effective lifetime of the PEP silicon diode as a function of temperature for various values of forward current.

The use of Figures 17.4 and 17.5 in estimating the reverse recovery time of a PEP silicon diode can be best described by means of the following design example.

Problem: Estimate the typical recovery time to 5 ma reverse current ($I_{R2}$) when the forward current is 20 ma ($I_F$) and the initial reverse current is 15 ma ($I_{r1}$) at a temperature of 75°C.

Solution: Enter the left side of Figure 17.4 at $I_{r1}/I_f = 15/20 = 0.75$ and follow horizontally (dotted line) until the $t_a$ vs. $I_{r1}/I_f$ line is reached. From the $t/\tau$ scale on the horizontal axis, it is seen that $t_a = 0.31\tau$. The $t_b$ portion of the curve is estimated by moving downward parallel to the general contour lines until reaching the line corresponding to $I_{r2}/I_f = 5/20 = 0.25$. The total switching time is thus $0.44\tau$. From Figure 17.5 the effective lifetime at $I_F = 20$ ma and $T_J = 75°C$ is 6.0 nsec, hence the calculated values are:

constant current phase $t_a = (0.31)\ (6.0) = 1.86$ nsec.

reverse recovery time $t_{rr} = (0.44)\ (6.0) = 2.64$ nsec.

For additional material on the reverse recovery time of diodes see References 3 and 4.

## DIODE ASSEMBLIES

The PEP silicon diodes are available in matched pairs and matched quads for use in applications where close matching in the forward characteristics is required. These units are sealed in small epoxy packages to preserve the identity of the diodes and minimize temperature differentials between diodes. The diodes used in these assemblies have all the high performance capabilities of the standard PEP silicon diodes and in addition are matched to within very close limits for $V_F$ over a range of forward current from 100 $\mu$a to 50 ma and over a range of temperature from $-55°C$ to $+125°C$.

These assemblies are used in discriminators, gating circuits, choppers, ring modulators and ring demodulators where the highest performance and reliability are required.

### REFERENCES

(1) Kvamme, E.F., "Controlled Conductance Applications," G-E Application Note 90.40.

(2) Gutzwiller, F.W., Sylvan, T.P., "Power Semiconductor Ratings Under Transient and Intermittent Loads," G-E Application Note 200.9.

(3) Chen, C.H., "Predicting Reverse Recovery Time of High Speed Semiconductor Diodes," G-E Application Note 90.36.

(4) Ko, W.H., "The Reverse Transient Behavior of Semiconductor Junction Diodes," IRE Trans. ED-8, March 1961, pp. 123-131.

# SEMICONDUCTOR RELIABILITY

CHAPTER 18

Of the many advantages which arise from the use of semiconductor devices in place of vacuum tubes, probably the most fundamental has been their long, reliable life expectancy. Early in semiconductor device development this was more anticipation than realization; but, by now, average failure rates of less than 0.01% per 1000 hours have been demonstrated in actual use[1] and life tests of longer than 40,000 hours (see Figure 18.9 – F and G) have shown that "wear-out" in semiconductors, if it actually exists, does not occur in the normal useful life of most electronic equipments.

Reliability is a measure of how well a device or a system can be expected to satisfy a set of performance requirements for a given period of time under a specified set of operating conditions. To be exact, this measure is the probability of successful performance. The basic reliability problem consists of two essentially different, but related, subproblems. This fact is frequently overlooked in current reliability thinking. The first, and by far the most important of the subproblems is that of designing, producing, and applying the device so that it actually will have the required reliability. The second subproblem, and the one which frequently receives all the attention, is the measurement of the reliability. It is not implied that measuring reliability is not important; but it is necessary to realize that the measurement of reliability in itself does not increase reliability. This difference becomes particularly important when the economic feasibility of lot acceptance tests to demonstrate extremely low failure rates is considered.

In both the achievement and measurement of reliability, there are major differences between systems and devices. In general, the system or equipment has to perform a somewhat narrowly defined function under a relatively narrow set of conditions for a relatively fixed period of time. For devices such as semiconductors which are mass produced, the ranges of applications, operating conditions, and required length of life are extreme. One transistor type in one application may be employed as a small signal i-f amplifier in a missile whose useful life is measured in minutes, and in another application may be employed in an air conditioned well maintained computer in a high level flip-flop where years of life are required. This diversity necessitates extreme care in the design, production, and evaluation to assure that the device will provide the required performance.

It is the purpose of this chapter to explain the factors which determine semiconductor reliability, and the techniques used in its measurement and to illustrate these with typical device reliability characteristics.

## ACHIEVING RELIABILITY

The achievement of reliability can only be realized through the proper *application* of devices which have been properly *designed* and properly *produced*. Any attempt to make one or two of these elements bear all the burden will result in higher costs and less than optimum performance. For example, placing excessive reliance on safety factors in application will result in heavier, bulkier, and more costly equipment which frequently will be slower in operation or be marginal in some other operational characteristic. Similarly, in device design, the specifying of a critical process in order to

obtain high performance will be paid for by uncertain yield and reliability. One aspect of the interdependence of these three factors in reliability which frequently is not sufficiently appreciated is the importance of feedback, feedback from the users of components to the producers and feedback from the production organization to the design organization. Most manufacturers have quite tight feedback paths between production and design. However, feedback from the "field" is generally much more difficult. A characteristic of many General Electric semiconductor devices is the means of permanent lot identification of each unit – which means that if at any time a unit should fail or exhibit unusual behavior, production records can be analyzed to determine possible causes. As this type of feedback continues, "field" experience can be factored into both production and design.

## DESIGN FOR RELIABILITY

### Mechanical Ruggedness

Mechanical ruggedness is a reliability *must*, not only for the end use but for the handling necessary to incorporate the device into an equipment. Mechanical ruggedness is achieved in design through incorporation of rigid assemblies, low mass, low moments of inertia, and through elimination of mechanical resonances in the normal range of vibration and shock excitation.

### Thermal Ruggedness

As important as mechanical ruggedness is thermal ruggedness. This is the ability to withstand rapid and extreme changes in temperature – whether caused by internal power dissipation or by external environmental changes.[2] The principles which are followed to assure reliability here are

1. The use of materials with matched temperature coefficients of expansion, and the use of hard solders to reduce the likelihood of metal fatigue
2. A low thermal resistance between junction and case to reduce thermal rise under power dissipation
3. The use of matched coefficient oxide seals in the headers to maintain a hermetic seal over wide temperature ranges. (Hard glasses and special metal alloys such as Fernico, Kovar, or Rodar are used to make these seals.)

### Surface Protection

Surface protection is one of the most critical factors in the design and production of semiconductor devices. General Electric device designs make use of one of two basic principles of surface protection – encapsulation in an inert atmosphere with a getter to maintain a satisfactorily low partial pressure of moisture; and passivation which is a process of deactivating and isolating the silicon or germanium surface with a chemically bonded protective film which shields the active surface from the influence of the gaseous environment and any contaminants which might come in contact with the surface. The first of these – internal atmosphere control – provides stability by initially establishing an internal atmosphere which gives satisfactory performance and then maintaining this condition by means of the getter. The getter is a material whose selective absorption characteristics have been chosen to provide maximum capacity for the removal of water vapor. The actual internal gaseous environment and getter must be selected specifically for each semiconductor design to optimize performance and reliability.

Passivation protects the surface of the semiconductor device by deactivation and by isolation.[3] Deactivation is the satisfaction of the unsaturated bonds of the semi-

conductor surface atoms by the formation of stable chemical bonds with a surface protecting film. The satisfaction of these unsaturated bonds greatly reduces the effect that electric fields have on the semiconductor behavior.

Isolation provides further stability by reducing the intensity of the electric fields reaching the semiconductor from charges residing on the outer surface. The thicker this passive layer or film, the greater the isolation. Furthermore, the passivation film will reduce the field intensity at the outer surface caused by the voltage across the junction depletion layer. This will reduce the tendency for surface contaminants to ionize and thus lead to still further device stability. Even in the case of passivated surfaces, the surrounding environment will exert some small influence and so for *maximum stability* it is desirable to provide a hermetic encapsulation.

In the case of the controlled environment method of surface protection it is obvious that hermetic encapsulation is essential. For these reasons, almost all transistors are hermetically sealed. Matched coefficient oxide seals give maximum assurance of a hermetic seal over wide temperature ranges. Although the use of copper leads and compression seals reduces the likelihood of lead breakage under severe installation conditions, it appreciably increases the danger of seal leakage and early failure caused by the influx of moisture and other contaminants. The cap to header weld, another important element of the seal, must be designed through proper shaping of cap, header, and welding electrode to give further assurance of a hermetic seal while eliminating the harmful effects of weld splash in internal contamination.

### Post Fabrication Processing

The factors brought out so far have dealt with the construction of the device. Certain elements of the design involve post fabrication processing. The most important of these is the stabilization performed on each unit. This is usually a high temperature bake for a period of days, the length of time depending on the device type.

The most important results of the high temperature bake is bringing the surface and the internal environment into equilibrium. In the case of devices using internal atmosphere control through getters, it is important to bring the internal surfaces of the device, the getter, and the internal gas itself all into equilibrium. Even though caps and headers may be prebaked at very high temperatures prior to fabrication, there is a certain amount of moisture and other gases that will be gradually evolved after fabrication. Furthermore, the getter will start acting on the gases in the unit as soon as it is welded. It is important to complete these changes and reach equilibrium prior to final testing so that the finished product will be stable. High temperature baking will in most cases accomplish this in a matter of a few days or a week.

In the case of devices where surface protection is provided by passivation, the stabilization bake is of much less importance. However, even well passivated units responds to a small degree to changes in internal atmosphere. A high temperature bake accelerates this process to give the ultimate in stability to the finished product.

### Reduction of Critical Processing

One of the responsibilities of product design when considering reliability is to reduce the critical nature of the manufacturing operation. When fabrication operations are critical, the vigilance of inspectors and quality control personnel must be increased and even then, some marginal units will slip through. By designing the product so that normal production tolerances will not produce early failures, the likelihood of marginal or poor units being delivered to the customer is greatly reduced. Poor units can then only be produced when the process is out of control and this situation can be readily monitored by the quality control function.

Many of the factors previously mentioned in connection with design for reliability also are important in connection with reducing the critical nature of manufacturing. For example, matched coefficient oxide seals are more easily produced without leaks than are compression bonds, resistance welding of the cap to header seal produces a more consistent seal than solder seals. The shaping of cap, header, and electrodes reduces the probability of weld splash contaminating the surface, the use of hard solders eliminates the need for fluxes and thus greatly reduces the chances of surface contamination. Gettering and passivation reduce the criticalness of many steps in production providing a major reduction in the probability of fabricating faulty units which could fail in operation.

### Examples of Reliable Design

Figures 2.8 through 2.11 show how these reliability design principles have been incorporated into General Electric transistors.

## PRODUCTION FOR RELIABILITY

Device reliability cannot be obtained through a design alone. The manufacturing operations must be established and maintained to assure that the design is actually followed – that is, the process must be kept in control. The most important factors pertaining to this element of reliability are workmanship, materials, environment, tools, screening, and quality control.

### Workmanship

Of all these, workmanship in the broad sense is the most important since the skill and attitude of every operator, maintenance man, inspector, and foreman contributes to the overall quality. Even in those cases of high level mechanization where need of human judgement and skill are greatly reduced in the direct fabrication steps, maintenance and control personnel, incoming material inspectors, and many others require high levels of skill to achieve reliability in the product. Factors which contribute to a high level of workmanship are morale, careful selection and training of personnel, managerial attitude toward quality (for example in General Electric Semiconductor Products Department, there are no piece rates; the emphasis is on making transistors right rather than making them fast), and performance feedback. This last point will be amplified in the section on quality control.

### Materials

The quality of the materials going into the finished product can be maintained at a high level through a combination of vendor control and incoming inspection. Vendor control starts with an evaluation of the vendor's product and of his facilities for consistently producing a high quality material. The second step is to maintain a rating on his performance combining price, service, and quality. This affords a factual basis for the selection of the best source for each material and a measure of the consistency of performance.

Most materials, particularly the direct materials can be subjected to an incoming inspection in the normal manner. A random sample of each lot can be taken and tested for the required characteristics. Failure to meet the requirements is cause for lot rejection. In those cases where screening is practical, failed lots may be screened to eliminate the faulty material and then resubmitted.

There are certain materials where this normal method is not applicable. Such situations arise in connection with the ultra-pure water used for cleaning and with gases

used in flushing and capping. The most appropriate manner by which to control the quality of these materials (in addition to adequate "vendor control") is to monitor the appropriate characteristics as the materials are used. This can be done in most cases by automatic recording monitors which have out-of-range warning indicators which forcibly bring to the attention of the production personnel that the material is out of limits. Typical characteristics which may be monitored are gas purity, dew point, and water resistivity.

### Environment

One of the most important factors in the manufacture of reliable semiconductors is the manufacturing atmospheric conditions, particularly humidity and dust. To reduce the effects of these factors to a minimum, *snow-white* and *dry-box* areas should be used for most operations, especially those after the device has been etched and cleaned.

The *snow-white* areas are rooms within rooms designed for the minimum tendency to collect dust and maximum ability to be cleaned. All air entering the areas should be filtered and a positive pressure should be maintained in the snow-white room so that any airflow is outward. All entrances into the rooms should have special shoe cleaning facilities. These areas should be vacuum cleaned regularly to remove what dust inevitably will leak in. To assure that the snow-white facilities are in order, dust count, temperature, and relative humidity should be monitored and recorded continuously with provisions for out-of-limits warning signals.

The *dry-box* is a further means of controlling the atmosphere in which manufacturing operations are performed. This technique is used where relative humidities are required which would be detrimental to operator health or where inert cover gases are required. The dry-box is an enclosed chamber completely sealed with trap doors for loading and unloading, and built in rubber arms for the operators to use for handling the devices.

### Tools

Another important factor in manufacturing reliable semiconductor devices is the tooling – both design and maintenance. Important characteristics of the tooling are that it requires little or no judgement on the part of the operator, that it be able to be set up readily and repeatably, and that it facilitate preventative maintenance.

### In-Process Inspection and Control

In-line control and inspection is the means that should be employed to assure that the product at each stage of production is within specification. This can be accomplished by monitoring the operating conditions of the tools such as fuzing temperatures, etch currents, by monitoring the characteristics of the water and gases being used and the environmental atmosphere as have been described, and by inspecting the product itself, electrically, mechanically, and visually. The importance of this aspect of reliable production cannot be over emphasized since this is the point where corrective action is most rapidly and effectively applied. This is the point where quality control can prevent poor production rather than reject it. Careful records of operators, materials, and machine maintenance will permit pinpointing and elimination of trouble spots. All reliability problems will not show up as defects detectable by these means; however, long experience has shown that an increase in the occurrence of those defects which can be thus detected are generally associated with a decrease in reliability.

### Screening

However, as the mechanisms of failure for each type of semiconductor device become known, means can be developed to screen out potential early failures. It must be emphasized that no two types of transistors necessarily have the same failure mechanisms, that no two products made by two different manufacturers, even though the same type, necessarily have the same failure mechanisms, and that no two products made at different times, even though the same type and made by the same manufacturer, necessarily have the same failure mechanisms. Therefore, reliability screening procedures must be determined separately for each product for each manufacturer for each period of time. The screening techniques generally are combinations of mechanical and environmental stresses utilizing device electrical parameter performance as criteria of quality. Almost all semiconductor products manufactured have passed through a reliability screen to some extent, but those products for use where the ultimate in reliability is required have very extensive screens. This subject will be covered in detail in a later section.

### Finished Product Quality Appraisal

It is not enough to set up a production line that *can make* a reliable product. It is necessary to provide some means of assuring that it *has made* a reliable product. That is one of the purposes of the quality control function in most semiconductor device manufacturing operations. This can be accomplished by properly sampling each production lot. The production lot may be defined as anything from a part of a day's production to a full month's production, but is most often considered as a week's production. The samples should be tested for conformance to the specified electrical, dimensional, and workmanship characteristics. In addition, they should be subjected to the specified mechanical and environmental and life test stresses. Certain of these sample tests should be restrictive, that is, if the sample fails the established criteria the lot should be rejected. Others of these tests may be for informational purposes only, used for optimizing the line performance or ascertaining the degree of safety factor between the product capabilities and the specification requirements.

A frequent characteristic of such testing is the use of failure criteria which are unrealistically tight compared to the normal use requirements (such as allowing only small percentage shift of the transistor current gain, or a failure definition of leakage current one or two orders of magnitude less than which would cause ordinary circuits to fail). This is done to provide a more sensitive control of production line performance.

### Quality Control

In most semiconductor manufacturing operations the quality control function not only carries out the end-of-line acceptance tests outlined above, but audits the many inspection and control operations in the incoming material and in-process areas as well, to make certain that they are being properly carried out. This provides an integrating means of tying together the great number of reliability factors important in production. A feature of General Electric transistors which makes this integration more effective is the date coding of each unit. Each transistor has embossed in its cap, just prior to main seal weld, a symbol which permanently identifies the time of production. This identification can be used to relate reliability problems with the many variables which are monitored at the various points in production. As has been previously mentioned this can also help to identify causes of failure in the field.

## APPLICATION FOR RELIABILITY

A perfect semiconductor device can exhibit very poor reliability if it is misapplied.

Reliable performance in equipment can only be achieved by selecting a device whose characteristics match those required by the function to be performed. This matching starts with the function to be performed and includes consideration of the environmental conditions and length of time of operation, the basic circuit configuration, the operating biases, the circuit margins allowed for, and the characteristics of the device itself. It is obvious that this matching process involves many interacting steps. Thus, to optimize the overall reliability requires much cut and try. For example, too much conservatism in circuit margins or derating on the device may make the individual sections of the equipment very reliable; but because the performance of the individual sections has been reduced, more sections are required resulting in an equipment with less overall reliability.[5]

## Function

The first step in applying semiconductors for reliable performance is to determine the circuit function to be performed. In many cases this is merely a matter of enumerating certain input, output, and transfer functions. However, in general, and for truly optimum equipment design, this step is part of the overall systems reliability design. There are usually many ways of solving a systems problems involving significantly different performance characteristics of semiconductors with resulting significantly different reliabilities. Control systems can be all electronic or they can be electromechanical. The requirements on the semiconductor devices are much different and so might be the overall reliability. A communications system can be strictly analogue or it can make use of pulse code modulation. Again the requirements on the semiconductors and the overall reliability will differ drastically. The application of semiconductor devices for optimum reliability starts with the recognition of their particular characteristics and the incorporation of this into the overall system design.

## Time

The second matching step has to do with time. The length of time that the equipment must perform may in many cases be the least controllable of the matching factors; however, frequently the length of time that a portion of the equipment must operate can be adjusted to improve a match. The element of time enters, in this manner, into the question of whether the equipment is subject to preventative maintenance, is reparable, or is a *throw-away*. Frequently when designing equipment from which very long life is expected, appreciable improvement in reliability can be achieved by utilization of the throw-away design since, if potting of the equipment or subassemblies is used, much better thermal characteristics can be obtained in the packaging. This, as will be shown below, will be beneficial. Furthermore, ability to withstand mechanical abuse will be greatly improved. The throw-away design will also frequently reduce the number of sockets and connectors which further improves overall reliability.

## Environmental Conditions

Some portions of the environmental conditions in which the semiconductor device will be required to function are sometimes beyond the control of the equipment designer. Generally, however, he has control over most conditions over at least a limited range. Generally speaking the ruggedness of semiconductor products minimizes the concern regarding the mechanical conditions which might be encountered *in equipment*. However, occasionally, it is found that unusual combinations of equipment packaging arrangements may set up resonances which will cause excessive stress in shock or vibration. These must be guarded against. Furthermore, there are some special application where such environments as high level acoustic noise or nuclear radiation are to be encountered. In these cases, particular attention must be given to selection of devices

best able to withstand these stresses as well as to protective measures which may be taken to reduce the level of the stresses.

The most important environmental factors which must be considered in reliability design are associated with temperature. Over the useful operating range, the higher the temperature the higher the failure rate is a safe rule. Furthermore, temperature cycling will tend to increase the failure rate relative to temperatures within the cycling range. (This will be discussed in detail in the section on failure mechanisms.) Once again, therefore, it is necessary to balance requirements on the system such as ambient temperature control or cooling against the improvement in failure rates to be obtained.

### Circuit Configuration

The recommendations so far have dealt primarily with the impact of the device on the system. Let us now consider the circuit design itself. A basic concept that should be followed for the design of reliable equipment is to make use of circuit configurations which have prime dependence upon the most stable semiconductor device characteristics and least dependence upon those characteristics which are least stable. Those transistor electrical characteristics which are most stable for most transistor types, both over temperature and time, are common base forward current gain ($h_{fb}$, $h_{FB}$), the common base breakdown voltage ($BV_{CBO}$), the input V-I characteristic – either common base or common emitter ($V_{EB}$, $V_{BE}$), and the output V-I characteristic in the "on" condition – either common base or common emitter ($V_{CB(SAT)}$, $V_{CE(SAT)}$). The least stable characteristics are the leakage currents ($I_{CBO}$, $I_{CEO}$, $I_{CER}$, etc.), the common emitter breakdown voltage ($BV_{CEO}$), and the common emitter forward current gain ($h_{fe}$, $h_{FE}$).

Consideration of this list points to the advantage of digital or on-off circuits which are primarily dependent upon the $V_{BE}$ and $V_{CE(SAT)}$ and must only be designed for a minimum value of $h_{FE}$ and a maximum value of leakage current. Where analog circuits are required, biasing methods which place most emphasis on $h_{FB}$ and a minimum on $h_{FE}$ and $I_{CBO}$ should be used. (See Chapter 7 on Biasing.) Feedback can frequently be advantageously employed, both within a single stage and around several stages, to minimize the effect of current gain variations and essentially reduce the requirement on this parameter to being above some minimum value.

### Operating Biases

A second circuit consideration for reliability is the choice of operating bias conditions. This is a very confused and uncertain area for two reasons:

1. The effect of voltage, current, power (temperature gradient within the device), and junction temperature on reliability depend considerably on the failure mechanisms to which the various devices may be susceptible
2. The ratings, which are usually used as the reference point for operating conditions for any particular device, are not consistently established relative to reliability either from device to device, manufacturer to manufacturer, or even stress to stress. It is obvious from this that blanket derating rules are of little value.

If we look at rating practices for the individual stresses we would find that

1. Voltage ratings usually are established as the breakdown voltage in one or more configurations leaving no margin of safety (furthermore, in some cases $BV_{CER}$ or $BV_{CES}$, which are always larger than $BV_{CEO}$, are specified and thus the ratings are not always applicable to all circuit conditions)
2. Maximum collector current is sometimes rated at a level at which the forward current gain drops to a uselessly low level, completely unrelated to reliability

3. Storage temperature is usually rated at the low end on the basis of what the customer would like to see (—65°C or —55°C), but sometimes at the lowest value where internal moisture condensation will not cause malfunction. At the upper end it is usually rated on the basis of life tests although the expected failure level may vary widely.
4. Power is almost always rated on the basis of life test but with a wide range of expected failure level.

Because of the variation in susceptibility of different failure mechanisms to the different stresses, because of the variations of the existence of different failure mechanisms in different device types, and because of the inconsistencies existing in the establishment of device ratings, derating should be applied with discrimination.

Caution should be applied in the matter of transients. Even though the average voltage, or the average current, or the average power are well within ratings, extreme care should be exercised to insure that voltage spikes (particularly important in connection with inductive loads) and excessive peak currents do not occur. Either of these can cause local hot spot temperatures which when repeated over a period of time can cause irreversible shift of parameters and ultimately outright failure.

Considering derating generally, there are several ways in which it can improve equipment reliability. If we assume we are concerned only in the area well away from voltage breakdown and hot spots due to excessive current, then we can say, further, that reducing the voltage while increasing the current has the advantages of lowering the impedance level so that surface effects are of much less importance.

Keeping the total power low will keep the junction temperature to a minimum and thus reduce the total junction temperature swing for which the circuit must be designed. These advantages will exist independent of improvement in failure rates which in the usual range of conditions will decrease with a decrease in stress.

## Circuit Margins

A third factor in the design of reliable circuits involves circuit margins — the limiting values of critical parameters at which the circuit will cease to perform satisfactorily. The wider the limit, obviously, the less likelihood there is that a parameter will exceed the limit and cause an equipment failure. On the other hand, wider limits usually result in lower performance which may decrease overall equipment reliability through a smaller system safety factor or through added complexity of more stages. An optimum must be established in determination of circuit margins.

A variation of this same problem of optimization has to do with the circuit performance considering all components simultaneously. One approach has been to assume that all components have their limit values in the worst direction simultaneously and design for adequate performance on this basis. Since the likelihood of this extreme combination happening in practice is infinitesimal, it is clear that this is too conservative for circuit reliability and may result in a less than optimum reliability design for the equipment and the system. Since the actual distribution of parameter values in temperature and time are rarely if ever normally distributed, the formal regression techniques cannot be applied. However, techniques have been developed which make more realistic assumptions than the "worst case" design.[6]

## Device Selection

This section describes the selection of the proper device for the application. The first step is to determine which devices have the electrical characteristics required. An

important rule to be followed is not to permit any parameter to have a critical role in circuit performance unless it is controlled by the specification. Reliance on *typical, nominal range,* or the observed distribution of small samples may be found to have been misplaced when production quantities are ordered.

If the distribution of a parameter is important it should also be specified by such means as a median control or by the use of dual min-max limits such that at least x percent fall within a tight set of limits and y percent fall within a looser set of limits (y>x). An example for $h_{FE}$ might be that 80% fall between 45 and 74 and that 99% fall within 30 and 90. The importance of specifying all critical parameters has been mentioned. It is equally important that parameters which are not important *not be* specified since this will only increase cost and reduce availability.

The selection of a device must also be based on its anticipated performance under the anticipated operating conditions. The first guide to this is the set of ratings for each device. However, it has been clearly pointed out that ratings are not at all consistent. Therefore, prior to even a preliminary selection, reliability data should be obtained. Since the user rarely, if ever, has time or money to obtain this information from his own testing, the device manufacturer must be able to furnish it. An evaluation of this data should be performed considering the life test conditions and end of life limits vs. the operating conditions and circuit margins anticipated in the circuit design. The derating factors which are to be used here, of course, should be based on as much factual data as the device supplier and the equipment designer have available to them and should consider the failure mechanisms to which the device is susceptible. Furthermore, mechanical and environmental test data should be obtained to ascertain that the device has sufficient safety factor to withstand those stresses to be encountered in the equipment.

It has been mentioned previously that the matching of device to function is a trial and error process since each step influences every other step. Thus, having made the first selection based on the above considerations the process should be repeated, re-evaluating each compromise in the light of succeeding decisions.

### Manufacturing Precautions

An extremely important aspect of application which has not previously been mentioned does not have to do with the equipment design, but its manufacture. Some of the most severe abuse that a semiconductor device encounters is received in the handling during acceptance, installation, and testing in the users plant. Semiconductor devices are mechanically rugged but the accelerations experienced when they are dropped even a little distance onto a hard surface can run into the thousands of G's and can harm units which are far stronger than necessary for the actual use conditions. Handling procedures for semiconductor devices should include provisions for preventing such drops and, in areas where the chances are still high, for cushioning the fall (such as foam rubber on a bench top where considerable handling is carried out).

Another means by which mechanical damage sometimes can be inflicted is the cutting of leads with a V shape cutting edge. At the time of separation of the portions of the leads, there is a high axial acceleration which is transmitted up the leads of the device proper. Tools for cutting leads should have a pure shearing action. Ideally there are no axial forces – in practice, very little. Machine shears are usually of this design. Cutting pliers which have one face vertical should be used for hand work; the vertical face of the pliers should face the semiconductor device.

Ultrasonic cleaning in the past has caused much trouble. When high energy ultrasonic vibrations are applied to semiconductors in the usual cleaning apparatus, the

probability is very high that a resonant frequency within the device will be excited. The accelerations which are then induced in the resonant portion of the device may be tens or even hundreds of times higher than the acceleration at the point of contact to the cleaning bath. Precautions which should be taken are to use the lowest level of excitation that provides satisfactory cleaning (3 psi average has been found satisfactory in many applications), and to monitor the pressure level over all the useful area of the bath since in most installations there are wide variations from point to point and time to time. It is also beneficial to use mass loading of the circuit board by the holding fixture to reduce the amount of acceleration transmitted to the device, to select an operating frequency as far removed as possible from any important internal resonant frequencies of the components on the circuit board, and to provide maximum stabilization of the exciter.

Another important manufacturing step which requires care is soldering. Damage to semiconductor devices by machine soldering is no problem since the temperatures and times which provide satisfactory soldering will not raise the internal temperatures above safe values. However, with hand soldering irons, particular care must be taken since the soldering iron temperature is much higher than most semiconductors can withstand. Precautions must be taken to prevent the device from coming to equilibrium with the soldering iron. This can be done by holding the device lead with a pair of pliers between the body and the point of application of the soldering iron and by keeping the soldering time to a minimum.

In handling semiconductors particular attention should be given to minimizing lead bending near the body of the device. Two types of damage may be caused – fatiguing of the leads themselves and cracking of the glass seal. Repeated insertion of devices into test equipment sockets, lead straightening, and mounting in the final equipment are operations which should be particularly guarded in this respect.

One of the most insidious forms of damage that devices suffer is that from transients in test equipment. These transients can cause instantaneous failure or they may cause performance degradation. If the transient occurs at the beginning of the measurement cycle, the device will appear as a failure or as having changed characteristics from previous measurements. If, on the other hand, the transient occurs at the end of the measurement, the damage may not be detected until further measuremnts are made or until the device is installed in an equipment. Whenever possible, all device leads should be short circuited during test equipment function switching, during card or tape punching (for automatic readout equipments), and at the time of application of biases.

## MEASURING RELIABILITY

The previous section was devoted to the achievement of reliability; this section will present information on how reliability can be measured.

The measurement of reliability can only be made, in the strict sense, by observing the performance of devices of interest in the finished equipment in actual use. For most purposes this is, of course, impractical as the information would be available too late to do anything if performance were unsatisfactory. Therefore, measurement of reliability must be carried out in some other way – but always it should relate to the ultimate measurement, performance in the finished equipment in actual use. How and when the measurements should be made depends upon what specific objectives are most important. Short of the final use test, the most appropriate method of measurement would be by simulated use conditions in actual circuits and for the length of time

that operation is required. This is still not practical for many purposes, particularly from the standpoint of the semiconductor device manufacturer. He must measure the reliability of his products when he doesn't even know in what circuits they will be used and when he only knows generally what the operating conditions will be.

The device manufacturer has three reasons for measuring reliability. He needs a knowledge of this characteristic for the control of his production line as it is just as important that he knows what the product failure rate is as that he know the production line yield. Since almost all vendor-buyer contracts have either an explicit or an implicit reliability requirement for lot acceptance, measurements must be made to determine eligibility for product shipment. Finally, circuit and systems designers need information on levels of reliability as a function of time, as a function of stress level, and as a function of circuit margins. Reliability measurements made in standard life test racks will not provide exact information but will give strong guidance for those who must convert this information into design decisions.

## MEASUREMENT OF RELIABILITY FOR APPLICATIONS GUIDANCE

Measurement of this purpose is best done by attributes since an equipment designer is primarily interested in whether a circuit will work or not and device stability, in itself, is usually not significant. The practicality of this measurement depends upon the required reliability. In those cases where failure rates of the order of 0.001% per 1000 hours are required, the sample sizes become so large that it is only in the most unusual circumstances that such measurements can be made.* A practical factor should be noted here; the measurement, testing and handling errors in even well designed and highly supervised measurement systems is at or above this level so that the problems of measurement at these degrees of reliability are more than just sample size. On a practical basis, reliability at the level of 0.001% cannot be measured but must be estimated from data taken at higher stress levels.

At lower levels of reliability (failure rates in the order of 0.1%) direct measurement becomes feasible, though expensive. For purposes of guidance to equipment designers it is not necessary to demonstrate this on a lot by lot basis but only as an average over a period of time. Thus long term (six months to one year) tests can be performed in which a small sample is put on test each production period. The results can be combined to give an average estimated failure rate for the particular product. If these small samples are put on test each period, at several stress levels (power, voltage, current, temperature), it is possible to perform a statistical regression analysis which will determine the relationship between failure rate and stress level. The data can be analyzed to determine, at each stress level what the relationship is between failure rate and the values of the critical parameters which are called failure. Similarly, the occurrence of failure in time can be analyzed to determine the form of the failure distribution.

In using this information, the circuit and systems designers must recognize that there are some factors which must be considered in relating the life test failure rates to in-use failure rates. Some of these life test factors are

1. Measurement errors on life tests
2. Test equipment failures which degrade units (oscillations on life racks, transients in measurement equipment)

*For example, with a sample of 230,000 transistors operating for 1000 hours, no failures could be allowed for a 90% confidence estimate of 0.001% failure rates; if one failure were to be allowed, the sample size would have to be 390,000. On the assumption of a constant failure rate, for 10,000 hours – about 15 months – one-tenth the sample size would be required. For a decreasing failure rate, which most devices exhibit, the reduction in sample size would not be as great.

3. Usually the definition of failure is tighter than the value of the parameter which would really cause malfunction
4. Usually the stresses – power, voltage, etc. – are more severe than in actual equipment
5. Whereas in actual application there is a significant probability that, if a parameter degrades, the other components in the circuit or in the system will have enough margin of performance to compensate for it, in life testing no compensation is considered.

To summarize, what is needed for measurement of reliability for applications guidance are long term, low stress, multi-level life tests spread out over a large production period. The data thus gathered must be analyzed (by attributes) to obtain the most possible information relating failure rate to stress level, definition of failure, and time.

## MEASUREMENT OF RELIABILITY FOR ACCEPTANCE

In almost every vendor-buyer contract there is an explicit or implicit requirement that the product have some acceptable level of reliability. Reliability measurement for this reason has considerably different requirements from that for applications guidance. The purpose of this measurement is to provide assurance that the reliability of the lot in question is not significantly poorer than that agreed to by the two parties. To be useful for lot acceptance, measurement must be made on each production (or shipping) lot, it must be performed in a reasonably short time (1000 hours is the currently accepted time), the stress conditions must result in failures similar to those which occur in use, and the results are most readily used if the measurement is in terms of attributes (failures vs. survivors).

It is well known that the sensitivity of an attribute sampling plan is dependent upon the number of failures which on the average will be observed. By sensitivity is meant the ability to differentiate between lots having average reliability and those that are much worse – or much better. There are only a limited number of ways in which the number of expected failures can be increased: increase time on test, increase sample sizes, tighten definition of failure, increase stress levels, and make use of product history.

The length of time on test is limited by factors of cost of inventory and logistics, 1000 hours appears to be a practical maximum with a need to reduce it. Sample sizes have been previously discussed; for low failure rate levels the required sample sizes are very large and costly. Tight definitions of failure will produce more failures; however, unless the failures produced correlate with failures to looser definitions actually important in the equipment, the test is worthless. The limit in this matter is reached when measurement errors produce an appreciable portion of the failures. Stress levels can also be made high. Here again, the failures produced must correlate with failures occurring in actual use conditions. At any stress level where the predominant failure mechanism differs from that at use conditions the results of tests at the high stress conditions will not be meaningful. The final method listed, used of product history, makes use of the premise that, if a production line is in continuous operation and is in control, the lot to lot variations will be small and that the main concern is with slower variations. There are many methods of using this principle. The simplest is to accept each lot based on the performance of it and some predetermined number of preceding lots. Other methods make use of sequential sampling or other continuous sampling

techniques but the broad principle is the same. One safeguard required in using product history is assurance of production homogeneity.

In practice, acceptance tests are designed by compromising on these five factors. Expected failure rates are set in the range of 0.1% to 10% in 1000 hours by selection of test conditions and definition of failure. Recently, use of product history has been incorporated for the lower failure rates to reduce testing costs. One practical method which has been employed to reduce testing costs for small lots without sacrificing reliability assurance has been the establishment of a *Bonded Warehouse*. Instead of performing life test and mechanical and environmental tests for each purchase order of 10 or 100 or even 1000 units to a particular specification, large lots, determined by production considerations, are accepted or rejected based on a single sample. Tests are performed under the surveillance of a government inspector or other surveillance agency as appropriate. Accepted lots are placed in a separate segregated warehouse. Shipments are then made to the particular specification directly to the customer. The customer receives the test report if requested.

## MEASUREMENT OF RELIABILITY FOR CONTROL

This type of reliability measurement has a lot in common with measurement for acceptance. It must be performed on a lot basis (production lot), to be effective the results must be known in a very short time, and the stress conditions should be carefully tailored to the prevalent failure mechanisms so that the most physically significant conclusions can be reached. In the case of measurement for control, attribute analysis is not necessary since the main requirement is to be able to ascertain whether the product reliability is remaining constant, improving, or degrading. Direction and rate of change of the parameter, rather than magnitude, is important.

## PAST PRACTICE, FUTURE TRENDS

In the past the three objectives of measurement of reliability have usually been combined into a test most closely related to the acceptance requirements with test conditions selected to protect the maximum ratings. This, of course, did not satisfy the control requirement because the time required for decision (125 hours for first read-out and 1000 hours for final decision) was too long for useful line control. The average number of failures usually was 0, 1, or 2 which meant that product reliability could change radically without showing as a significant change in the test results, and the tests were general purpose tests which were not specifically related to the prevailing failure mechanism. From the standpoint of application guidance, the test was not long enough (10,000 to 50,000 hours would be more reasonable), the stress levels were too high (users couldn't live with, in general, the failure rates expected at these levels), and the test conditions were not selected so as to permit regression analysis to relate failure rate to stress.

The trend for future measurement of reliability is to separate the three objectives, or at least use two sets of tests in place of one. Each of these would be optimized to achieve its particular objectives. The one set of tests would be for acceptance and control with test conditions selected to highlight the most important failure mechanisms. The analysis techniques and criteria of performance would be chosen as either attribute or variables, dependent upon the typical device performance, so as to maximize the sensitivity of the test to product change. The duration would be chosen to be one or at most a few days. The second set of tests would be directed to the problems of the user, optimized to provide application guidance. The form would be a small scale response surface (multi-level) test designed for maximum analysis efficiency. The stress levels would range from full rating downward. Small samples would be put

on test from each production interval and continued on for an extensive period of time. Analysis would be performed periodically (such as every six months).

This approach to the reliability measurement problem would result in the manufacture of more reliable equipments because of the improved feedback for control of device manufacture and because of the improved guidance provided to circuit and systems designers.

## FAILURE MECHANISMS

Frequently in the preceding discussion reference has been made to *failure mechanisms,* the physical and chemical processes which cause semiconductor devices to fail. An understanding of failure mechanisms is essential for the design, production, and application of semiconductors if the maximum reliability is to be obtained. Figure 18.1 shows the major failure mechanisms which affect semiconductor devices and also shows the stresses which are most likely to indicate their presence in a device.

| FAILURE MECHANISM \ STRESS | MECHANICAL | | | | TEMPERATURE | | | ELECTRICAL | | | | MISCELLANEOUS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | STATIC FORCE | SHOCK | VIBRATION | PRESSURE (FLUID) | STATIC | SHOCK | CYCLING | VOLTAGE | CURRENT | POWER (CONTINUOUS) | POWER (CYCLED) | CORROSION | ABRASION | HUMIDITY | RADIATION |
| STRUCTURAL FLAWS – WEAK PARTS | ● | ● | ● | ● | ● | ● | ● | | | ● | ● | | | | |
| – WEAK CONNECTIONS | ● | ● | ● | ● | ● | ● | ● | | | ● | ● | | | | |
| – LOOSE PARTICLES | | ● | ● | | | | ● | | | | ● | | | | |
| – THERMAL FATIGUE | | | | | | ● | ● | | | | ● | | | | |
| ENCAPSULATION FLAWS | | | | ● | | ● | ● | | | ● | | ● | ● | ● | |
| INTERNAL CONTAMINANTS – ENTRAPPED FOREIGN GASES | | | | | ● | | ● | | | | | | | | |
| – OUTGASSING | | | | | ● | | ● | | | | | | | | |
| – ENTRAPPED IONIZABLE CONTAMINANTS | | | | | ● | | | ● | | | | | | | |
| – BASE MINORITY CARRIER TRAPPING | | | | | ● | | | | ● | | | | | | |
| – IONIC CONDUCTION | | | | | ● | | ● | ● | ● | ● | | | | | |
| – CORROSION | | | | | ● | | | ● | ● | ● | | | | | |
| MATERIAL ELECTRICAL FLAWS – JUNCTION IMPERFECTION | | | | | | | | ● | ● | ● | | | | | |
| METAL DIFFUSION | | | | | ● | | | | | ● | | | | | |
| SUSCEPTABILITY TO RADIATION | | | | | | | | | | | | | | | ● |

**FAILURE MECHANISMS AND ASSOCIATED STRESSES**

**Figure 18.1**

### STRUCTURAL FLAWS

The *Structural Flaws* classification includes weak parts such as cracked pellets and nicked base or emitter leads, weak connections such as poor base lead welds, loose particles either conducting or non-conducting, and thermal fatigue. The failures included in this group may be due to design weakness, to production faults, or to misapplication. The weak parts and connections and loose particles terms are self explanatory. These can best be stimulated and detected by monitoring the device in an operating circuit either under shock or in vibration. The latter would be particularly effective if run at a resonant frequency for that portion of the device which is weakest. This is not easy to do, however, in most devices because of the high resonant frequencies involved, therefore a shock test is preferred. For applications encountering extreme levels of mechanical stress, static force (centrifuge) may be the only means

of uncovering weak parts or connections. Thermal stresses frequently will show up these faults through mechanical stresses and strains established by differential thermal expansion. Applied power may similarly be useful because of the thermal gradients set up.

### Thermal Fatigue

Thermal fatigue has been covered under *Achieving Reliability.*[2] The most important requirement of the stresses to be used to detect faults of this type is that the internal temperature of the device change rapidly. This change may be brought about by external means or by internal power dissipation. The latter is preferred.

Since the number of cycles required to show failure may be quite large, the duration of each cycle should be as short as possible. Frequently a five or six minute cycle can be used. Depending upon construction, the parameter which is most sensitive to failure may be $\Theta_R$ (thermal resistance), $h_{FE}$ (current gain), or $V_{CE(SAT)}$. In general, the last is the most useful.

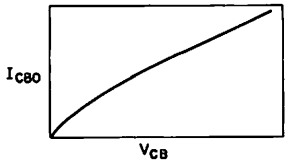
## ENCAPSULATION FLAWS

The second major classification of failure mechanisms is *encapsulation flaws.* These may consist of poor cap welds, cracked lead feed-throughs, permeability of plastic encapsulant, or imperfect passivation. The primary way in which these flaws may affect device performance is through the effect that moisture and oxygen which may leak in have on the device surface performance (see Figure 18.2).[7] Other gases which might penetrate may affect device performance but the fact that these two are so universally present gives them prime position. Since the parameters which are most affected by the surface changes are leakage current ($I_{CBO}$ is generally most important) and common emitter current gain ($h_{FE}$ or $h_{fe}$), these are usually monitored as indicators of the presence of this class of failure mechanism. However, other specialized measurements are required to pin point the actual mechanism as being a particular type within this class.

### Leak Detection

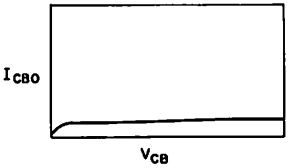
Humidity cycles (such as found in MIL-STD-202) and *detergent pressure bomb* tests are useful to detect flaws of this nature regardless of the type of construction. However, for certain types of construction, there are more sensitive (and more quantitative) measurement methods.[1] The best known is the Radiflo* which makes use of krypton 85 as a tracer gas. It is claimed that this is sensitive down to a leak rate of $10^{-13}$ cc/sec at standard temperature and pressure. However, in production, testing time limits the useful sensitivity to about $10^{-11}$ cc/sec. There are certain other limitations. The device must not retain any radioactivity when there are no leaks (this rules out most potted devices); if there are very large leaks in the hermetic enclosure, the tracer gas which has been forced in during exposure will escape prior to measurement and the very bad will appear good. This situation does not exist if there is a material within the hermetic seal which will retain any tracer gas which is forced in. In the majority of General Electric's gettered products, this is the case. Thus, General Electric is able to use Radiflo for 100% screening of most of its products – detecting *gross leakers* as well as marginal seals. For those cases where it does not detect gross leakers, Radiflo must be supplemented by a detergent pressure bomb test using $I_{CBO}$, $I_{EBO}$, or junction to cap leakage current as a detector of moisture penetration. This supplementary test has a sensitivity which overlaps the Radiflo sensitivity.

*Manufactured by the Consolidated Electrodynamics Corporation, Analytic and Control Division, Pasadena, California.



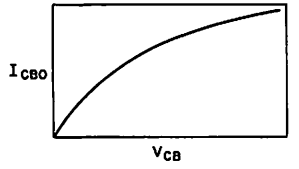

CONDUCTION CAUSED BY MOBILE SURFACE CHARGES, CURRENT DOES NOT SATURATE

PNP GERMANIUM TRANSISTOR WITH EXCESSIVE MOISTURE



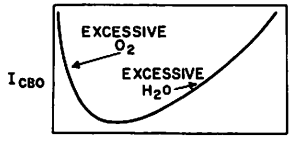

PRESENCE OF AN "$N^+$" SURFACE RESULTS IN LOW CARRIER GENERATION, CURRENT SATURATES.

PNP GERMANIUM TRANSISTOR WITH SLIGHT MOISTURE




PRESENCE OF A "P" SURFACE RESULTS IN INCREASED JUNCTION AREA, PARTIALLY "PINCHED OFF" BY LEAKAGE CURRENT THROUGH THE HIGH RESISTANCE P INVERSION REGION. AS VOLTAGE IS INCREASED, LESS IS "PINCHED OFF" AND LEAKAGE CURRENT INCREASES.

PNP GERMANIUM TRANSISTOR WITH EXCESSIVE OXYGEN




LEAKAGE CURRENT AS FUNCTION OF RELATIVE HUMIDITY

**INVERSION LAYERS AND THEIR EFFECTS ON JUNCTION LEAKAGE CURRENT**

**Figure 18.2**

A caution should be expressed here that detergent pressure bomb is not a satisfactory method of leak detection when grease or oil is used to provide temporary protection to the junction.

Two other methods of leak detection that have been used for hermetically sealed devices make use of helium. In one method helium is sealed into the unit at the time of encapsulation and then the units are tested for leakage of helium from the inside of the unit. The second method is a form of pressure bomb. The units are subjected to a helium environment at high pressure. If leaks exist some helium will be forced in. Then the units are tested for leakage of helium from the inside of the unit. The sensitivity of this method is reportedly about $10^{-6}$ cc/sec standard. Both of these methods suffer from the weakness that gross leaks will tend to release helium before the sensing instrument can be applied and so gross leakers will not be detected. Thus something similar to detergent pressure bomb is required here also.

In some unusual circumstances, stresses such as corrosion (salt spray) or abrasion (sand or dust) may cause failures because of inadequate or faulty encapsulation. Chipped paint which allows corrosion of the cap to occur is the only form of this which is common and this rarely proceeds to the point where device failure occurs. Special requirements should be given special consideration in these matters.

## INTERNAL CONTAMINANTS

One of the most important of the classifications of failures mechanisms is that of *internal contaminants*. They can be roughly classified as moisture, other foreign gases, and ionizable materials. They affect device operation through the induction of inversion layers in the semiconductor material itself, through modification of the surface oxides which may alter recombination center densities and rates of recombination, through irregularities at the junctions themselves, and through ordinary surface conduction.

### Entrapped Foreign Gases

One form of failure mechanism of this general classification is that of *entrapped foreign gases*. This is of most importance in greased units since the grease will protect the junction for a time. Thus, at the time of manufacture a unit will appear to be good. Later as the moisture penetrates through the grease to the juncion, it will affect the unit's performance. Greases which are not penetrated by moisture *eventually* do not exist. Leakage current ($I_{CBO}$ particularly), and current gain ($h_{FE}$ and $h_{fe}$) are normally the most sensitive parameters for the entire class of internal contaminant failure mechanisms. Failure caused by entrapped foreign gases is most rapidly brought about by high temperature storage. Even on non-greased units, high temperature operation or storage may cause slow changes in the surface conditions resulting in shifting of parameters.

One other factor should be considered here. Even though units work well at room temperature and at elevated temperatures, they may fail at or below freezing because of condensation of internal moisture. This can be detected by low temperature leakage current measurements. Extreme care should be taken in this measurement since condensation external to the device may produce misleading data.

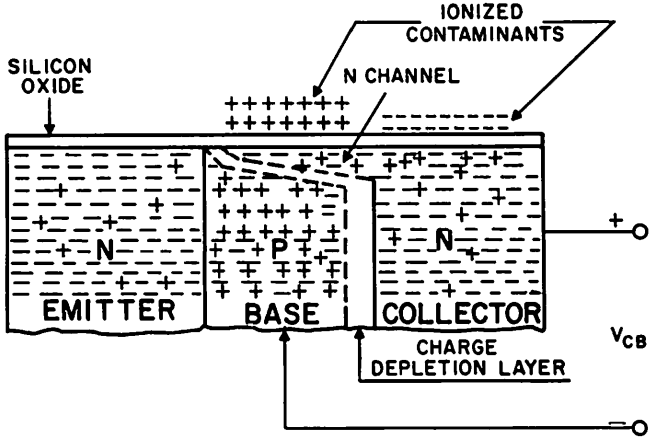
### Outgassing

*Outgassing* is probably the most important failure mechanisms for non-gettered, non-passivated devices. All surfaces have absorbed moisture and other gases. Under the influence of high temperatures, these gases will gradually be released until the concentration of gas within the enclosure is in equilibrium with gas in the surface. Experience with ungettered units has shown that this equilibrium point, even with processes which use very high temperature bake prior to capping, is high enough to produce semiconductor device failure through excessive leakage current. High temperature storage is the most useful stress in this case.

### Entrapped Ionizable Contaminants

*Entrapped ionizable contaminants* is a term describing a class of failure mechanisms in which ionizable materials in the presence of moisture and voltage ionize at a rate which is a function of temperature. These ions migrate under the influence of the voltage and may set up inversion layers.[8] Figure 18.3 is a pictorial representation of this action. Bar type devices generally are more susceptible to this migration failure than alloys or mesa types because of the narrow base at the surface (collector to emitter short). In rectifiers this inversion layer may short the junction to one of the ohmic

contacts. An interesting relationship exists between temperature and degradation with this mechanism of failures. For temperatures at and somewhat above room temperature, the degree of degradation which will ultimately be achieved will increase with temperature. However, if the temperature is increased still further, the rate of recombination of ions, due to thermal energy, overtakes the rate of ionization and the degree of degradation is reduced. The relationship between degradation and temperature is




**N CHANNELING IN AN NPN BAR STRUCTURE**

**Figure 18.3**

non-monotonic with a maximum depending on voltage, geometry, and degree of contamination (for some practical silicon devices it is in the range of 150°C to 200°C). If voltage is removed and temperature maintained, the ions will recombine and the contaminant molecules will redistribute themselves essentially in the original manner. The mechanism is reversible.

The stress which is most useful in detecting this mechanism is a combination of temperature and voltage. When taking the units off test for measurement, the voltage should not be removed until the units are cooled off. Leakage current (generally $I_{CBO}$) is the best indicator of failure for this mechanism.

### Ionic Conduction and Corrosion

*Ionic conduction* and *corrosion* are extreme cases of entrapped ionizable contaminants. When the level of moisture and contaminant reach a certain level, failure can occur due to ordinary conduction on the surface of the oxide film without the need of the induced inversion layers. When the amount of contaminant is even greater, actual chemical corrosion may take place. In this last case the failure may sometimes show up as an "open" rather than as excessive leakage. In all these cases, high temperature and voltage would point up the fault.

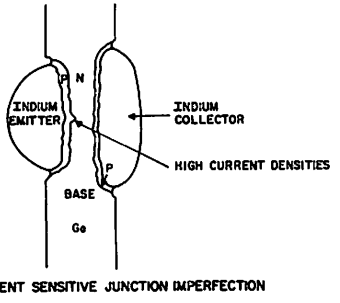
### Base Minority Carrier Trapping

Base minority carrier trapping is a somewhat different form of failure. This is dependent upon the density of surface states (allowed energy levels within the band gap) and on the difference in time constants between the slow surface states in the oxide layer on the surface (milliseconds to days) and the fast surface states within the surface of the semiconductor (microseconds). These factors in turn are influenced by

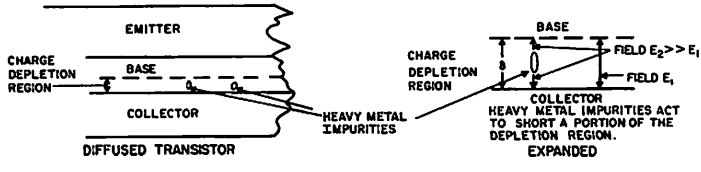
the surface treatment (degree of oxidation, etc.) and on gases in the enclosure. Initially the fast surface states act to keep the current gain low through high surface recombination. However, if a bias current is passed through the base continuously for a period of time the fast surface states will become filled and will remain filled. To maintain charge neutrality the slow surface states within the oxide layer, will slowly be emptied. Once this has been brought about, the current gain will be raised appreciably because the fast surface states are now maintained in a filled condition by the charge in the slow surface states. The stress which brings this about is primarily current. An increase in temperature will increase the rate at which this action takes place. However, if the temperature is raised beyond a critical point the amount of degradation will decrease due to the increase in speed of response of the slow surface states. If current is removed the slow and fast surface states will re-establish the original equilibrium and the unit is essentially as it was originally. The higher the temperature the faster the original equilibrium is re-established. The most critical parameter to monitor for this mechanism is current gain ($h_{FE}$, $h_{fe}$) although $I_{CBO}$ is also informative.

## MATERIAL ELECTRICAL FLAWS

A fourth major failure mechanism category is *material electrical flaws*. These flaws consist principally of junction imperfections. The junction imperfections may consist of two types, those which produce failure at high currents and those which produce failures at high voltages (Figure 18.4). Alloy or diffusion may result in an unequal penetration of the semiconductor by the doping agent resulting in the base having one or more relatively narrow separations between emitter and collector. These points will receive higher than average current densities which will generate local hot spots. As total current is increased, these local hot spots may reach temperatures where further diffusion or alloying will occur, resulting ultimately in a shorted base (collector to emitter). In some device designs, currents above ratings, such as under pulse conditions, can cause this same type of failure, even with no junction imperfections because of the distribution of current in the base region.




CURRENT SENSITIVE JUNCTION IMPERFECTION




**VOLTAGE SENSITIVE JUNCTION IMPERFECTION**

**Figure 18.4**

If the resistivity of the semiconductor material near the collector junction is not uniform, the depletion region will expand irregularly, as voltage is applied, giving rise to differences in voltage gradients in this region.[9] Differences in voltage gradients in turn will affect the collector multiplication factor producing unequal current distribution. This will only be important at high voltages approaching $BV_{CEO}$ or above. Below that point, the multiplication factor is so close to unity that variations in it would have no detrimental effect. However, near breakdown, the high local currents and high voltages can generate local hot spots which can lead to cumulative degradation and ultimate failure.

High current operation and high voltage operation at room temperature are respectively the best means of detecting the current and voltage sensitive junction imperfections. When these faults exist and are strongly stimulated, the results are usually catastrophic so that monitoring for opens and shorts should normally be adequate. If life test racks are used which do not allow burn out (through protective circuits) monitoring should be for changes in current gain ($h_{FE}$) or breakdown voltage ($BV_{CEO}$).

## METAL DIFFUSION

Another failure mechanism classification is *metal diffusion*. Whenever two metals are in intimate contact, whether compression bonded, alloyed, diffused, or welded, a disequilibrium is established. In accordance with the general laws of diffusion, the metals on each side of the interface will diffuse so as to establish an equilibrium condition. The rate at which this takes place is a function of temperature and the diffusion constants in the metals involved. Two general types of problems may exist; diffusion of dopants and ohmic contact material into the semiconductor material, and diffusion of ohmic contact materials and lead materials into each other. In the first type this may cause a decrease of base width with a resulting reduction in reach-through voltage (for some abrupt junction types) or a change in the resistivity profile which might result in a change in avalanche breakdown or other parameters. In the second type, changes which have been observed are weakening of base or emitter leads by the creation of brittle alloys and increases in ohmic resistance through the forming of high electrical resistivity alloys. In general these types of failures are of minor concern since even if the failures could occur, the rate of diffusion is so low that it would not occur in the useful life of most equipment.

## SUSCEPTIBILITY TO RADIATION

A failure mechanism which is only important in special applications – but then is vital – is that of *susceptibility to radiation*. There are two modes of failure

1. Temporary malfunction caused primarily by transient gamma radiation pulses
2. Permanent degradation resulting primarily from the total fast neutron dosage.[10,11]

The temporary degradation is due to both volume and surface ionization resulting in excessive leakage currents. These leakage currents may in some circuits produce permanent damage through thermal run away. Some decrease in current gain is sometimes observed during the transient burst.

Gamma radiation may cause permanent degradation as well as temporary if the total dosage becomes high enough. However, in the usual case, the fast neutron total dosage reaches the degradation level first. Degradation in this case is the result of decrease in the base minority carrier lifetime which in turn causes the current gain to decrease. Since this is a volume phenomenon, it is relatively predictable as opposed

to the transient leakage current effects which, because of the surface contribution, are relatively unpredictable. Exposure to a radiation environment is the only sure means of determining the ability of a device to perform in a particular radiation environment. Since this is extremely expensive and available time on appropriate reactors is so limited, a reasonable approach to this failure mechanism problem would be a unified, industry wide, semiconductor device evaluation program. Up to the present, no such program exists.

### FAILURE ANALYSIS

Both in the production of semiconductors and in their use, it is important that failures be carefully analyzed. Failure analysis when it is correlated with use (or test) conditions and with manufacturing variables can be the most powerful tool in improving reliability. It normally will indicate whether the failure was due to misapplication or operating abuse (screwdriver mechanics), to poor workmanship or materials, or to inadequate device design. This obviously is a start on the road to correction.

Since failures are relative rarities and since they are so vital in learning how to improve reliability, it is important that failure analyses be performed by properly trained personnel carrying out a thoroughly thought-out plan. Otherwise, not only may the real reason for failure be obscured but incorrect conclusions may be drawn which may lead to much wasted effort or even to a decrease in reliability. The subject of failure analysis is too complex to cover here in any detail. The most important areas of analysis that may be used to isolate the causes of failure are

1. Complete summary of operation and production history (as complete as possible)
2. Measurement of electrical parameters, including static characteristic curves
3. Special tests, more than one of which may be run in a sequence, such as
   (a) low temperature $I_{CBO}$
   (b) non-operating high temperature storage
   (c) high temperature with back bias
   (d) high temperature with forward current
4. Radiflow leak detection (where appropriate)
5. Gas analysis (mass spectrometer)
6. Special tests on the opened unit, more than one of which may be run in a sequence such as those listed above in number 3
7. Visual examination
8. Reprocessing and testing; such as rewash, re-etch, etc.
9. Metalographic Analysis.

Of course only those steps need be performed which are meaningful and only enough of them to draw a conclusion.

## FAILURE DISTRIBUTIONS

Reliability, as defined at the beginning of this chapter, is the probability of satisfactory performance for a specified period of time. If an appropriate statistical model of this probability as a function of time can be found, it can be used to advantage in improving reliability. Systems and circuit designers can take advantage of this to estimate reliability when optimizing their designs; it can also be used in planning maintenance systems and in determining the logistics requirements. Device manufacturers can use this reliability model to optimize life test acceptance plans, to screen produc-

tion so as to weed out potential failures, and to provide clues to failure mechanisms whose elimination will ultimately lead to product improvement.

## MATHEMATICS OF FAILURE DISTRIBUTIONS

There are many terms used in analyzing and describing the reliability of devices or systems. These are given and defined below:

Reliability Function – R(t) The probability of a unit (system, equipment, device) from a population surviving up to time, t. (also called survival function)

Cumulative Failure Function – F(t) The probability of a unit from a population failing before time, t.

Probability Density Function of Time to Failure – f(t) The limiting value of the ratio of the probability of failure in the time interval, $t+\Delta t$, over $\Delta t$ as $\Delta t$ approaches zero.

Instantaneous Failure Rate – Z(t) The limiting value of the ratio of the probability of failure in the time interval, $t+\Delta t$, *having survived to time, t,* over $\Delta t$ as $\Delta t$ approaches zero. This is the conditional probability density function.

These are all related and knowing any one as a function of time permits the others to be determined.

$$f(t) = \text{limit}_{\Delta t \to o} \frac{F(t+\Delta t) - F(t)}{\Delta t}$$

$$R(t) = 1 - F(t) = 1 - \int_o^t f(x)\,dx$$

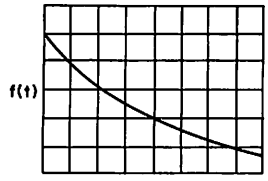
$$Z(t) = \frac{f(t)}{R(t)} = \frac{f(t)}{1 - F(t)} = \frac{f(t)}{1 - \int_o^t f(x)\,dx}$$

Relationships such as these are only useful if the observed probability of survival, R(t), or the more commonly used term, instantaneous failure rate, Z(t), can be expressed in mathematical terms and if the product characteristics are consistent enough to make calculations meaningful. Extensive testing by many semiconductor manufacturers have resulted in three mathematical models being found applicable over certain portions of the useful life of the devices. These are the Weibull, [12,13,14] the exponential,[15,16] and the lognormal.[17,18] Figure 18.5 shows these three distributions in the form of the density function, f(t), and the instantaneous failure rate, Z(t). It will be noted that the exponential distribution is the same as the Weibull with the shape factor, $\beta$, equal to unity and the mean life, $\theta$, equal to the scale factor $\alpha$. For the case of the exponential distribution the instantaneous failure rate, Z, is constant in time and equal to the reciprocal of mean life $\left(Z(t) = \lambda = \frac{1}{\theta}\right)$.

For the Weibull distribution, the failure rate is decreasing continuously for values of $\beta$ less than unity and increasing for values of $\beta$ greater than unity. In some situations it may permit a better fit of the model to the data if a delay time, t, is introduced. This means that no failures occur until after a time, t. This delay is usually symbolized by $\gamma$. This changes the equations for the Weibull in Figure 18.5 to

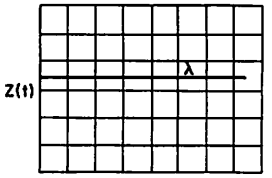
$$R(t) = \exp\left[-\frac{(t-\gamma)^\beta}{\alpha}\right], \text{ etc.}$$

The lognormal distribution has two parameters, the standard deviation, $\sigma$ and the




$$f(t) = \frac{1}{\theta} \exp\left[-\left(\frac{t}{\theta}\right)\right]$$

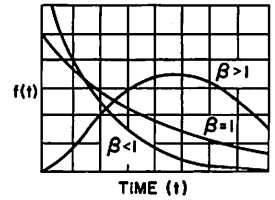
$$F(t) = 1 - \exp\left[-\left(\frac{t}{\theta}\right)\right]$$




$$Z(t) = \frac{1}{\theta} = \lambda$$

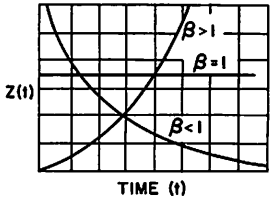
$$R(t) = \exp\left[-\left(\frac{t}{\theta}\right)\right]$$

EXPONENTIAL DISTRIBUTION




$$f(t) = \left[\frac{\beta t^{(\beta-1)}}{\alpha}\right] \exp\left[-\frac{t}{\alpha}^{\beta}\right]$$

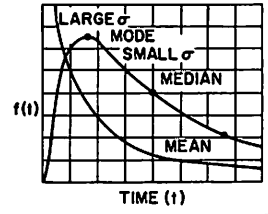
$$F(t) = 1 - \exp\left[-\left(\frac{t}{\alpha}^{\beta}\right)\right]$$




$$Z(t) = \frac{\beta t^{(\beta-1)}}{\alpha}$$

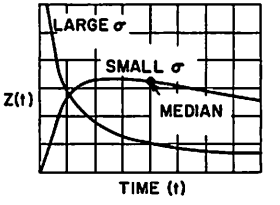
$$R(t) = \exp\left[-\left(\frac{t}{\alpha}^{\beta}\right)\right]$$

WEIBULL DISTRIBUTION




$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{\ln t - \mu}{\sigma}\right)^2\right]$$

$$F(t) = \frac{1}{\sigma\sqrt{2\pi}} \int_0^t \frac{1}{x} \exp\left[-\frac{1}{2}\left(\frac{\ln x - \mu}{\sigma}\right)^2\right] dx$$




$$Z(t) = \frac{\frac{1}{t} \exp\left[-\frac{1}{2}\left(\frac{\ln t - \mu}{\sigma}\right)^2\right]}{\int_t^\infty \frac{1}{x} \exp\left[-\frac{1}{2}\left(\frac{\ln x - \mu}{\sigma}\right)^2\right] dx}$$

$$R(t) = 1 - F(t)$$

LOG NORMAL DISTRIBUTION

**FAILURE DISTRIBUTION MODELS**

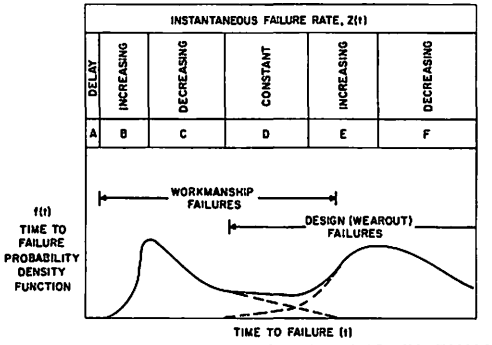
**Figure 18.5**

mean, $\mu$. In practice, the practical parameters used are $\sigma$ and $e^{\mu}$. This latter is the median life, the time by which one-half the units are expected to have failed. For the lognormal distribution, the median life is a more convenient measure of central tendency than the mean life because, unlike the latter, the median is independent of the

standard deviation. The lognormal differs from the other distributions in that over one portion of time the failure rate is increasing while over another portion the failure rate is decreasing. In fact, the instantaneous failure rate, Z(t), is zero both at time zero and at infinity.

## GENERALIZED FAILURE DISTRIBUTION

The general shape of the failure distribution density function, f(t), is shown in Figure 18.6 by the solid line. The descriptive terms for regions A through F refer to the instantaneous failure rate, Z(t), associated with the density function.



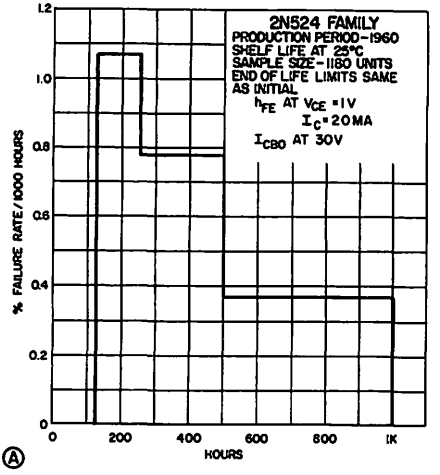

**GENERAL FAILURE PROBABILITY DENSITY FUNCTION**

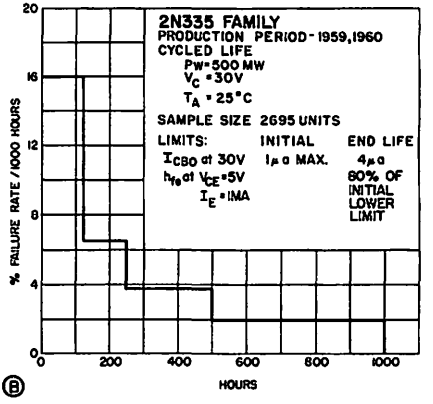
**Figure 18.6**

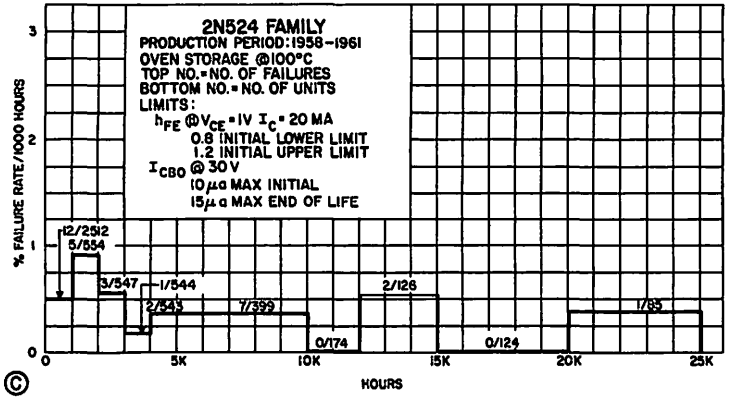
The delay (A) is due to the fact that the definition of failure almost always incorporates a safety factor beyond the initial parameter values and it takes some finite time for any units that are initially good to degrade to this end point limit. Of course, the lower the stress level, the longer this would be. At high stress levels this might be so short that it might not be seen. Region B is the transition region as the first units begin to degrade beyond the design margin. Region C covers the time that failures due to workmanship faults drop out. This generally is a decreasing failure rate and has been so observed in transistors, vacuum tubes, and other components. Two distributions have been found to fit regions A, B, and C very well. They are the Weibull distribution with a shape factor, $\beta$, less than unity and a delay term, $\gamma$, and the lognormal distribution. On transistor data, it has been found that these two can be equally well fitted to large quantities of data on many transistor types.

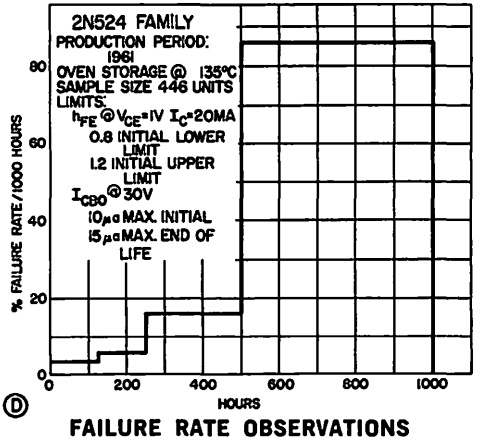
In Region D the failure rate appears to be essentially constant and relatively low. It can be hypothesized that this constant failure rate condition occurs because of the overlap of the decreasing failure rate of the workmanship failures and the increasing failure rate of the wearout failures of Region E and F. These overlapping distributions are shown by the dotted lines.

This generalized failure distribution model assumes that eventually everything wears out. In some component parts such as batteries or light bulbs the wearout mechanism is the exhaustion of a non-replaceable material. In transistors it is not so clearly defined. However, it may be the eventual leakage into the encapsulation of enough moisture to degrade this surface (even for well passivatd units this is possible) or it may be mechanical fatiguing of leads or mountings, or diffusion of doping materials or impurities into the semiconductor material. From the physical laws associated with these possible failure mechanisms, it is likely that the failure distribution in




**FAILURE RATE OBSERVATIONS**

**Figure 18.7**

regions E and F follow a lognormal distribution.[17] Considerable data from high stress level life tests show this pattern. Based on this, region E is the increasing failure rate portion of the lognormal distribution whereas region F has a decreasing failure rate.

Figure 18.7 presents four sets of failure rate observations which illustrate various portions of the general failure distribution model. Curve A shows regions A, B, and C for a germanium PNP alloy transistor life tested at shelf storage (25°C). Curve B shows the failure rate of an NPN silicon grown diffused transistor operated at full power rating (500 mw). Here the delay is so short that it is not observed in the operation of the life test. Curve C shows the long term performance of a PNP germanium allow transistor tested at rated storage temperature (100°C). This illustrates regions A, B, C, and D. The final curve, D, illustrates wearout, region E. The data was obtained from storage life tests at conditions well beyond the ratings on the same PNP germanium alloy type as that in curve A. The storage test was run at 135°C compared to a maximum rating of 100°C.

### PUTTING FAILURE DISTRIBUTIONS TO WORK

It has been pointed out that in regions A, B, and C both the Weibull and the lognormal distributions can usually be fitted to transistor life test data equally well. From a physical standpoint, the lognormal distribution appears to be more reasonable in that discontinuities such as those introduced by a delayed Weibull are not likely in nature. On the other hand, from the standpoint of the development of screening techniques and of improving sampling plans, the errors introduced by the use of the Weibull are small. The advantages of the Weibull as a working tool are primarily the completeness with which the shape factor, $\beta$, describes the rate at which the failure rate changes and the simplicity of the equations relating probability of failure to average failure rate, instantaneous failure rate, and mean life.[18]

In the next section, consideration will be given to *burn-in* for the improvement of reliability. An important factor in selecting the stress conditions for burn-in is the Weibull $\beta$, the set of burn-in conditions with the lowest $\beta$ (less than unity) will bring about the greatest improvement in failure rate in the least time. On the other hand, a $\beta$ greater than unity indicates an increasing failure rate in which case a burn-in actually will make the resulting product less reliable.

In the matter of sampling plans, the knowledge of the Weibull parameters of the failure distribution can lead to savings in testing costs if the distribution has a $\beta$ appreciably less than unity (and no appreciable delay). For example, if the beta is 0.5 which is typical, testing time can be cut to one-half by increasing the sample size by only 40% without changing the basic sampling plan. The result is a savings of 30% in the number of socket hours required. On the other hand, if the distribution has a delay, $\gamma$, or an increasing beta, this is a clear warning that reduced hour testing is dangerous and should be avoided. Much work is presently being directed, industry-wide, to greater use of the knowledge of failure distributions, particularly in the field of life test sampling plans.

## ACCELERATION FACTOR AND MODULUS OF FAILURE

Frequently through this chapter there has been mention made that high stresses generally will cause more failure than low stresses. It has also been pointed out that the definition of failure also determines the probability of failure. The subject of this section is the relationship between the probability of failure, stress level, definition of failure, and time. Much must be learned before this relationship can be based on solid theory; but a start has been made in its empirical determination.

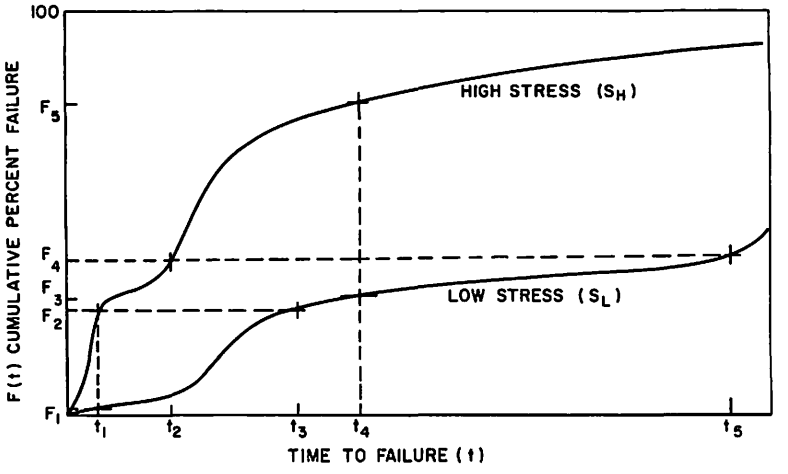
## DEFINITIONS

Before continuing, two terms must be defined: *acceleration factor* and *modulus of failure*. In the past the term acceleration factor, has been used to mean the ratio of failure rates at two stress levels or the ratio of times to obtain the same cumulative failure at two stress levels or the ratio of cumulative failure at a particular time at two stress levels. This one term can unambiguously mean all three of these ratios if – and only if – the instantaneous failure rate is constant over all time and if we are only concerned with low cumulative failure levels (say less than 10%). However, as has been shown in the previous section, constant failure rates are not the general rule. Therefore, more generally applicable definitions of terms relating failures, time, and stress level are needed if they are to be meaningful. Consider, first of all, the ratios of the failure rates. Referring to the generalized failure probability density function shown in Figure 18.6, it can be seen that the multi-valued nature of the instantaneous failure rate (increasing, decreasing, increasing, decreasing) would lead to an ambiguous and generally meaningless factor if ratios of instantaneous failure rates were related to stress levels. For this reason no such term should be used.

Next let us consider acceleration factor. Acceleration is generally regarded as the speeding up of a process or action. For this reason it is logical to apply the term, acceleration factor (A) to the ratio of the time of occurrence of a specified cumulative failure level at one stress level to the time of occurrence of the same cumulative failure level at a higher stress. Figure 18.8 shows hypothetical cumulative failure distributions for two life tests at different stress levels. These are the cumulative distributions associated with the general failure distribution model of Figure 18.6 with different time scales. The two equations for A below Figure 18.8 illustrate how the acceleration factor is determined. It is seen that, as the name implies, it is the factor by which the time to observe a particular level of failure is speeded up or accelerated with the increase of stress. From the illustration, it can be seen that this is not necessarily a constant factor as the level of cumulative failure is changed. The third ratio which has been loosely called acceleration factor concerns the ratio of cumulative failure levels at a particular time. A new term should be used for this. It is the modulus of failure (M) and is defined as the ratio of the probability of failure prior to a specified time at one stress to the probability of failure prior to the same time at a lower stress. The two equations for M below Figure 18.8 illustrate how the modulus of failure is determined. It is the factor by which the level of failure is increased with the increase in stress. The curves illustrate that this too is not a constant factor as time is varied.

A question which might be raised is why we need two different terms. To answer this let us first consider how the two might be applied. The first example is an equipment design problem where there is a specified operating time. The question to be answered is how operating stresses affect the failure level. Since we have a fixed time, the factor we need is the modulus of failure, M. In a second example, a device manufacturer is interested in performing an accelerated life test for lot acceptance purposes. He is interested in observing in one week the same level of failure that normally would take 3 years to occur. Here the failure level is fixed, the factor we need is the acceleration factor, A. Since in general neither A nor M is constant over all time and all levels of failure for a given device type and pair of stresses, it is clear that they are not generally equal nor related by a constant factor. Therefore, we must have the two factors for use in the different kinds of problems.

So far only stress vs. failure rate and time have been mentioned. The same kinds of relationships would hold if instead of two stress levels, we used two levels of definition of failure, the more stringent definition of failure taking the place of higher stress.




$$A(F_2, S_H, S_L) = \frac{t_3(F_2, S_L)}{t_1(F_2, S_H)} \qquad M(t_1, S_H, S_L) = \frac{F_2(t_1, S_H)}{F_1(t_1, S_L)}$$

$$A(F_4, S_H, S_L) = \frac{t_5(F_4, S_L)}{t_2(F_4, S_H)} \qquad M(t_4, S_H, S_L) = \frac{F_5(t_4, S_H)}{F_3(t_4, S_L)}$$

**ACCELERATION FACTOR AND MODULUS OF FAILURE**

**Figure 18.8**

## RESPONSE SURFACE RELATIONSHIP

Figure 18.1 showed that there are many stresses which induce failure. It would be highly desirable, particularly from the circuit designer's viewpoint to know not only how each stress alone affects the probability of failure but also how the stresses in combination affect it. The *response surface relationship* provides the answer to this question. A response surface relationship can be considered as a multi-dimensional "surface" relating the probability of failure to many stresses at a given time. $F(t_i)$ is a function of voltage, current, power, ambient temperature, junction temperature, cycling rate, etc., at time $(t_i)$. A response surface can also be solved for the time to observe a given percent failure as a function of the stresses but since the first form is generally more applicable to the user's needs, that is the one most commonly solved.

To determine the relationship mentioned above requires considerable testing and analysis. This is particularly true when the stresses near those the circuit designer might employ are considered. If the device is worth using, the failure level will be so low at the use condition that extremely large sample sizes are required. Furthermore, limitations on testing accuracy and reliability provide a limit of significance independent of the sample sizes. Investigations are currently underway to determine means of making use of stability data under these circumstances; however, at present the solution is to test at high levels and to extrapolate the relationship down to the low levels. There is, of course, a major weakness in this approach in that there is no assurance that the failure mechanism which is accelerated at high stress levels is the one

that is important at low stress levels. For example, it is possible that at high power, the failure mechanism may be the excessive shift in current gain brought about by minority carrier trapping. At low power, failures may be caused by moisture leaking into the case through faulty seals. Although this type of risk exists with extrapolations there is presently little alternative within the realm of economic feasibility.

One important safeguard which should be included within response surface evaluation program is a field service performance feed back. Long term service in actual equipment with comprehensive reporting on failures and failure mechanisms can provide the cross check on the extrapolated estimations that is needed. Such information over a period of time can build up an understanding of the relationships between high and low performance that can make extrapolations very useful.

## SCREENING

The constantly increasing transistor reliability requirement is imposing a more and more severe responsibility on transistor manufacturers to eliminate not only poor designs and poor workmanship but even the so called *freaks*. Freak transistors may be considered to be the result of unusual combinations of factors which elude ordinary detection but will in use fail relatively early in life relative to most of the units. On large scale production lines, it is unreasonable to expect that this *freak rate* will be reduced to a level acceptable for some of the more severe reliability requirements. Even in those cases where the reliability requirements are no more severe than good production techniques can satisfy (for example 0.1% to 0.01% failure in 1000 hours), the assurance of this quality on either a lot basis or on a production history basis is not generally economically feasible. An approach to this problem which both increases the likelihood of detection of freaks and at the same time provides an indirect means of measuring reliability is *screening* (or post fabrication processing). Broadly, this consists of performing a sequence of inspections, measurements, and tests on all units, each with a set of criteria for rejection, then submitting all of the units remaining to a low level operating burn-in. This last provides final screening and, simultaneously, a measurement of the quality of the product.

In setting up the screening sequence, it is important to keep in mind what is being sought – freaks. Since these are generally unpredictable it is necessary to provide a screen that will stand a very good chance of detecting the freaks regardless of the form they take. Of course an understanding of the product can lead to an optimization through the knowledge of tendencies for one type of freak or another to occur, but too much reliance should not be placed on this knowledge. The screen should consist of inspections, measurements, and tests. Inspections and measurements are screening operations which do not affect the individuals but merely measure some significant characteristic. Tests are screening operations which apply a stress to the units in order to determine the unit's *strength*. In applying these stresses, it is important not to destroy units which would provide satisfactory performance in ordinary use and, even of more importance, not to damage good units in such a way that they appear satisfactory but have a reduced life expectancy. A knowledge of the product including data on long term life tests at high stress conditions provides guidance in this respect.

Below is a general outline of a screen sequence which might be used. (Steps 1 through 7 are primarily inspections and measurement).

1. *Visual inspection* – lead condition, critical dimensions (an example is misalignment of cap and header leading to greater tendency for development of leaks), paint or plating, etc.

2. *Electrical parameters screened* – so as to eliminate tails of tailed distributions and to provide ample safety margins within specification limits

3. *Static characteristics observed* – on oscilloscope, rejecting units with irregularities or excessive instability; observe both breakdown characteristic (off) and the saturation characteristic (on)

4. *Measurement of internal dewpoint* – through low temperature $I_{CBO}$, when applicable

5. *X ray* – for proper placement of internal structure

6. *Leak detection* – both Radiflo and detergent pressure bomb

7. *Diode leakage* current ($I_{CBO}$) stability, short term (such as 10-30 seconds)

(Steps 8 through 13 are primarily testing)

8. *Mechanical stress* – this may be monitored shock or repetitive tapping, centrifuge, etc., to look for intermittents or weak parts or connections

9. *Voltage stress* – probably a high back bias with high temperature; if operated in avalanche this can detect junction flaws.

10. *Current stress* – high power at lowest possible collector voltage

11. *Thermal fatigue* – rapid 50% duty cycle, high power, high current

12. *Temperature stress* – this might be high temperature storage only or it might be cycled high and low (–65°C) slow cycle (2 hours each cycle)

These "life tests" generally will produce results in a few days or a week if there is any weakness to detect.

13. *Burn in* – this would normally be on operating life test at power and voltage between rated conditions and expected use condition. The duration of this test might be from a few days to several weeks or even months. This test is intended to do three things: catch delayed failures from the accelerated tests, stabilize the transistors, and monitor final performance. On the premise that stability is essential for reliability, this portion of the screen can be used for reliability *assurance*. If more than a prescribed number of units change characteristics more than a specified amount, the lot can be assumed to be of substandard quality even after screening and should be rejected.

The screen inspections, measurements, and tests and the criteria of rejection must be tailored to each situation. Not only will the differences in transistor types affect the design of the screen; but, in addition, the required level of reliability and the allowable total cost will affect it. As the importance of eliminating potential failures increases, the duration of tests, the number of measurements, and the severity of rejection criteria will increase. This will generally increase the number of good units that will be rejected and will rapidly increase the cost. The balance between effectiveness of the screen and the efficiency will be determined by the balance between reliability requirement and cost.

The screening principles outlined have been applied to several different products at General Electric. No one screen has made use of all the steps shown in the sequence; however in some cases other tests have been included. The most comprehensive screen and the one whose effectiveness has been most carefully evaluated has been applied to the Minuteman version of the 2N335 (North American Aviation, Autonetics Division Type 703). The screen consisted of electrical measurements, Radiflo leak detection, monitored repetitive shock test, high power cycled operation, and high temperature storage. Following this there was a burn-in at 348 mw (rated 500 mw) for one week. When units which were acceptable after this sequence were operated for 2700 hours at

348 mw and compared on the same test to units not subjected to the screen, there was found a reduction in cumulative failure of 8 to 1. The tests are continuing to strengthen the measure of product improvement for long life operation.

## RELIABILITY DATA FOR TYPICAL TRANSISTOR TYPES

### EXPLANATION OF ANALYSIS AND PRESENTATION

The reliability data shown on the following pages are the results of both the routine quality control acceptance testing performed on the particular production lines and of special evaluation testing programs. The characteristics shown are on specific products which are representative of the General Electric product lines. There is one PNP germanium alloy (the 2N524 family), one NPN silicon grown diffused (the 2N335 family), one PNP germanium mesa (the 2N705 family), and one NPN silicon planar diffused (the 2N1613 family).

Two methods of analysis and presentation of reliability data are used, an attribute analysis of a large number of life test samples and variables analysis of a single sample (in some cases a few similar samples have been combined). As an aid in understanding these data, let us consider Figure 18.9, (A) and (D). Figure 18.9(A) is a plot of the average failure rate as a function of time to failure. The theoretical average failures rate is the average of the instantaneous failure rate, Z(t), over the interval of time considered. Empirically it is determined by dividing the percentage of those transistors which started on test in a particular time interval and failed by the duration of that interval. The unit of measure of time used is that in which it is desired to express the average failure rate. As an example, let us calculate the average failure rate (in percent per thousand hours) between 7,000 and 10,000 hours. From Figure 18.9(A) it can be determined that there were 286 transistors which started that interval. Of these, 2 failed for a percentage of 0.7%. Dividing this by 3 (3 units of 1000 hours each) yields 0.23% per 1000 hours average failure rate. The failure rate calculated by this means is shown by the heavy solid line.

Since such estimates have a sizeable element of uncertainty in them, it is desirable to indicate intervals within which there is a specified likelihood that the true values exist. These intervals are called confidence intervals. Since we are making an attribute analysis, the binominal distribution can be used to determine the limits of these intervals.[19] The eighty percent confidence intervals are shown in these figures by the shaded area. This may be interpreted to mean that of all the failure rates confidence intervals shown in these figures approximately four out of five will include the true value of the failure rate – one out of ten of the true values will be higher than the upper limit, one out of ten will be lower than the lower limit.

A word on how the data for these figures were obtained. The data for the first 1000 hours are the results of the routine quality control life tests which are restrictive on all General Electric products. The longer hours data are primarily the results of the extensions of these same life tests. However, beyond 1000 hours the sample sizes are substantially reduced. In some instances engineering evaluation data have been included in the long term data where they were pertinent. It will be observed that as the hours increase, the sample sizes decrease, fewer units having had the opportunity to reach the longer hours. There are many other ways in which this same data could have been presented. This method was chosen because it requires no assumptions of a particular failure distribution, nor implies any; it is readily applied in the case of diminishing sample sizes, and it clearly shows the various regions of the general failure distribution model.

For those who would wish to plot the data on cumulative probability paper (such as Weibull or lognormal), the following formula can be used

$$F(t_a) = [1 - R(t_a)]\ 100 = \left[1 - \prod_{i=0}^{a} \frac{N_i - n_i}{N_i}\right] 100 \cong \left[\sum_{i=0}^{a} \frac{n_i}{N_i}\right] 100$$

where $F(t_a)$ is the percent cumulative failure to time $t_a$

$t_i$ is the duration of test up to the $i^{th}$ measurement period

$i$ is the sequence number of measurement periods and varies from 0 to (a)

$R(t_a)$ is the percent survival to time, $t_a$

$N_i$ is the sample size starting the life test interval between $t_{(i-1)}$ and $t_i$

$n_i$ is the number of failures in the interval between $t_{(i-1)}$ and $t_i$

$\prod_{i=0}^{a}$ indicates the product of all factors with i having values of 0 through (a)

$\sum_{i=0}^{a}$ indicates the sum of all terms with i having values of 0 through (a)

The approximation is good for total cumulative failures less than 10%.

Let us now consider the second form of data analysis and presentation as exemplified by Figure 18.9(D). This method of analysis is intended to determine the degree of stability of the important parameters. In this form of analysis each transistor is considered rather than the few that exceed a relatively arbitrary limit. Although it is more difficult to interpret this data into failure rate calculations for equipments and systems, it is much more sensitive in showing trends which might anticipate the future. For example, the situation might exist where the observed percent failure is small because the initial distribution of the important parameters is considerably below the definition of failure; however if the entire distribution of that parameter was increasing substantially, this would indicate that a large percent of the units are heading towards failure.

Stability data is presented in terms of *percentiles*. A percentile is the value of the particular parameter being considered below which the specified percentage of the transistors are expected to fall. For example, in Figure 18.9(D) at zero hours, 95% of transistors are expected to fall below 12.5 microamperes.

In applying percentiles to life test data, several details should be explained. In calculating percentiles at the various measurement periods, every transistor which started the test is included even if it has completely failed and has been removed from test. Failures are included at one extreme or the other depending upon the mode of failure and how it would have affected an operating circuit. The only exceptions to this rule are transistors which were lost, damaged in measurement, or otherwise affected independent of the life test. These units are then removed completely from the sample, from zero hours on. If a plotted percentile leaves the range of the graph paper, the next reasonable percentile (usually 5 percentage points up or down as appropriate) is plotted for that and succeeding measurement intervals.

In plotting parameter distributions with time, it is necessary to keep the same sample throughout. If samples are added or subtracted (the latter is the more likely since some samples that might be combined in the early hours have not yet reached the longer hours), the differences in initial distributions will cause an apparent shift in parameters making it appear that the units are unstable.

## RELIABILITY DATA ON A GERMANIUM PNP ALLOY TRANSISTOR (Figure 18.9)

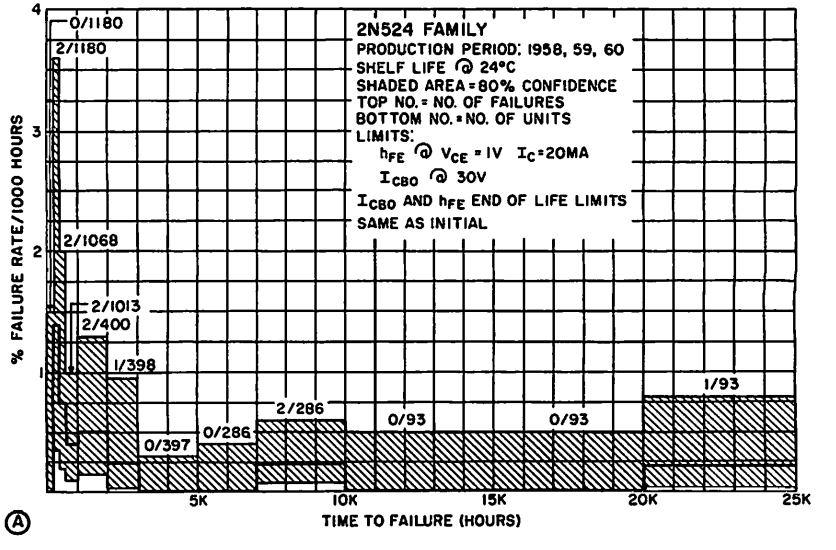
Graph A – It should be noted that the definition of failure for this test condition is very tight; the end of life limits are the same as the initial limits. Note the delay – no failures for 125 hours, then a sharp rise and a gradual decrease in rate of failure until by 5,000 hours it appears that a constant failure rate has been obtained.

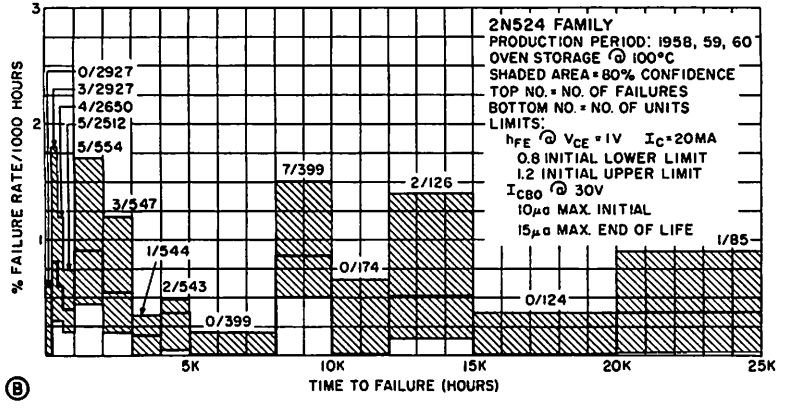
Graph B – The same general pattern at 100°C (maximum rating) but not as clear cut. Even though the definition of failure has been loosened the failure rate is higher in the constant failure rate region. This demonstrates the effect of higher temperature stressing.

Graph C – For this operating life test at full rated power, there is no apparent delay initially. The failure rate decreases, but slowly, until about 5,000 hours. After that it appears constant. The reason that this test only extends to 20,000 hours while the previous two went to 25,000 is that only the "on" time of the 50 minute on – 10 minute off cycle is counted; actual elapsed time is approximately 23,000 hours. The last 2,000 hours give the appearance of the start of wearout; however it will be noted that this is the result of only one failure. A study of the total sample of graphs D and E shows no shift of the main portion of the distribution up to this point leading to the conclusion that this is not the beginning of wearout.

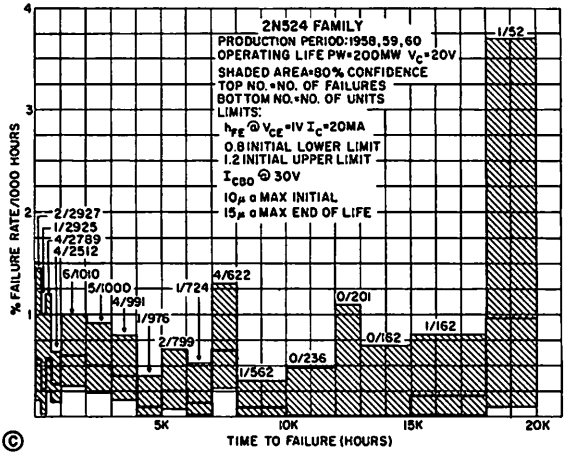
Graphs D & E – These curves show that on cycled operating life test the principal cause of failure is an increase in $I_{CBO}$. However, as has been pointed out, the main portion of the distribution is very stable. The $h_{FE}$ decreased for most units initially but over the last 10,000 hours was quite stable.

Graphs F & G – The units represented by these curves are early engineering samples utilizing the molecular sieve getter which has made this family of transistors so reliable. On high temperature storage, the stability of both $I_{CBO}$ and $h_{FE}$ is outstanding after the initial few thousand hours. Lack of signs of wearout at this high stress level after five years of testing indicates the long life which can be expected at normal use conditions.

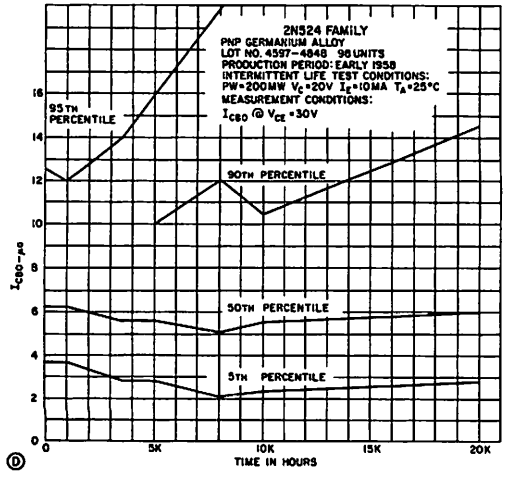



2N524 FAMILY
PRODUCTION PERIOD: 1958, 59, 60
OVEN STORAGE @ 100°C
SHADED AREA = 80% CONFIDENCE
TOP NO. = NO. OF FAILURES
BOTTOM NO. = NO. OF UNITS
LIMITS:
$h_{FE}$ @ $V_{CE}$ = 1V $I_C$ = 20MA
0.8 INITIAL LOWER LIMIT
1.2 INITIAL UPPER LIMIT
$I_{CBO}$ @ 30V
10μa MAX. INITIAL
15μa MAX. END OF LIFE
0/2927
3/2927
4/2650
5/2512
5/554
3/547
1/544
2/543
0/399
7/399
0/174
2/126
0/124
1/85
% FAILURE RATE/1000 HOURS
TIME TO FAILURE (HOURS)
5K
10K
15K
20K
25K

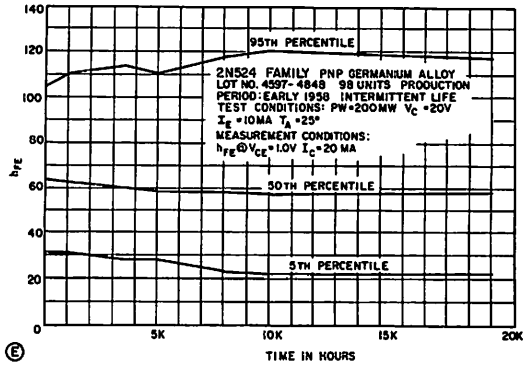
Ⓑ

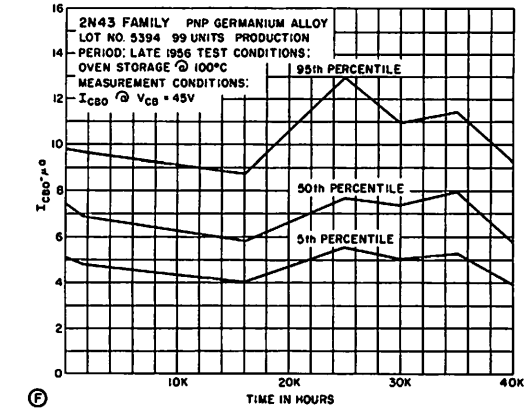

2N524 FAMILY
PRODUCTION PERIOD: 1958, 59, 60
OPERATING LIFE PW = 200MW $V_C$ = 20V
SHADED AREA = 80% CONFIDENCE
TOP NO. = NO. OF FAILURES
BOTTOM NO. = NO. OF UNITS
LIMITS:
$h_{FE}$ @ $V_{CE}$ = 1V $I_C$ = 20MA
0.8 INITIAL LOWER LIMIT
1.2 INITIAL UPPER LIMIT
$I_{CBO}$ @ 30V
10μa MAX INITIAL
15μa MAX END OF LIFE
2/2927
1/2925
4/2789
4/2512
6/1010
5/1000
4/991
1/976
2/799
1/724
4/622
1/562
0/236
0/201
0/162
1/162
1/52
% FAILURE RATE/1000 HOURS
TIME TO FAILURE (HOURS)
5K
10K
15K
20K

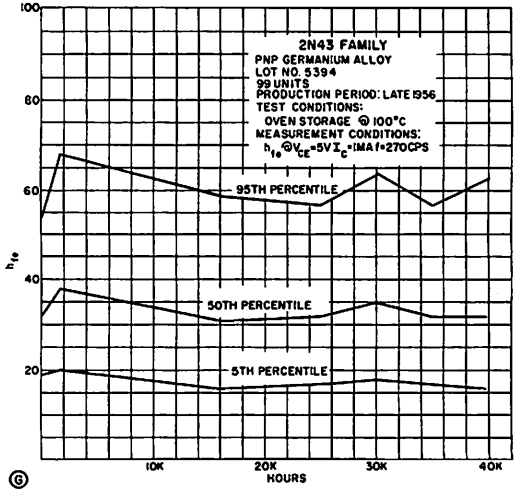
Ⓒ


2N524 FAMILY
PNP GERMANIUM ALLOY
LOT NO. 4577-4848 98 UNITS
PRODUCTION PERIOD: EARLY 1958
INTERMITTENT LIFE TEST CONDITIONS:
PW = 200MW $V_C$ = 20V $I_E$ = 10MA $T_A$ = 25°C
MEASUREMENT CONDITIONS:
$I_{CBO}$ @ $V_{CE}$ = 30V
95TH PERCENTILE
90TH PERCENTILE
50TH PERCENTILE
5TH PERCENTILE
$I_{CBO}$-μa
TIME IN HOURS
0
5K
10K
15K
20K

Ⓓ




**RELIABILITY DATA FOR A GERMANIUM PNP ALLOY TRANSISTOR**

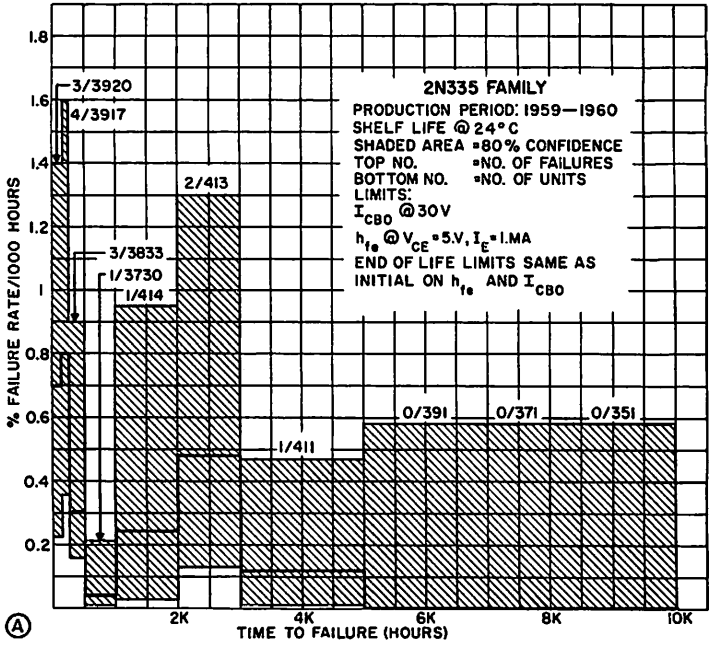
**Figure 18.9**

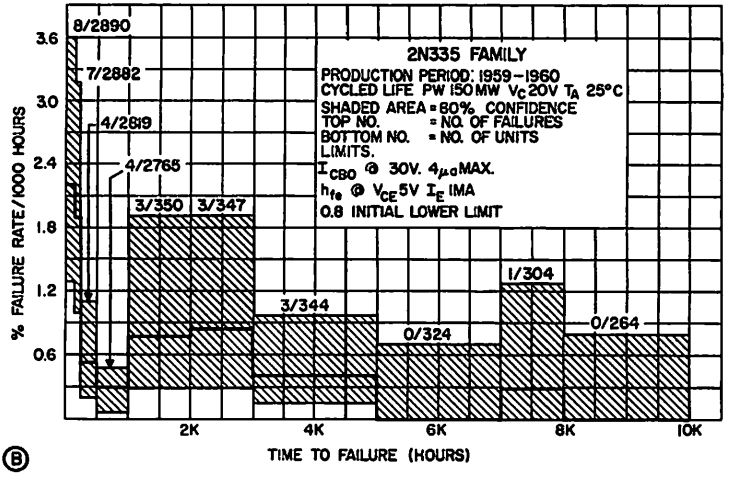
## RELIABILITY DATA ON A SILICON NPN GROWN DIFFUSED TRANSISTOR (Figure 18.10)

Graph A – The definition of failure limits on this shelf storage test are the same as the initial limits. As in the case of the alloy, there is an increasing failure rate initially followed by a rapidly decreasing failure rate.

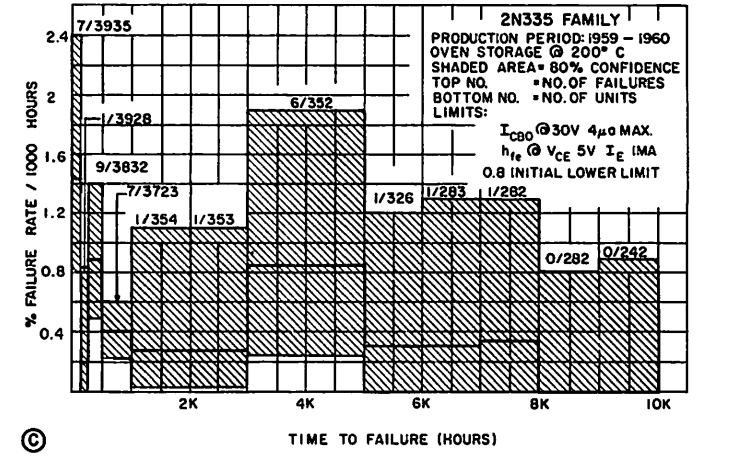
Graphs B, C, & D – All three curves show similar decreasing failure rate patterns right from the start with the 500 mw operating test the most extreme. Any delays which exist are not observed since the first set of measurements is made at 125 hours. The decreasing failure rate continues right out to 10,000 hours with no failures observed in the nearly 900 transistors (A, B, C, and D) between 8,000 and 10,000 hours.

Graphs E & F – These curves show that whether the stress is temperature alone or cycled power (both at full rating) the leakage current ($I_{CBO}$) is very stable. What changes there are in $h_{FE}$ are in an increasing direction which in most circuits is of little concern.

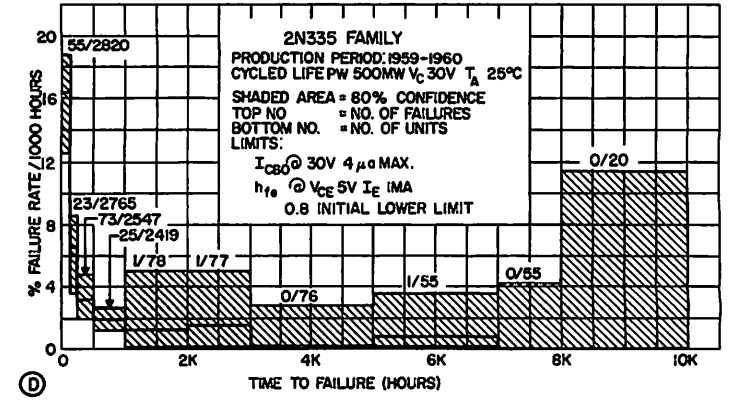



2N335 FAMILY
PRODUCTION PERIOD: 1959–1960
CYCLED LIFE PW 150 MW $V_C$ 20V $T_A$ 25°C
SHADED AREA = 80% CONFIDENCE
TOP NO. = NO. OF FAILURES
BOTTOM NO. = NO. OF UNITS
LIMITS.
$I_{CBO}$ @ 30V. 4μa MAX.
$h_{fe}$ @ $V_{CE}$ 5V $I_E$ IMA
0.8 INITIAL LOWER LIMIT
8/2890
7/2882
4/2819
4/2765
3/350
3/347
3/344
0/324
1/304
0/264
% FAILURE RATE/1000 HOURS
3.6
3.0
2.4
1.8
1.2
0.6
2K
4K
6K
8K
10K
TIME TO FAILURE (HOURS)

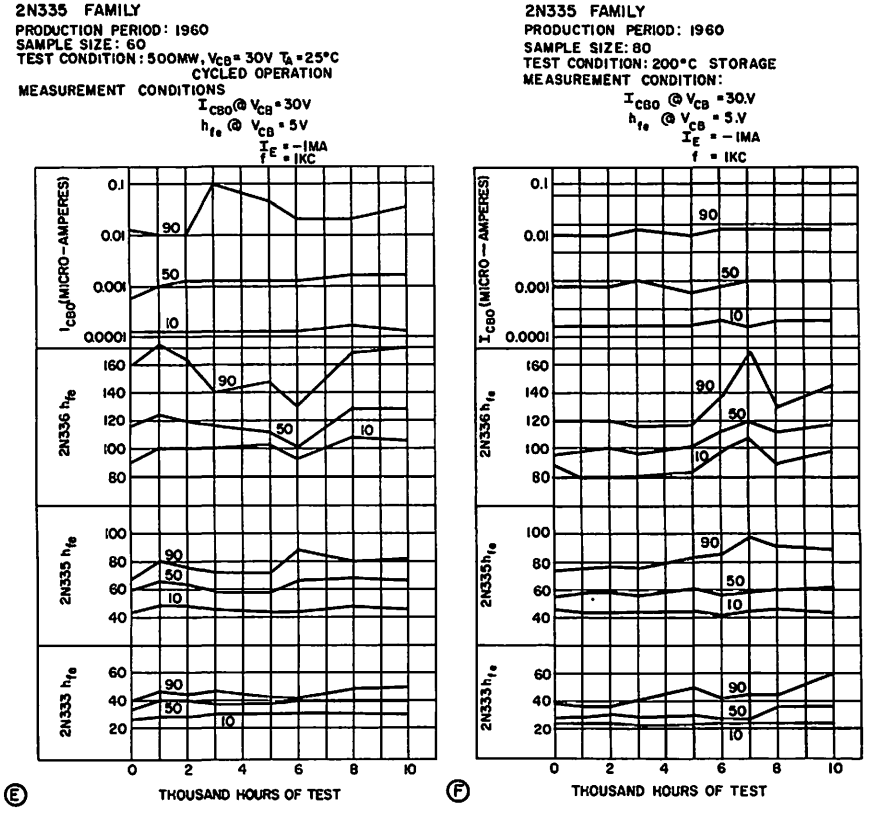
Ⓑ


2N335 FAMILY
PRODUCTION PERIOD: 1959 – 1960
OVEN STORAGE @ 200° C
SHADED AREA = 80% CONFIDENCE
TOP NO. = NO. OF FAILURES
BOTTOM NO. = NO. OF UNITS
LIMITS:
$I_{CBO}$ @ 30V 4μa MAX.
$h_{fe}$ @ $V_{CE}$ 5V $I_E$ IMA
0.8 INITIAL LOWER LIMIT
7/3935
1/3928
9/3832
7/3723
1/354
1/353
6/352
1/326
1/283
1/282
0/282
0/242
% FAILURE RATE / 1000 HOURS
2.4
2
1.6
1.2
0.8
0.4
2K
4K
6K
8K
10K
TIME TO FAILURE (HOURS)

Ⓒ


2N335 FAMILY
PRODUCTION PERIOD: 1959–1960
CYCLED LIFE PW 500MW $V_C$ 30V $T_A$ 25°C
SHADED AREA = 80% CONFIDENCE
TOP NO = NO. OF FAILURES
BOTTOM NO. = NO. OF UNITS
LIMITS:
$I_{CBO}$ @ 30V 4 μa MAX.
$h_{fe}$ @ $V_{CE}$ 5V $I_E$ IMA
0.8 INITIAL LOWER LIMIT
55/2820
23/2765
73/2547
25/2419
1/78
1/77
0/76
1/55
0/55
0/20
% FAILURE RATE /1000 HOURS
20
16
12
8
4
0
0
2K
4K
6K
8K
10K
TIME TO FAILURE (HOURS)

Ⓓ




**RELIABILITY DATA FOR A SILICON NPN GROWN DIFFUSED TRANSISTOR**

**Figure 18.10**

## RELIABILITY DATA ON A GERMANIUM PNP MESA TRANSISTOR (Figure 18.11)

Graph A – This graph shows a decreasing failure rate to about 500 hours and a constant failure rate continuing out to 10,000 hours. The data is on early production transistors.

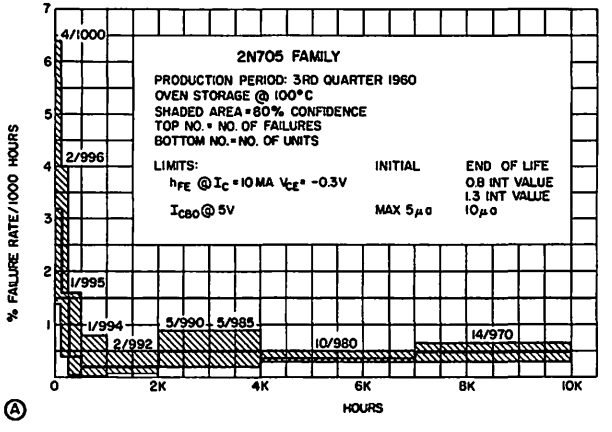
Graph B – Recently, the rating on this type has been raised to 150°C maximum storage temperature. Thousand hour data on recent production shows the product improvement. It also shows that although the number of failures are limited, there still is a decreasing failure rate after the initial buildup.

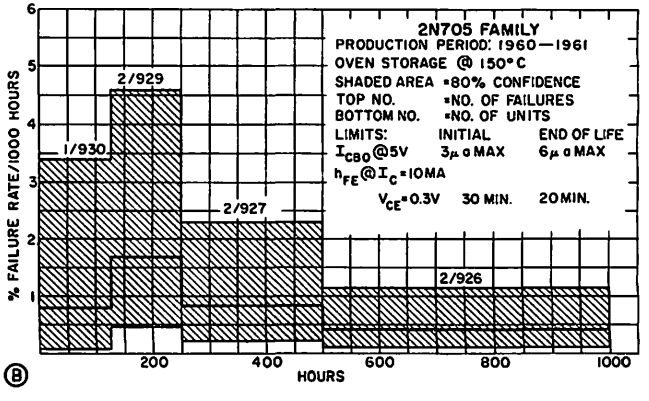
Graph C – The data shown on this graph is on early production units. This cycled operating life test data indicates that out to 10,000 hours there is a decreasing failure rate.

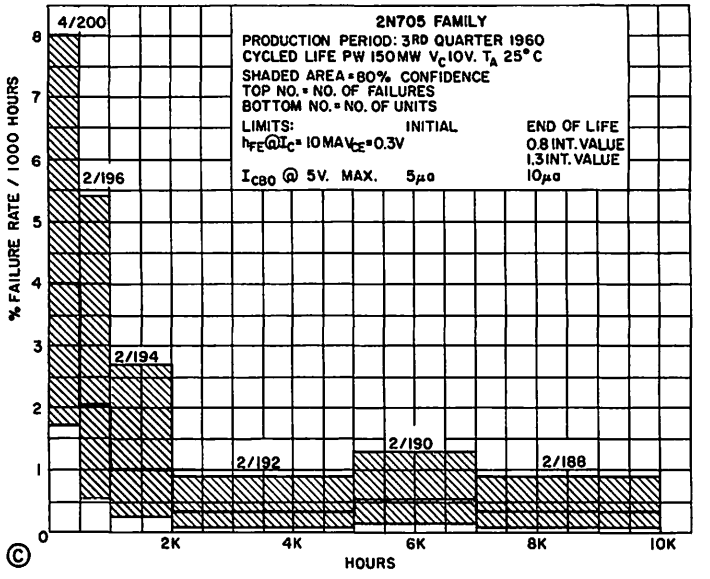
Graph D – More recent production showed a marked reduction in failure level. This graph shows this for the first 1000 hours. Even more recently, the rating on this type has been increased to 200 mw. Based on a sample size of over 400 units, there have not been sufficient failures to establish a failure pattern. The average failure rate for the latest product at 200 mw is compared on this graph to the average failure rate on earlier product at 150 mw. The improvement is evident.

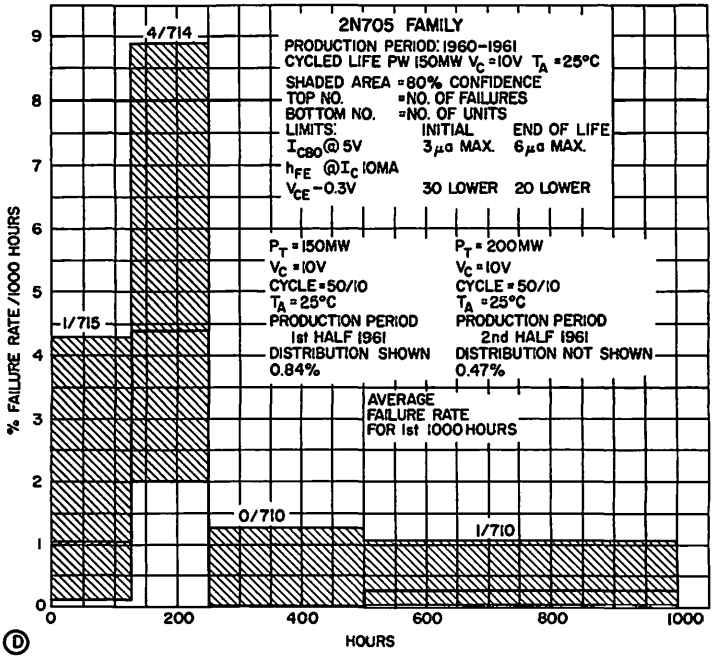
Graph E – The back bias life test data shown here consists actually of two life tests combined, one at 55°C and the second at 75°C. There were approximately equal sample sizes in each and approximately the same percent failure. The failure rate decreases very rapidly indicating the possibility of this test as a reliability screen.

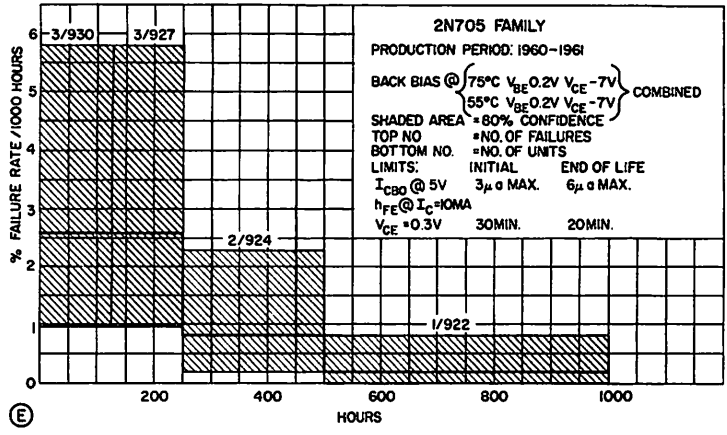
Graphs F through I – As in previous stability data, most change occurs in the first few thousand hours with a high degree of stability beyond. $I_{CBO}$ is the most common source of failures; but as can be seen from the medians, the bulk of the distributions are remaining constant or even decreasing their leakage current.

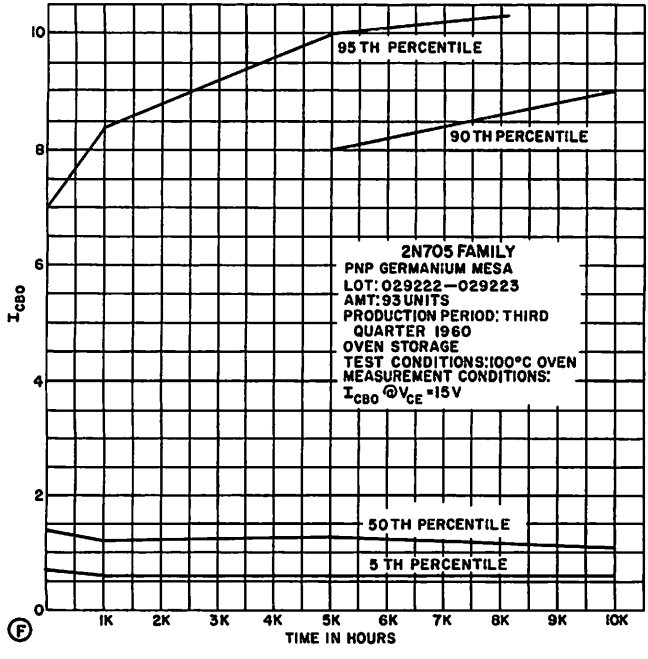


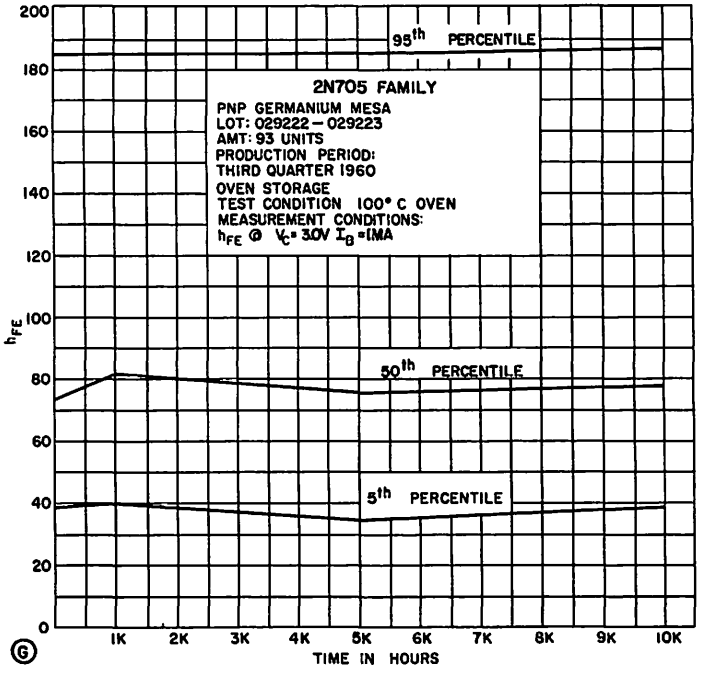




2N705 FAMILY
PRODUCTION PERIOD: 3RD QUARTER 1960
CYCLED LIFE PW 150MW $V_C$ 10V. $T_A$ 25° C
SHADED AREA = 80% CONFIDENCE
TOP NO. = NO. OF FAILURES
BOTTOM NO. = NO. OF UNITS
LIMITS: INITIAL END OF LIFE
$h_{FE}$@$I_C$ = 10MA $V_{CE}$ = 0.3V 0.8 INT. VALUE
1.3 INT. VALUE
$I_{CBO}$ @ 5V. MAX. 5μa 10μa
4/200
2/196
2/194
2/192
2/190
2/188
% FAILURE RATE / 1000 HOURS
HOURS
0
1
2
3
4
5
6
7
8
2K
4K
6K
8K
10K
©

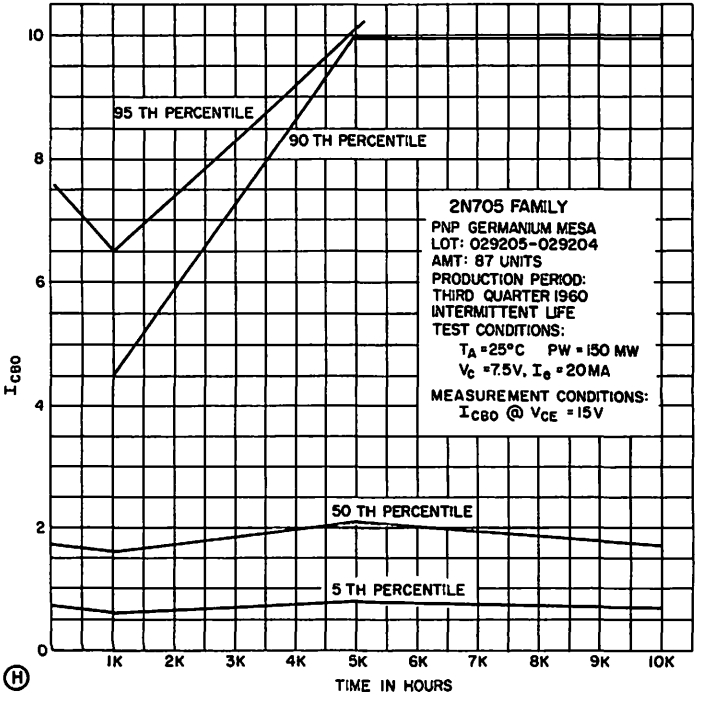

2N705 FAMILY
PRODUCTION PERIOD: 1960-1961
CYCLED LIFE PW 150MW $V_C$ = 10V $T_A$ = 25°C
SHADED AREA = 80% CONFIDENCE
TOP NO. = NO. OF FAILURES
BOTTOM NO. = NO. OF UNITS
LIMITS: INITIAL END OF LIFE
$I_{CBO}$@5V 3μa MAX. 6μa MAX.
$h_{FE}$ @$I_C$ 10MA
$V_{CE}$ -0.3V 30 LOWER 20 LOWER
$P_T$ = 150MW
$V_C$ = 10V
CYCLE = 50/10
$T_A$ = 25°C
PRODUCTION PERIOD
1st HALF 1961
DISTRIBUTION SHOWN
0.84%
$P_T$ = 200MW
$V_C$ = 10V
CYCLE = 50/10
$T_A$ = 25°C
PRODUCTION PERIOD
2nd HALF 1961
DISTRIBUTION NOT SHOWN
0.47%
AVERAGE
FAILURE RATE
FOR 1st 1000 HOURS
4/714
1/715
0/710
1/710
% FAILURE RATE / 1000 HOURS
HOURS
0
1
2
3
4
5
6
7
8
9
200
400
600
800
1000
Ⓓ


2N705 FAMILY
PRODUCTION PERIOD: 1960-1961
BACK BIAS @ 75°C $V_{BE}$ 0.2V $V_{CE}$ -7V
55°C $V_{BE}$ 0.2V $V_{CE}$ -7V
COMBINED
SHADED AREA = 80% CONFIDENCE
TOP NO = NO. OF FAILURES
BOTTOM NO. = NO. OF UNITS
LIMITS: INITIAL END OF LIFE
$I_{CBO}$ @ 5V 3μa MAX. 6μa MAX.
$h_{FE}$ @ $I_C$ = 10MA
$V_{CE}$ = 0.3V 30MIN. 20MIN.
3/930
3/927
2/924
1/922
% FAILURE RATE / 1000 HOURS
HOURS
Ⓔ

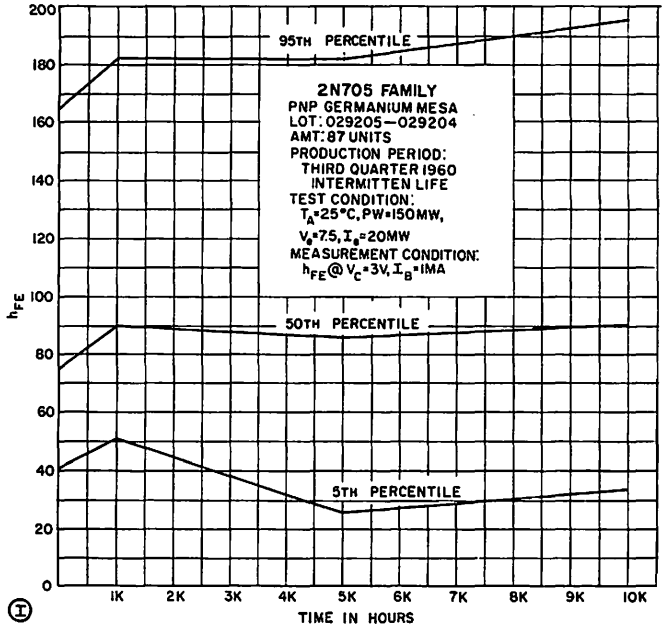

95 TH PERCENTILE
90 TH PERCENTILE
2N705 FAMILY
PNP GERMANIUM MESA
LOT: 029222—029223
AMT: 93 UNITS
PRODUCTION PERIOD: THIRD QUARTER 1960
OVEN STORAGE
TEST CONDITIONS: 100°C OVEN
MEASUREMENT CONDITIONS:
$I_{CBO}$ @ $V_{CE}$ = 15V
50 TH PERCENTILE
5 TH PERCENTILE
$I_{CBO}$
TIME IN HOURS
Ⓕ


95th PERCENTILE
2N705 FAMILY
PNP GERMANIUM MESA
LOT: 029222 – 029223
AMT: 93 UNITS
PRODUCTION PERIOD:
THIRD QUARTER 1960
OVEN STORAGE
TEST CONDITION 100° C OVEN
MEASUREMENT CONDITIONS:
$h_{FE}$ @ $V_C$ = 30V $I_B$ = 1MA
50th PERCENTILE
5th PERCENTILE
$h_{FE}$
200
180
160
140
120
100
80
60
40
20
0
1K
2K
3K
4K
5K
6K
7K
8K
9K
10K
TIME IN HOURS

Ⓖ


95 TH PERCENTILE
90 TH PERCENTILE
2N705 FAMILY
PNP GERMANIUM MESA
LOT: 029205-029204
AMT: 87 UNITS
PRODUCTION PERIOD:
THIRD QUARTER 1960
INTERMITTENT LIFE
TEST CONDITIONS:
$T_A$ = 25°C PW = 150 MW
$V_C$ = 7.5V, $I_e$ = 20MA
MEASUREMENT CONDITIONS:
$I_{CBO}$ @ $V_{CE}$ = 15V
50 TH PERCENTILE
5 TH PERCENTILE
$I_{CBO}$
10
8
6
4
2
0
1K
2K
3K
4K
5K
6K
7K
8K
9K
10K
TIME IN HOURS

Ⓗ




**RELIABILITY DATA FOR A GERMANIUM PNP MESA TRANSISTOR**

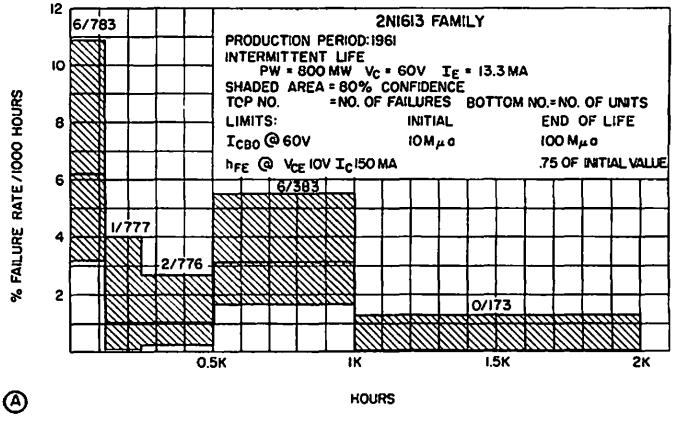
**Figure 18.11**

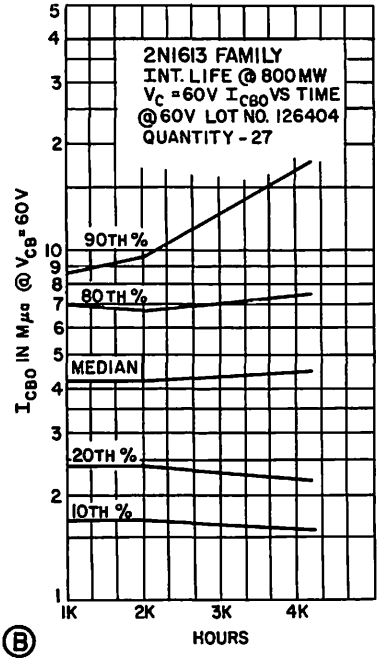
## RELIABILITY DATA ON A SILICON NPN DIFFUSED PLANAR PASSIVATED TRANSISTOR

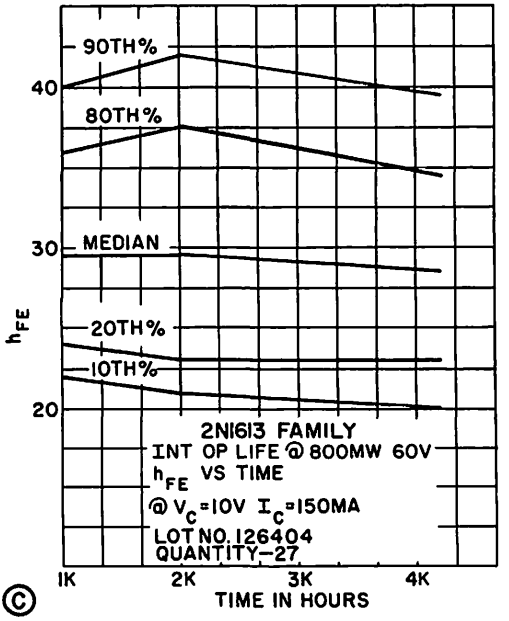
(Figure 18.12)

Graph A – As in most operating life tests at maximum rated power, this also displays a rapidly decreasing failure rate.

Graphs B & C – The only appreciable change in leakage current or current gain at full rated power out to more than 7000 hours is an increase in $I_{CBO}$ by the fringe of the distribution.






**RELIABILITY DATA FOR A SILICON DIFFUSED PLANAR PASSIVATED TRANSISTOR**

**Figure 18.12**

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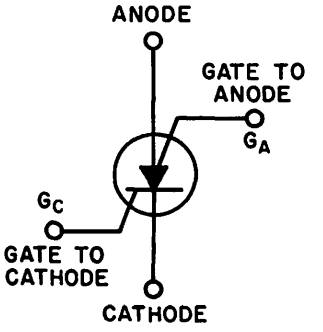
# SILICON CONTROLLED SWITCH

CHAPTER 19

## WHAT IS IT?

- silicon 4 layer PNPN structure
- all layers accessible
- TO-5 electrically isolated case
- military reliability
- industrial prices
- available in production quantities

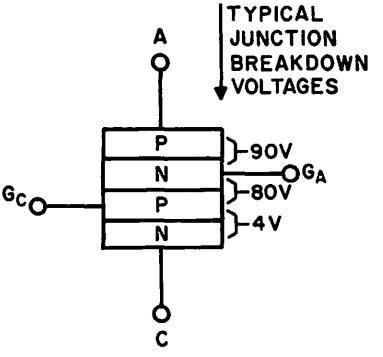


SYMBOL

## WHAT FUNCTIONS CAN IT PERFORM?

Depending on the characterization it can be used as

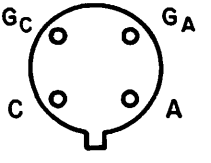
- extremely sensitive NPNP controlled switch (complement of SCR)
- extremely sensitive PNPN controlled switch (SCR configuration)
- NPN silicon transistor
- PNP silicon transistor
- N type negative resistance (Trigistor, Transwitch)
- S type negative resistance (Binistor)
- four layer diode (Shockley Diode)
- zener diode



STRUCTURE

## WHAT ARE ITS APPLICATIONS?

- time delay generator
- SCR trigger pulse generator
- tone generator
- pulse generator
- telemetry oscillator
- sensitive voltage level detector
- bistable memory element
- binary counter
- ring counter
- shift register
- relay driver
- indicator lamp driver
- low level SCR
- low level complementary SCR

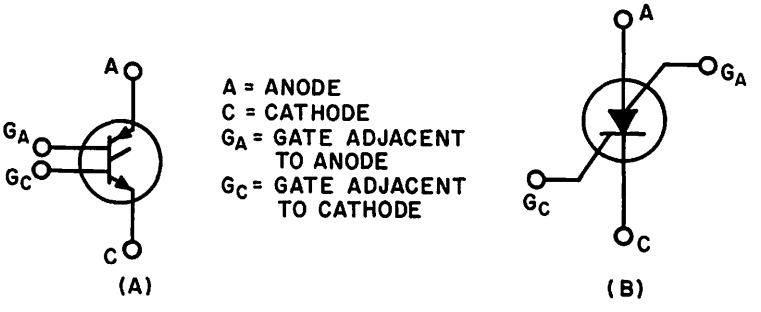


BASING — BOTTOM VIEW

## INTRODUCTION

The General Electric 3N58 series device (formerly ZJ93) is a silicon controlled switch (SCS) designed for use in industrial and military digital computer and control applications. It is a four layer (PNPN) device with all four layers accessible. It can therefore be used as a PNPN controlled switch, NPNP controlled switch, NPN transistor, PNP transistor, N type negative resistance device, S type negative resistance device (negative conductance), four layer diode, and zener diode. It is characterized specifically as a PNPN and a NPNP device with designations 3N58 and 3N59.

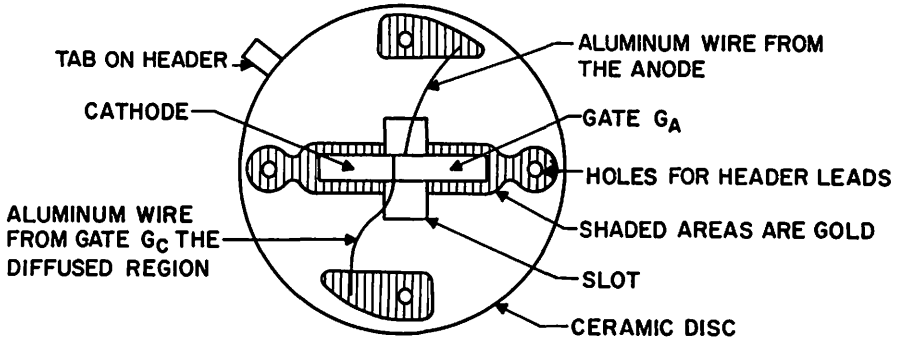
Its TO-5 isolated case package, extremely high firing sensitivity, and forty volt rating make it suitable for applications including sensitive voltage level detectors, bistable memory elements, binary counters, shift registers, ring counters, telemetry oscillators, time delay generators, pulse generators, tone generators, relay drivers, indicator lamp drivers, SCR trigger generators, low level SCR and low level complementary SCR. The IRE semiconductor symbol for this device is shown in Figure 19.1.




**SYMBOLS FOR SILICON CONTROLLED SWITCH**

**Figure 19.1**

This symbol offers a clear picture of the semiconductor structure of the device. In circuit applications, however, the alternate symbol suggested by current silicon controlled rectifier usage may be of help in visualizing the significance of the gates.



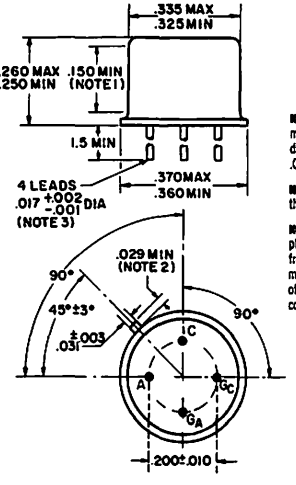

**METHOD OF CONSTRUCTION — TOP VIEW**

**Figure 19.2**

## CONSTRUCTION

The SCS is essentially an NPN diffused base transistor with a third junction to form a PNPN device. The transistor structure is a bar approximately 10 mils in cross section and 10 mils effective length. For mechanical strength, low thermal resistance, electrical case isolation, and manufacturing ease, the bar is mounted on a ceramic disc or fixed-bed mounting. This method of construction is shown in Figure 19.2 below. A wafer of non-porous ceramic material which has the same coefficient of thermal expansion as the pellet forms the base of the mechanical structure. Gold is deposited on the disc in four areas to form electrical contacts. Header wires projecting through holes in the disc are bonded to the disc with a gold-tin alloy. The transistor bar is mounted across a narrow slot in the disc with the diffused base region over the slot. The bar is alloyed into gold areas on either side of the slot. Aluminum wires alloyed into the bar make the remaining two connections. The aluminum wire to the diffused base forms the cathode gate ($G_c$). The other wire forms the anode (A) junction. Header leads are made of kovar with a coating of 24 carat gold of 0.04 mil minimum thickness.

To ensure stability with life all parts are outgassed prior to capping in a nitrogen atmosphere. Two gettering materials "molecular sieve" and fiber glass, used to absorb any possible outgassing materials after capping, are firmly held at the top of the cap. They absorb water vapor as well as many organic vapors. The case meets the TO-5 outline and has all leads electrically insulated from the case. The lead locations and packaged dimensions are shown in Figure 19.3.




**DIMENSIONS WITHIN JEDEC OUTLINE TO-5**

NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

NOTE 2: Measured from max. diameter of the actual device.

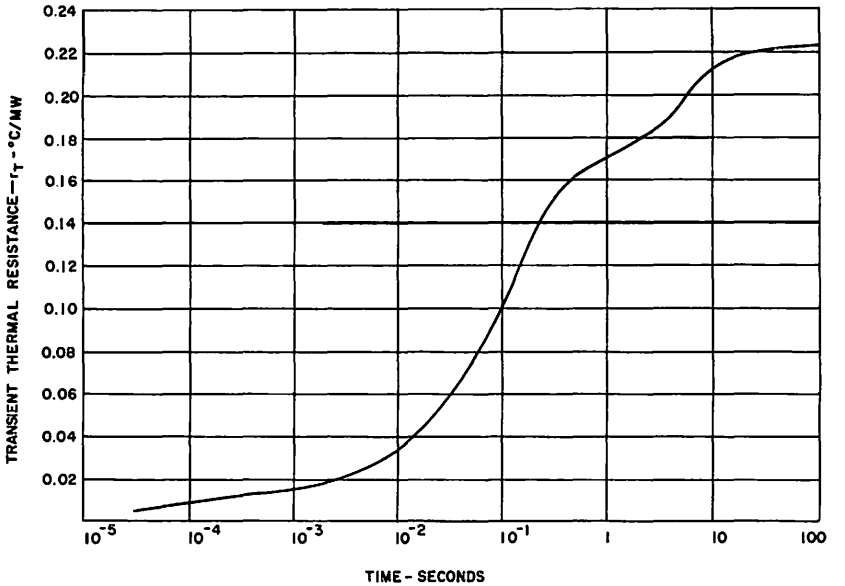
NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and .5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled.

**TO-5 PACKAGE DIMENSIONS**

**Figure 19.3**

## THERMAL CHARACTERISTICS

Since PNPN devices tend to turn on more readily at high temperatures the silicon control switch is characterized to remain non-conducting, i.e., "block" current at its maximum rated voltage while at its maximum rated junction temperature. Its dissipation rating is designed to avoid exceeding this maximum junction temperature. The transient thermal resistance curve in Figure 19.4 permits calculation of the maximum junction temperature for pulsed input power.




**TRANSIENT THERMAL RESISTANCE JUNCTION TO CASE — SCS 3N58 SERIES**

**Figure 19.4**

For single load pulses separated by more than 10 seconds the rise in junction temperature ($T_h$) is given by

$$T_h = P\, r_T$$

where $r_T$ is the transient thermal resistance at the time of the end of the pulse of power P. For example, for a 20 microsecond pulse of 1 watt power $T_h = (1000)\ (.005) = 5°C$.

For repetitive pulses of equal amplitude the maximum junction temperature can also be calculated from the transient thermal resistance. The method is covered in detail in the General Electric Silicon Controlled Rectifier Manual.* However, a conservative estimate of maximum junction temperature is given by

$$T_{J_{max}} = T_A + P\,\frac{t}{\tau}\,R_T + P\,r_T$$

where P is the pulse power, $T_A$ the ambient temperature, t the pulse width, $\tau$ the period between pulses, $R_T$ the steady state thermal resistance, and $r_T$ the transient thermal resistance at time t.

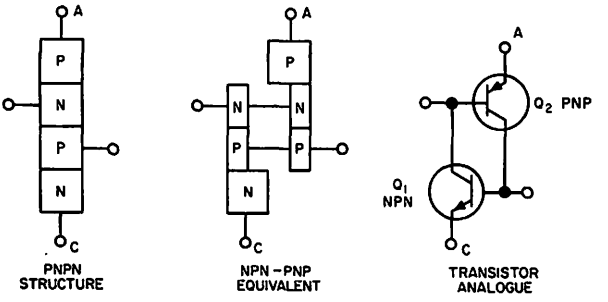
For pulses shorter than 20 microseconds the thermal mass of the junction controls heating. The junction thermal mass is $2 \times 10^{-6}$ joules per degree centigrade, i.e., $2 \times 10^{-6}$ watt-seconds will raise the junction 1°C. Illustrating this, a .1 $\mu$fd capacitor charged to 40 volts on discharging into the SCS will raise the junction temperature by

$$T_H = \frac{CV^2}{2} \cdot \frac{1}{2 \times 10^{-6}} = \frac{(.1)\ (1600)}{10^6\ (4)\ (10^{-6})} = 40°C.$$

## TWO TRANSISTOR ANALOGUE OF PNPN SWITCH

The two transistor analogue shown in Figure 19.5 is very useful in understanding the operation of PNPN structures such as the SCS.

*See Chapter 1 Reference List



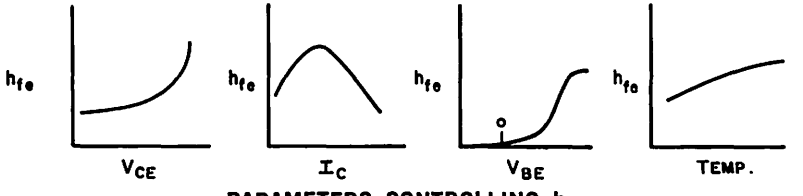

**TRANSISTOR ANALOGUE OF PNPN SWITCH**

**Figure 19.5**

The PNPN structure is considered to be equivalent to an NPN and PNP transistor interconnected in a positive feedback configuration. The specific characteristics of each junction can now be interpreted in transistor terms, taking advantage of the circuit theory developed for transistors. Transistor and SCS terminology will be used interchangeably as required.

When the anode is positive with respect to the cathode the center junction (corresponding to the transistor collectors) is reverse biased. In this case it can be shown that anode to cathode current ($I_{AC}$) is then given by $I_{AC} = \frac{I_{co}}{1 - h_{fe1} h_{fe2}}$ where $I_{co}$ is the leakage of the center junction and $h_{fe1}$ and $h_{fe2}$ refer to the gains of $Q_1$ the NPN transistor and $Q_2$ the PNP transistor respectively. When $h_{fe1} \cdot h_{fe2} < 1$, $I_{AC}$ is a relatively small current hence the PNPN is said to be "blocking."

When $h_{fe1} \cdot h_{fe2} = 1$ the loop gain is unity and $I_{AC}$ as defined, becomes infinite. In practice it increases to a value limited only by circuit impedance. At unity loop gain PNPN structures turn "on" at a speed determined by the effective frequency response of the two transistors. The condition $\alpha_1 + \alpha_2 = 1$ commonly used in PNPN literature is identical to $h_{fe1} \cdot h_{fe2} = 1$. Current gain $h_{fe}$ is a function of $V_{CE}$, $I_C$, $V_{BE}$ and temperature as shown in Figure 19.6. These variables, alone or in combination may be used to increase $h_{fe}$ sufficiently to achieve unity gain.

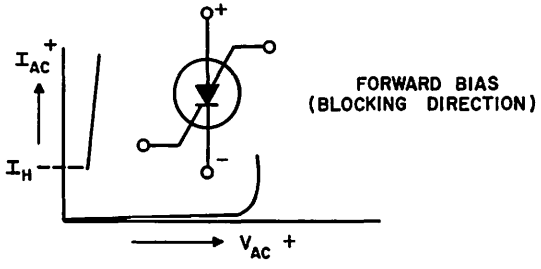



**PARAMETERS CONTROLLING $h_{fe}$**

**Figure 19.6**

The rise in $h_{fe}$ with $V_{CE}$ is the result of approaching the breakdown voltage of the collector junction. As $h_{fe}$ increases it causes $I_C$ to also increase. Therefore, raising the anode voltage near breakdown results in unity loop gain and the device turning on. The usual method of turning on the device is to increase $I_C$ by applying a base current to either transistor. In this manner the device may be turned on when the junction voltages are well below breakdown. It is also possible to turn on the device by apply-

ing forward bias voltage only. Theoretically, for a transistor, $I_c = h_{fe} I_{co}$ when the base current is zero. Therefore, $I_c$ increases from $I_{co}$ to $h_{fe} I_{co}$ as the emitter junction is forward biased. This latter value of $I_c$ may be adequate to yield unity loop gain in a PNPN device. Since $h_{fe}$ and $I_{co}$ both increase with temperature then the sensitivity to turn on increases with temperature. Anode to cathode characteristics for forward bias are as shown in Figure 19.7.

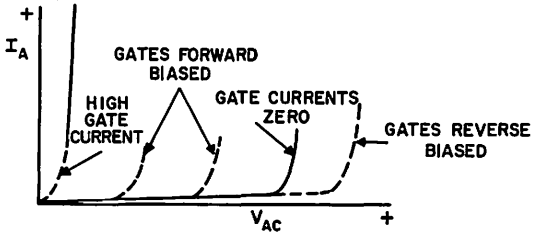



**ANODE TO CATHODE BLOCKING CHARACTERISTICS**

**Figure 19.7**

It is seen that only a small leakage current exists for low blocking voltages. As voltage is increased until it approaches the center junction breakdown, $h_{fe}$ increases due to its dependence on voltage. Unity loop gain is reached and $V_{AC}$ no longer increases. It does not drop, however, until the loop gain can be unity due to $h_{fe}$ dependence on current alone. As $I_A$ builds up to meet the above criteria $V_{AC}$ is essentially constant.

Unity gain may also exist with various combinations of $I_A$ and $V_{AC}$. This generates plateaus in the "negative resistance" region between the breakdown voltage and the forward conducting region, leading to partial switching if the chosen load line intersects a plateau. Partial switching is avoided by turning the device on by a gate input or by using a lower impedance load.




**BLOCKING CHARACTERISTICS**

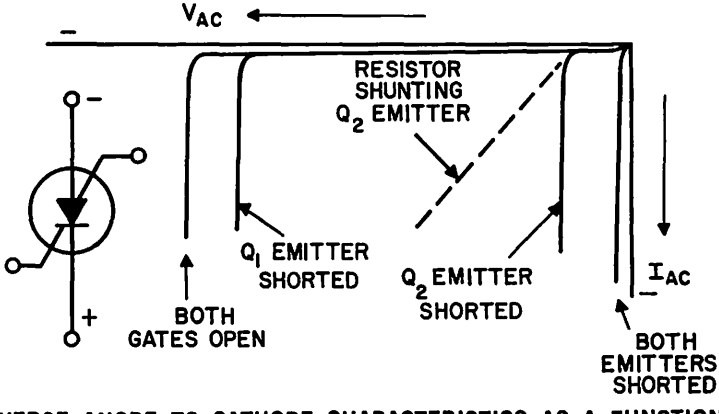
**Figure 19.8**

Reverse biasing the gates raises the collector junction breakdown. Applying forward bias to either or both emitter junctions lowers the breakdown voltage until in the limit the characteristic resembles that of a forward biased diode. Once turned on the PNPN switch stays on until the "holding current" is reached. At this current, loop gain falls below unity and the switch turns off.

To turn off the SCS, the anode current must be reduced below the holding current. This can be achieved either by actually reducing $I_A$ or by increasing $I_H$. The usual techniques for reducing $I_A$ include reverse biasing the anode, diverting $I_A$ by a shunt current path or incorporating the SCS in an under-damped tuned circuit.

To raise the holding current, loop gain is reduced by reverse biasing the gates. Because of the inherent regeneration in a PNPN device, reverse bias is not easily attained. In fact while the voltages seen on the device leads may show reverse bias, because of resistance in series with the leads, the junctions may remain forward biased. If, as is the case with the SCS, the PNP analogue transistor has much lower gain than the NPN, the SCS can be turned off by diverting only a fraction of the anode current through the NPN base lead ($G_K$). (For reasons discussed later this only applies to low anode currents.) On the other hand, very nearly the full anode current is required by $G_A$ to turn off the SCS.

When the anode is negative with respect to the cathode, the middle junction is forward biased; the other two junctions reverse biased. The reverse biased junctions will share the voltage on the basis of their breakdown voltages or leakage currents. Should one of these junctions be shunted by a resistor as is common in many biasing circuits, the full reverse voltage would be applied to the other junction. Figure 19.9 shows the breakdown voltages that can be expected under various conditions of emitter junction shunting.




**REVERSE ANODE TO CATHODE CHARACTERISTICS AS A FUNCTION OF GATE CIRCUIT**

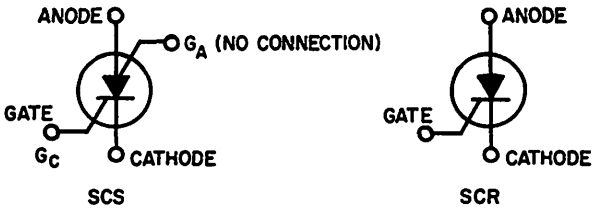
**Figure 19.9**

## GENERAL COMPARISON WITH OTHER SEMICONDUCTORS

The SCS can be used in some applications in place of four layer diodes, trigistors, transwitches, unijunction transistors, controlled rectifiers and binistors. Therefore the extensive literature on these devices is directly applicable to the SCS. Since the SCS may replace such a variety of devices, the importance of the designer's viewpoint is evident. That is, how he intuitively visualizes the mode of operation of the device, channels his thoughts into specific circuit configurations. With this in mind, the comparisons that follow are aimed at offering the greatest insight into the similarities between these devices without dwelling on minor specification differences.

## COMPARISON WITH SILICON CONTROLLED RECTIFIER

The 3N58 is characterized essentially as a sensitive SCR. Figure 19.10 shows the symbol equivalence.




**CORRESPONDENCE BETWEEN SCS AND SCR SYMBOLS**

**Figure 19.10**

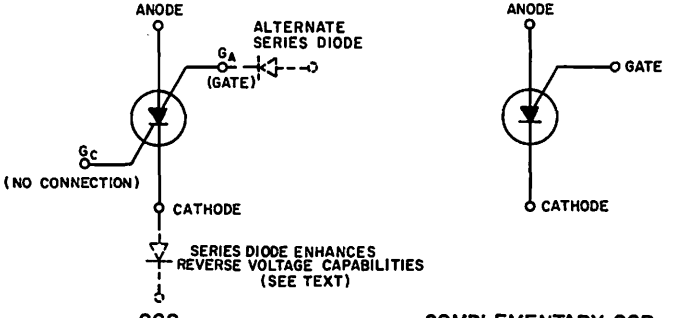
The SCS, being designed for low level logic and general industrial control and computer switching, is characterized by low leakage current, anode currents below 0.5 amperes, voltage ratings below 60 volts, low holding currents, sensitive well defined firing conditions and small physical size. Within these constraints both devices can perform the same functions.

Some SCR applications apply a reverse bias to the gate junction. Generally the gate must be clamped to avoid excessive dissipation. The SCS maximum gate current ratings apply to the reverse bias on the gates as well as forward bias to fire. The SCS firing sensitivity permits a high resistance to be connected in series with the gate to minimize dissipation without the necessity for clamping diodes.

A 40 volt reverse bias can be applied to $G_A$. To take advantage of this the SCR circuitry can be adapted to a "complementary" configuration as suggested in the next section.

## COMPARISON WITH COMPLEMENTARY SCR

A PNPN structure always blocks in one direction only, i.e., when the P end is biased positive. The complementary SCR therefore also blocks in the same direction as the conventional SCR. It differs from a conventional SCR in that the gate is adjacent to the anode and fires the SCR when a negative pulse is applied to it.




**CORRESPONDENCE BETWEEN SCS AND COMPLEMENTARY SCR SYMBOLS**

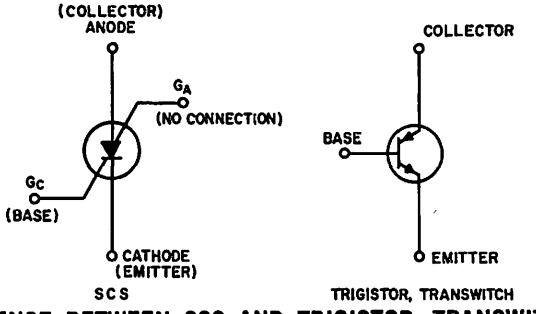
**Figure 19.11**

An SCR is generally required to withstand reverse voltage. When the SCS is reverse biased the cathode junction breaks down at about four volts. Higher reverse voltages are therefore blocked by the anode junction. If a DC gate signal return exists between

$G_A$ and A, it is in parallel with the anode junction and appears as a reverse leakage current. This is shown in Figure 19.9. This leakage current through the load can be avoided by connecting a diode in series with the cathode as shown in Figure 19.11. An alternate method is to connect a diode in series with the gate as shown. In this case the gate can be used to turn off the SCS while $G_C$ is used to turn it on.

## COMPARISON WITH TRIGISTOR, TRANSWITCH

The trigistor and transwitch are similar in that they are PNPN devices capable of stable blocking or conducting states without a maintaining input being required. They can be switched to either state by an appropriate input. In SCR terminology the SCR can be turned on and off from the gate. A positive pulse turns it on; a negative, off.



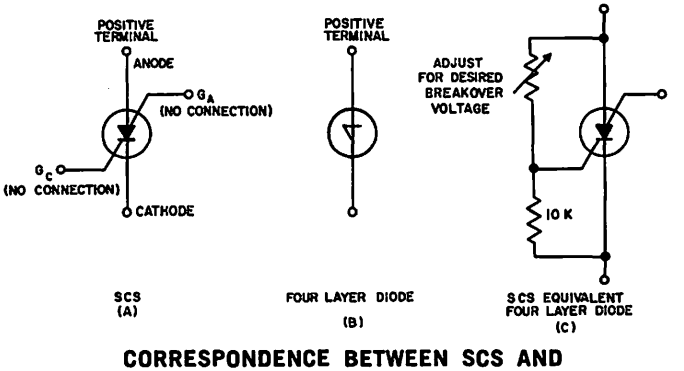

**CORRESPONDENCE BETWEEN SCS AND TRIGISTOR, TRANSWITCH SYMBOLS**

**Figure 19.12**

The SCS can also be turned on and off by gates as indicated in Figure 19.12 above. $G_C$ will only turn off anode currents below about 4 ma. For anode current up to 50 ma the load may be connected to cathode and $G_A$ used for turn off.

## COMPARISON WITH FOUR LAYER DIODE

The four layer diode can be considered to be an SCS with no gate leads as shown in Figure 19.13. The SCS, however, is not characterized in narrow ranges of forward breakover voltage.



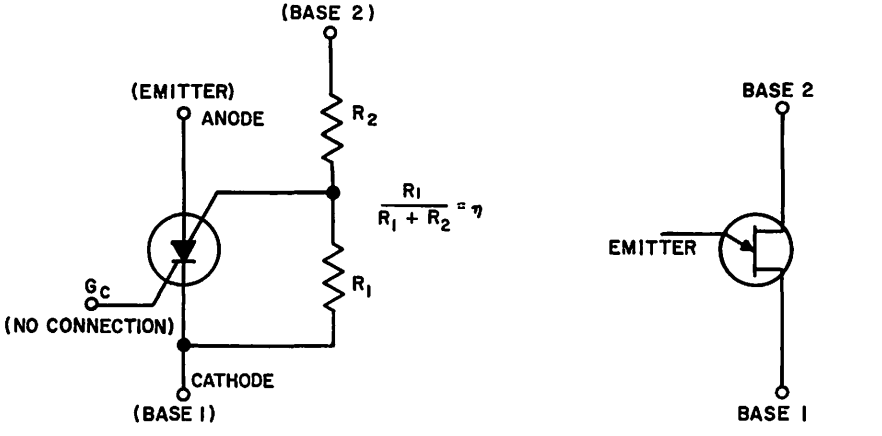

**CORRESPONDENCE BETWEEN SCS AND FOUR LAYER DIODE**

**Figure 19.13**

A diode of any desired breakdown voltage within the ratings of the SCR can be synthesized as shown in Figure 19.13(c) by adding a voltage divider across the SCS. When the anode voltage reaches the desired breakover voltage the divider is arranged to supply the required gate firing input. Better stability with temperature and voltage transients will result from returning the cathode end of the divider to a negative bias voltage. In some applications it may be more convenient to connect the divider to $G_A$ rather than $G_C$.

## COMPARISON WITH UNIJUNCTION TRANSISTOR

Physically the two components are different. However, both devices are capable of generating negative resistances. The unijunction transistor is uniquely suitable for timing and oscillatory applications based on RC charging networks. It uniquely combines very low leakage current, low current to fire, circuit variable "breakover voltage" and self-compensation for temperature or power supply variations. Its controlled high holding current makes it suitable for delivering high energy pulses for SCR firing circuits. The SCS on the other hand has a very low holding current making it more suitable for low power bistable circuits. It can also be used for SCR firing provided the load is AC coupled or some other precautions are taken to turn the SCS off. Figure 19.14 shows the voltage divider necessary to synthesize the unijunction transistor.

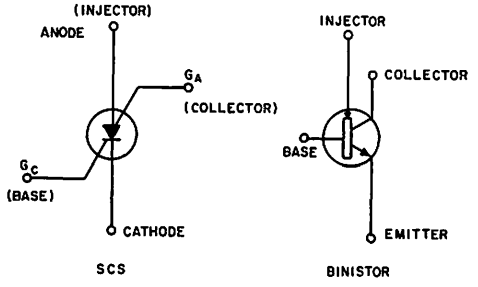



**CORRESPONDENCE BETWEEN SCS AND UNIJUNCTION TRANSISTOR**

**Figure 19.14**

## COMPARISON WITH BINISTOR

The binistor is very similar to the SCS in that both devices have leads connected to all four semiconductor layers. The binistor is characterized specifically as a transistor with an extra control lead. While this characterization leads to many useful and novel circuits it does not suggest to the circuit designer the SCR, trigistor, transwitch and unijunction transistor applications of which the device is capable. Figure 19.15 shows the one-to-one correspondence between the binistor and SCS.




**CORRESPONDENCE BETWEEN SCS AND BINISTOR**

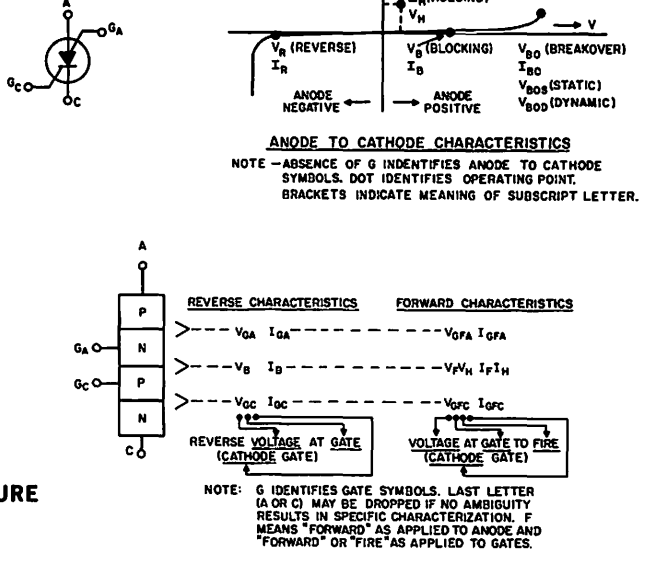
**Figure 19.15**

In general, circuits designed for the binistor will operate with the SCS without any circuit modification. SCS circuits, however, are capable of higher voltage, higher dissipation operation.

## DEFINITION OF TERMS USED IN SCS SPECIFICATIONS

### BASIS FOR NOMENCLATURE

PNPN devices available at present do not have a common nomenclature. In part, this is due to their different construction ranging from the two terminal four layer diode to the four terminal binistor. SCR nomenclature on the other hand reflects the surge problems associated with rectifier applications. SCS nomenclature permits the reverse characteristics of all three junctions to be specified. The anode forward characteristic and gate firing characteristics can also be specified fully. Figure 19.16 illustrates the principles used in assigning symbols.




**SCS NOMENCLATURE**

**Figure 19.16**

## MAXIMUM RATINGS

*Anode Blocking Voltage* – With the anode forward biased, the anode blocking voltage is the minimum static voltage at which the SCS will remain non-conducting. It is the maximum voltage at which the SCS leakage current will not exceed a specified value indicated in the anode blocking current rating.

*Anode Reverse Voltage* – With the anode reverse biased the anode reverse voltage is the maximum voltage at which the SCS leakage current will not exceed a specified value. The gates are generally biased as in the Anode Blocking Voltage Test. Where the biasing resistors mask the true voltage breakdown of the junctions additional data is supplied.

*Gate to Cathode Reverse Voltage* – The maximum voltage at which the gate leakage current will not exceed a specified current. All other leads are open circuited.

*Continuous D.C. Forward Current* – The forward current is the maximum anode to cathode current when the device is turned on and is primarily limited by the dissipation rating of the SCS. Gate current ratings are defined separately. This current can be exceeded as is implied by the peak current forward current rating if precautions are taken to limit the maximum junction temperature.

*Peak Recurrent Forward Current* – Maximum forward anode to cathode current when the device is on with specified time and temperature conditions. Peak current is recurrent at 400 cps unless otherwise specified. For shorter duration peak currents such as are characteristic of capacitor discharge the thermal mass rating determines the permissible peak current.

*Peak Gate Current* – Maximum gate current with same time temperature and recurrence as peak recurrent forward current. The same rating applies whether the gate is forward or reverse biased.

*Average Gate Current* – Average gate current rating applies to both forward and reverse gate current and is limited primarily by dissipation.

*Operating Temperature Range* – The operating temperature range is the range in which the SCS will exhibit blocking characteristics under specified biasing conditions. Life tests are used to ensure no failure mechanisms or degradation characteristics over this temperature range.

*Storage Temperature Range* – Storage temperature range defines the temperature range in which life tests have shown no failure mechanisms or degradation characteristics. The SCS will not necessarily exhibit its blocking characteristic over the whole range.

*Dissipation* – The maximum total power dissipation in an ambient of 25°C. The rating applies to operation with free air cooling unless otherwise specified.

## ELECTRICAL CHARACTERISTICS

*Anode Blocking Current ($I_B$)* – $I_B$ is the anode current in the forward biased anode while blocking voltage at a specified junction temperature and specific gate biases.

*Gate Reverse Current ($I_G$ $I_{GC}$ $I_{GA}$)* – $I_G$ is the leakage current in a reverse biased gate with other electrodes connected as specified. $I_{GC}$ is the leakage of the cathode junction; $I_{GA}$ of the anode.

*Gate Current to Fire ($I_{GF}$ $I_{GFC}$ $I_{GFA}$)* – $I_{GF}$ is the gate current required in the direction of forward gate bias to turn on a blocking anode under specified circuit conditions.

*Gate Voltage to Fire ($V_{GF}$ $V_{GFC}$ $V_{GFA}$)* – $V_{GF}$ is the gate voltage at which the SCS turns on under specified circuit conditions.

*Anode Forward Voltage ($V_F$)* – Voltage from anode to cathode after SCS has fired with specified gate biases and temperature.

*Anode Holding Current ($I_H$)* – $I_H$ is the minimum anode current at which SCS will not turn off under specified circuit conditions and temperature.

### DEFINITIONS

*Fire* – Undergo the transition from forward blocking to saturation. This is the "turning on"of the SCS.

*Static Voltage* – A voltage which is applied gradually. Specifically a voltage applied at a rate that if the rate were doubled there would be no change in the measurement under test.

*Dynamic Voltage* – A voltage applied rapidly enough to induce changes in measurements made under static conditions. Specifically, the breakover voltage is a function of the rate of rise of anode voltage.

## GATE CHARACTERISTICS

The SCS has two gates: $G_C$ and $G_A$. $G_C$ is the gate adjacent to the cathode and $G_A$ is the gate adjacent to the anode. Both of these are effective in firing the SCS, therefore it is essential that the conditions of both be specified in defining firing sensitivity.

### $G_C$ CHARACTERISTICS

Since the SCS is fabricated from an NPN transistor structure, $G_C$ characteristics are identical to common emitter input characteristics. The characteristics are shown in Figure 19.17.

REVERSE BREAKDOWN VOLTAGE 4 TO 6V
$r_b'$ AT $I_G$ = 50μA = 1000Ω
$r_b'$ AT $I_G$ = 1 MA = 50Ω
$r_b'$ AT $I_G$ = -1MA = 5K
$dV_{GFC}/dT$ = -2MV/ °C
TURN OFF GAIN = 2 TO 6

**$G_C$ CHARACTERISTICS**
**Figure 19.17**

REVERSE BREAKDOWN VOLTAGE 70 TO 120
$r_b'$ AT $I_G$ = 10MA =40Ω
$r_b'$ AT $I_G$ = 1 MA =200Ω
$r_b'$ AT $I_G$ = -10MA =200Ω
TURN OFF GAIN = 1

**$G_A$ CHARACTERISTICS**
**Figure 19.18**

When $G_C$ is forward biased $r_b'$ shows the variation common to transistors. Minority current flow modulates the base resistance decreasing it at high currents. When $G_C$ is reverse biased modulation ceases and $r_b'$ increases. The reverse current out of $G_C$ is limited to about 1 ma before the gate is clamped to the cathode via the 5 volt emitter breakdown voltage. This reverse current will turn off the SCS when $I_A < 2$ ma and $G_A$ is open, or $I_A < 4$ ma when $G_A$ is shorted to A.

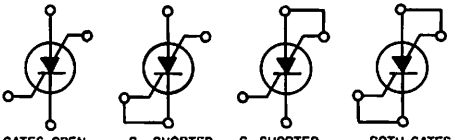
### $G_A$ CHARACTERISTICS

$G_A$ is the collector of the NPN transistor and therefore has a series "saturation" resistance. Its characteristics are shown in Figure 19.18.

While reverse biasing $G_A$ readily turns off anode currents of 50 ma, turn off gain is unity. The 200Ω effective series resistance requires approximately 10 volts of reverse bias to develop a 50 ma gate current. The turn off gain is essentially unaffected by opening or shorting $G_C$.

### FIRING CHARACTERISTICS

Four limit combinations of gate biasing are possible as shown in Figure 19.19.

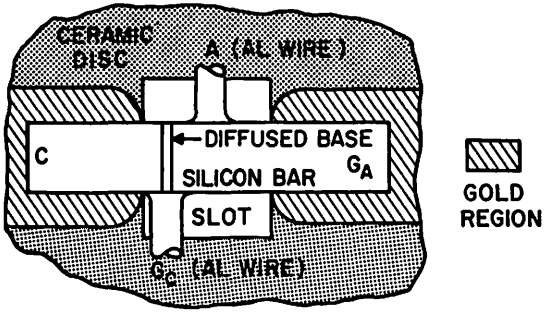



| | | | | |
|---|---|---|---|---|
| BREAKOVER VOLTAGE $V_{BO}$ VOLTS | 0 TO 20 | 70 | 50 | 80 |
| REVERSE VOLTAGE $V_R$ VOLTS | 80 | 80 | 4 | 0.5 |
| $I_H$ MA | 0 | 0.5 TO 1 | 2 TO 3 | 2 TO 3 |
| $I_{BO}$ MA (TO FIRE) | 0 | 0.5 | 2 | 4 |
| $I_{GFC}$ MA (TO FIRE) | −TO 1μA | | 10 TO 60 μA | |
| $V_{GFC}$ VOLTS (TO FIRE) | 0.4 TO 0.6 | | 0.5 TO 0.8 | |
| $I_{GFA}$ MA (TO FIRE) | 0 TO 8μA | 0.2 TO 1.0 MA | | |
| $V_{GFA}$ VOLTS (TO FIRE) | 0.4 TO 0.6 | 0.6 TO 0.9 | | |

**TYPICAL ANODE CHARACTERISTICS FOR SPECIAL GATE BIASES**

**Figure 19.19**

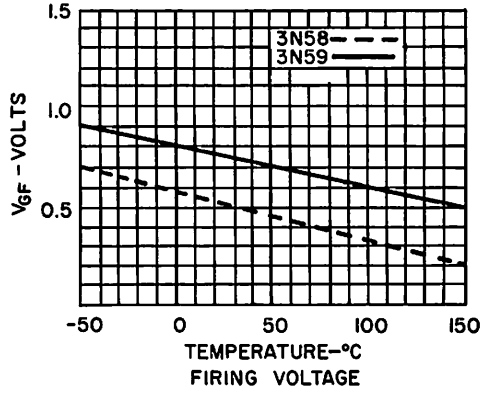
It is significant that shorting out an emitter junction does not destroy the PNPN characteristic. Figure 19.20 shows the location of $G_C$ and A wires on opposite sides of the bar. Anode current can readily forward bias $G_C$ due to the cross-base resistance. Similarly $G_A$ can be forward biased due to the ohmic "saturation resistance" inherent in this structure.

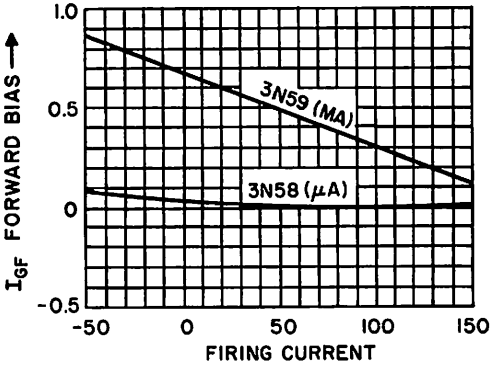



**EXPANDED VIEW OF SCS STRUCTURE**

**Figure 19.20**

The shorted configurations are useful in decreasing sensitivity in the presence of noise, high temperature, or dV/dt problems. SCS type 3N58 is essentially a "gates open" characterization. The extremely low $I_{CO}$ of the center junction gives a 40 volt minimum blocking voltage at 150°C while simultaneously offering very high sensitivity. A negligible gate current is required to fire. Typically, forward biasing $G_C$ is sufficient. SCS type 3N59 is characterized with $G_C$ shorted. This configuration offers high blocking and reverse voltage. Sensitivity is decreased sufficiently that a forward bias gate current is always required to fire.




**TYPICAL GATE FIRING CHARACTERISTICS VS. TEMPERATURE**

**Figure 19.21**

Figure 19.21 indicates the change in firing characteristics with temperature. The firing voltage decreases with temperature as can be expected from the transistor analogue analysis. The 3N59 firing current also decreases with temperature showing the increased tendency to turn on at high temperatures. The typical 3N58 fires with less than 0.1 μa input current over the whole range of temperature.

### TURN-OFF CHARACTERISTICS

As was indicated in discussing gate characteristics $I_{GC}$ reverse is limited to approximately 1 ma. Only currents in the range of 4 ma can be turned off with $G_C$. Turn off gain is about 2.

$G_A$ can turn off anode currents of 50 ma but the required gate voltage may be impractical at this current level. Turn off gain is approximately 1.

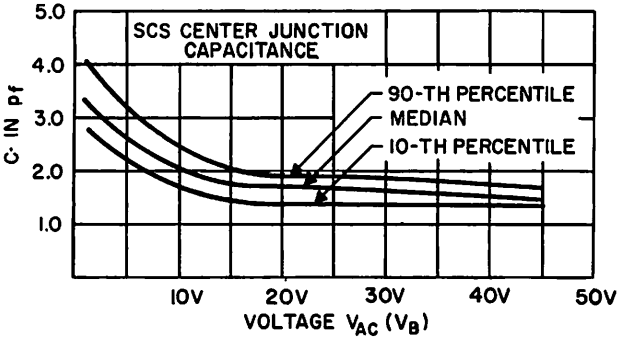
## ANODE TO CATHODE CHARACTERISTICS

Some anode to cathode characteristics or simply "anode characteristics" depend strongly on gate biasing. These have been discussed in the gate characteristics section to a large extent. Other anode characteristics such as the forward conducting voltage,

the holding current, and reverse leakage are relatively independent of gate biasing. The dV/dt or rate-of-rise of anode voltage problem, speed of turn-on, and recovery time during turn-off will also be discussed in this section.

## RATE EFFECT — dV/dt

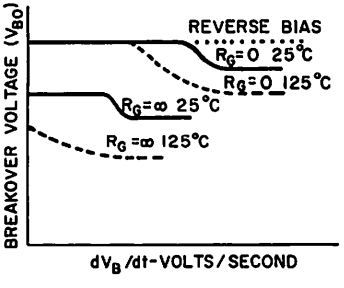
When anode blocking voltage is applied the capacitance of the middle junction becomes charged. If the voltage is applied slowly the charging current is small and can be ignored. If the anode voltage is applied rapidly, the charging current, as it flows through the emitter junctions, may raise $h_{fe}$ sufficiently to cause turn-on. Figure 19.22 indicates the middle junction capacitance is under 5 picofarads.




**CENTER JUNCTION CAPACITANCE**

**Figure 19.22**

Another way of looking at this problem is to consider the equivalent analogue transistors as being charge controlled devices. If the input charge is supplied at a rate slow compared to the recombination time of the transistors, the SCS will block. If it is supplied rapidly the transistors will only turn-on if the charge supplied is comparable to the charge required to turn them on. The latter charge is determined by the frequency response of the transistors.




**TYPICAL DYNAMIC BREAKOVER CHARACTERISTICS**

**Figure 19.23**

Figure 19.23 illustrates typical SCS behavior. At "static" voltages the forward breakover voltage is a function of gate biasing resistance. As dV/dt is increased the breakover voltage drops to a plateau determined by the charge requirements discussed in the previous paragraph. The gate resistor shunts some of the charge around the

emitter junction increasing its tolerance to dV/dt. At high temperatures the device is more sensitive therefore the dV/dt charge introduced is more effective in lowering the breakover voltage. The typical data in Figure 19.24 illustrates the above facts. The breakover voltage shown is the plateau value using a 1 nanosecond risetime voltage source.

| MINIMUM DYNAMIC BREAKOVER VOLTAGE IN | |
|---|---|
| −3N58 CONFIGURATION | 13 V |
| −3N59 CONFIGURATION | 35 V |
| −3N58 CONFIGURATION WITH $V_{GC} = -1V$ | 50V |
| −3N59 CONFIGURATION WITH $V_{GA} = +1V$ | 80V |
| STATIC BREAKOVER VOLTAGE | 80V |

**TYPICAL DYNAMIC BREAKOVER VOLTAGE CHARACTERISTICS AT 25°C**

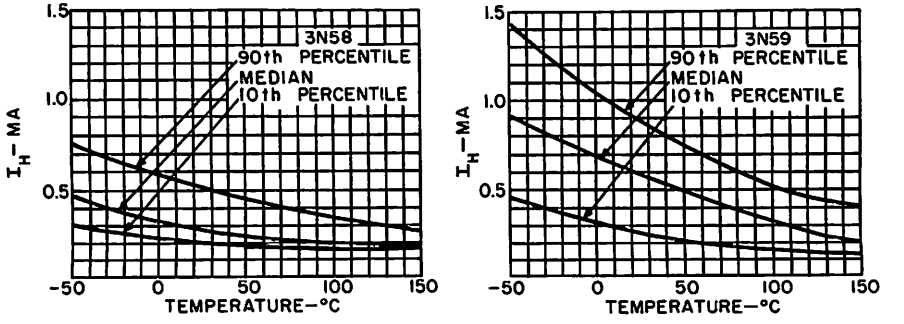
**Figure 19.24**

## BREAKOVER VOLTAGE

The maximum breakover voltage is the breakdown voltage of the center junction. Gate biasing and dV/dt invariably lowers this voltage. The breakdown voltage increases with rising temperature but is within 10% of its 25°C value from −65°C to +150°C.

## HOLDING CURRENT

Figure 19.25 shows the variation of holding current with temperature. The existence of $I_H$ at 150°C indicates the device is still able to block in the forward direction.

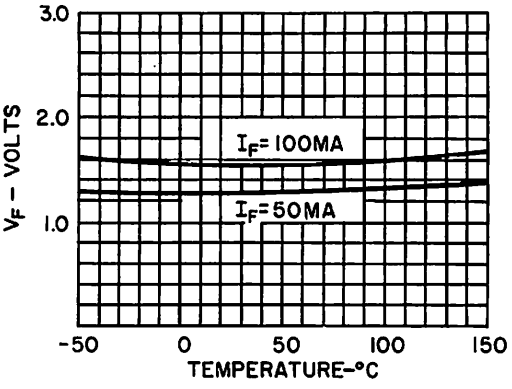



**HOLDING CURRENT $I_H$ VS. TEMPERATURE**

**Figure 19.25**

## FORWARD VOLTAGE

The forward voltage is relatively insensitive to temperature as shown in Figure 19.26. In calculating dissipation at high peak currents a conservative approximation for $V_F$ is $V_F = 1.1 + 5\ I_A$.




**FORWARD CHARACTERISTICS VS. TEMPERATURE**

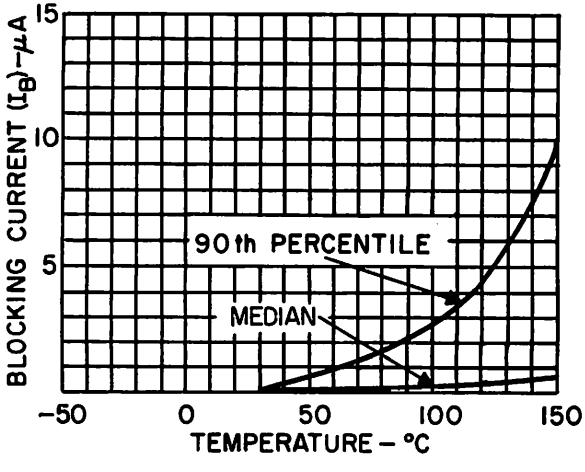
**Figure 19.26**

### REVERSE LEAKAGE CURRENT

At 25°C and rated voltage the leakage current is typically below 1 nanoampere and never exceeds 0.1 microampere. At 150°C essentially all units still have under 1 microampere leakage.

### BLOCKING LEAKAGE CURRENT

The leakage current in the forward or blocking direction can be higher. At 25°C and rated voltage it is essentially identical to the reverse leakage. As Figure 19.27 shows, at 150°C leakage currents are typically 0.5 microamperes.

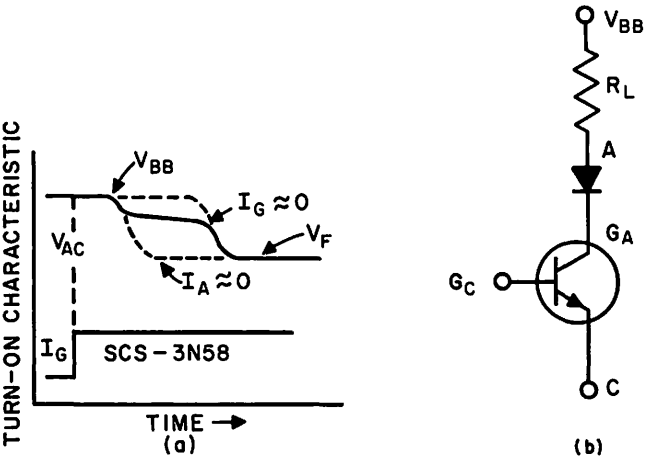



**BLOCKING CURRENT VS. TEMPERATURE**

**Figure 19.27**

### TURN-ON TIME

While $f_{ab}$ is approximately 30 mcs for the effective NPN transistor, the PNP is significantly slower, $f_{ab}$ being about 1 mc. Delay and rise time of anode current depend both on the gate and load currents. Figure 19.28 shows typical waveforms seen as the currents are varied.




CIRCUIT DEPENDENCE OF TURN-ON TRANSIENT

**Figure 19.28**

At low anode currents and high gate currents the SCS equivalent circuit is an NPN transistor with its collector coupled to the load by a diode as shown in Figure 19.28(b). The fast response time of the NPN drives it into saturation before the PNP transistor becomes effective regeneratively. A gate current barely adequate to turn on the SCS will result in a long delay time prior to a rapid turn on. For intermediate gate and load currents the 3N58 may exhibit partial turn on followed by rapid regenerate turn on.

The 3N59 is fired by turning on the PNP section. Since it is inherently slow a large gate current is necessary to minimize delay before firing. However, once the PNP section becomes active, loop gain increases rapidly resulting in a turn-on time of less than 20 nanoseconds. Figure 19.29 tabulates turn-on time to final load current for the 3N58 as a function of load current, gate current and temperature.

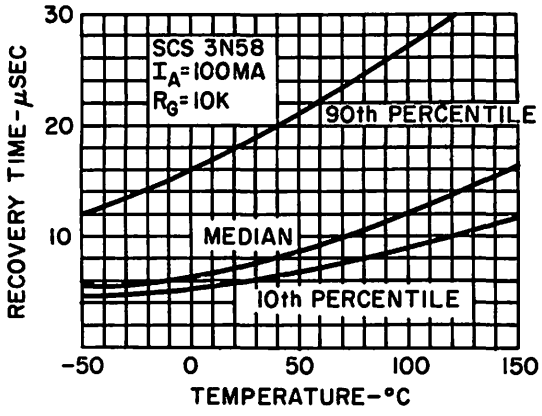
| | GATE CURRENT = 20μ A | | | GATE CURRENT = 100μ A | | |
|---|---|---|---|---|---|---|
| | LOAD CURRENT MA | | | LOAD CURRENT MA | | |
| | 1 | 10 | 100 | 1 | 10 | 100 |
| 25 °C | 2.1 | 1.8 | 1.8 | 0.7 | 0.7 | 0.8 |
| 125 °C | 1.7 | 1.6 | 1.7 | 0.7 | 0.7 | 0.8 |

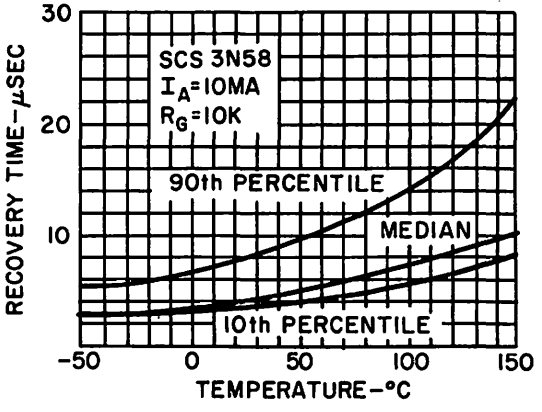
TURN-ON TIME OF 3N58 (MICROSECONDS)

**Figure 19.29**

RECOVERY TIME

Recovery time has been measured as a function of anode current and temperature. Recovery time increases with both anode current and temperature as shown in Figure 19.30. There is no simple way to substantially speed up recovery time, consequently the maximum speed of the SCS is limited to about 100 kcs.


30
20
10
RECOVERY TIME-μSEC
SCS 3N58
$I_A$=100MA
$R_G$=10K
90th PERCENTILE
MEDIAN
10th PERCENTILE
-50
0
50
100
150
TEMPERATURE-°C


30
20
10
RECOVERY TIME-μSEC
SCS 3N58
$I_A$=10MA
$R_G$=10K
90th PERCENTILE
MEDIAN
10th PERCENTILE
-50
0
50
100
150
TEMPERATURE-°C

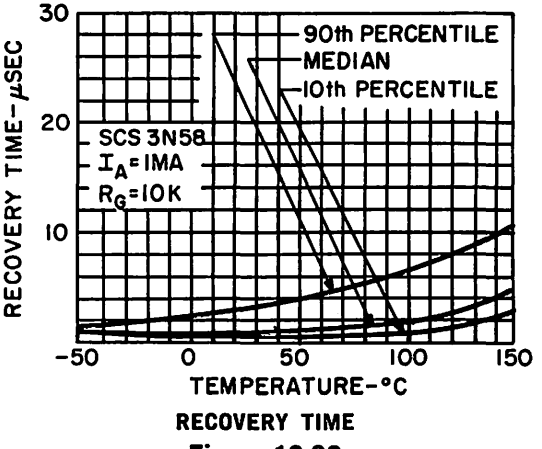

30
20
10
RECOVERY TIME-μSEC
90th PERCENTILE
MEDIAN
10th PERCENTILE
SCS 3N58
$I_A$=1MA
$R_G$=10K
-50
0
50
100
150
TEMPERATURE-°C
RECOVERY TIME

**Figure 19.30**

## MEASUREMENT OF ELECTRICAL CHARACTERISTICS

The test conditions given in defining and specifying the electrical characteristics suggest appropriate test circuits. It is possible, however, to perform semi-quantitative measurements on the Tektronix 575 Curve Tracer rather than construct the special test circuits. In particular the holding current, breakover voltage, forward voltage drop, gate voltage and current, and junction breakdown voltages can be measured in this manner. The appropriate control settings on the Tektronix 575 and the resulting typical traces are discussed below.

The remaining electrical characteristics should be measured with special circuits in order to obtain the necessary accuracy. For example, leakage currents are too low in value to obtain desired accuracy on the Tektronix 575. Thus a Keithley ammeter and associated circuitry may be used.

### MEASUREMENTS ON TEKTRONIX 575

The control settings to measure the various characteristics on the Tektronix 575 are given in Figure 19.31. These suggested settings should be suitable for most units at room temperature. Typical waveforms corresponding to these settings are shown in Figure 19.32.

TEKTRONIX 575 SETTINGS FOR SCS ELECTRICAL TESTS

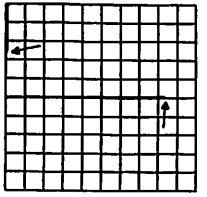
| UNIT | TEST | TEST SOCKET CONNECTIONS | | | COLLECTOR SWEEP | | | BASE STEP GENERATOR | | | | SENSITIVITY | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | COLLECTOR | BASE | EMITTER | POLARITY | LOAD RESISTANCE | VOLTAGE RANGE | SERIES RESISTANCE | POLARITY | STEP SELECTOR | STEP ZERO | VERTICAL MA./DIV | HORIZONTAL VOLTS/DIV |
| 3N58 | $I_H/V_B$ | A | $G_C$ | C | + | 100K | 0-200 | 10K | − | OFF | | 0.1 | 10 |
| | $V_R$ | A | $G_C$ | C | − | 100K | 0-200 | 10K | − | OFF | | 0.01 | 10 |
| | $V_{GC}$ | $G_C$ | NO CONN. | C | − | 2K | 0-20 | | | | | 0.01 | 1.0 |
| | $V_F$ | A | $G_C$ | C | + | 1K | 0-200 | 10K | + | .002 | | 10 | 0.2 |
| | $I_{GF}/V_{GF}$ | $G_C$ | A | C | + | 1K | 0-20 | 10K | + | 10 | FULL CLOCK-WISE | 0.01 | 0.1 |
| 3N59 | $I_H/V_B$ | $G_C$−C | $G_A$ | A | − | 100K | 0-200 | 10K | − | OFF | | 0.2 | 10 |
| | $V_R$ | $G_C$−C | $G_A$ | A | + | 100K | 0-200 | 10K | − | OFF | | 0.01 | 10 |
| | $V_{GA}$ | $G_A$ | NO CONN. | A | + | 100K | 0-200 | | | | | 0.01 | 10 |
| | $V_F$ | $G_C$−C | $G_A$ | A | − | 1K | 0-200 | 10K | − | 0.2 | | 10 | 0.2 |
| | $I_{GF}/V_{GF}$ | $G_A$ | $G_C$−C | A | − | 1K | 0-20 | 10K | − | 10 | FULL CLOCK-WISE | 0.5 | 0.2 |

**Figure 19.31**

**WAVEFORMS FOR $I_H$**

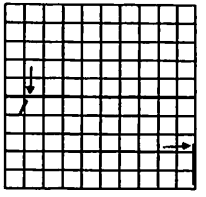
SCS – 3N58
VERTICAL SCALE – 0.1 MA / DIV
(a) HORIZONTAL SCALE – 10 VOLTS / DIV

$V_{BO}$ = 82 V
$I_H$ = 0.24 MA



SCS – 3N59
VERTICAL SCALE – 0.2 MA / DIV
(b) HORIZONTAL SCALE – 10 VOLTS / DIA

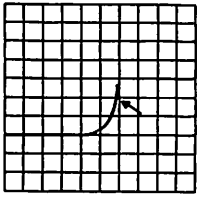
$V_{BO}$ = 88 V
$I_H$ = 0.48 MA



**WAVEFORM FOR $V_{GC}$**

SCS – 3N58
VETRICAL SCALE – 0.01 MA / DIV
(c) HORIZONTAL SCALE – 1.0 V / DIV

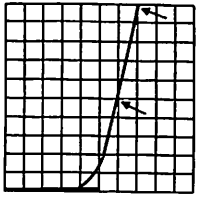
$V_{GC}$ = 5.9 VOLT
(READING AT $I_{GC}$ = 20 μA)



**WAVEFORM FOR $V_F$**

SCS – 3N58
VERTICAL SCALE – 10 MA / DIV
(d) HORIZONTAL SCALE – 0.2 V / DIV

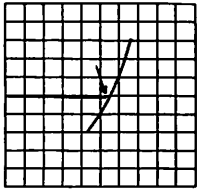
$V_F$ ($I_F$ = 50 MA) = 1.2 V
$V_F$ ($I_F$ = 100 MA) = 1.4 V



**WAVEFORM FOR $V_{GF}$ & $I_{GF}$**

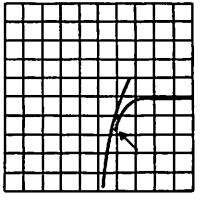
SCS – 3N58
VERTICAL SCALE – 0.01 MA / DIV
(e) HORIZONTAL SCALE – 0.1 V / DIV

$V_{GF}$ = 0.52 V
$I_{GF}$ = 0.0 MA



SCS – 3N59
VETRICAL SCALE – 0.5 MA / DIV
(f) HORIZONTAL SCALE – 0.2 V / DIV

$V_{GF}$ = 0.8 V
$I_{GF}$ = 0.8 MA

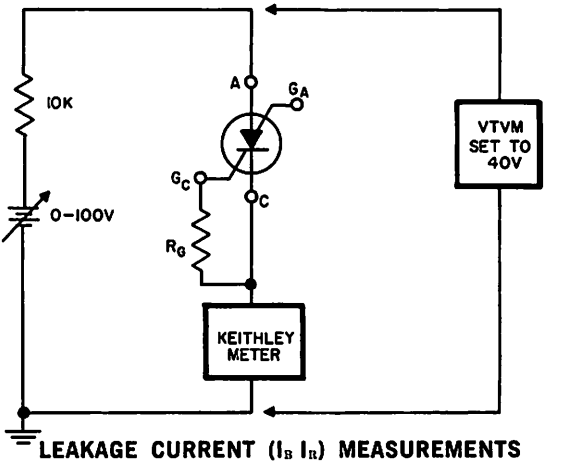


**WAVEFORMS FOR ELECTRICAL TESTS ON TEKTRONIX 575 CRO**

**Figure 19.32**

## LEAKAGE CURRENT MEASUREMENTS

The fundamental circuit for making leakage current measurements is shown in Figure 19.33. In particular the case of blocking current measurement is illustrated. One simply adjusts the power supply until the VTVM reads 40 volts. The voltage must be increased slowly to 40 volts to avoid firing the unit in the blocking condition. For the same reason one may wish to set the meter initially in the "short-circuit" position since only the 10K resistor limits the load current for the "on" condition.



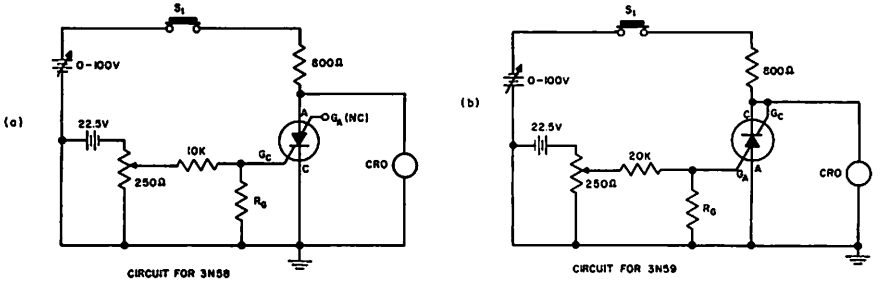

**LEAKAGE CURRENT ($I_B$ $I_R$) MEASUREMENTS**

**Figure 19.33**

For measurements on the 13A1 $R_G = 10K$. For the 3N59 unit $R_G = 0$. To measure the reverse leakage current simply reverse the battery polarity from that shown in the circuit.

## DYNAMIC BREAKDOWN VOLTAGE MEASUREMENTS

For these measurements a step voltage input with 800 Ω impedance is applied to the SCS. This voltage was applied by means of a mercury relay switch with a rise time of about 1.0 nanoseconds. The basic circuits employed are shown in Figure 19.34.



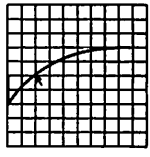

**DYNAMIC BREAKOVER VOLTAGE MEASUREMENTS**

**Figure 19.34**

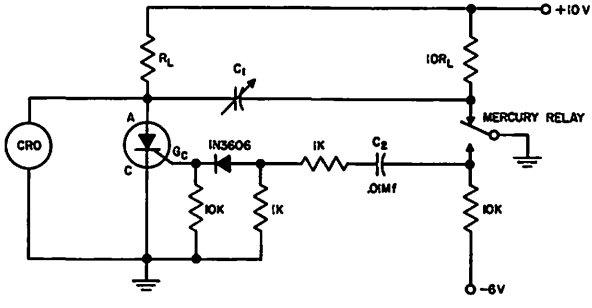
In Figure 19.34 $S_1$ is the mercury relay switch, $R_G$ is 10K for both the 3N58 and 3N59. With no bias applied, the potentiometer, the 10K series dropping resistor, and the 22.5 volt battery are removed for the 3N58. For the 3N59 $R_G$ is also removed. The CRO is a Tektronix 545 and a 0-100 volt regulated power supply was used to obtain the anode to cathode voltages. The operation of the circuit is as follows. The voltage from the power supply is increased until the unit conducts. The voltage applied to the unit is a rectangular pulse. The power supply voltage is then decreased until the unit just blocks again (this may be as low as 1/10 of the upper conduction voltage). This value is then the "true" dynamic breakover voltage. The difference in the two values is due to the fact that the collector capacitance develops and holds a charge while the voltage is "slowly" increased. This charge minimizes the dV/dt effect.

## TURN-OFF TIME MEASUREMENTS

In order to measure the turn-off time of the 3N58 one may use the circuit shown in Figure 19.35. The operation of the circuit is as follows. When the switch touches the upper position (that shown in the figure) capacitor $C_2$ charges. At the same time $C_1$ (which was previously charged to 10 volts) drives the anode to $-10$ volts and then begins to discharge. If the SCS turns off, the anode voltage will rise to $+10$ volts. $C_1$ is adjusted to the minimum value for turn-off and the turn-off time is measured.



HORIZONTAL SCALE = 0.5 μSEC/DIVISION
$T_0$ = 0.9 μS




**TURN-OFF TIME CIRCUIT FOR 3N58**

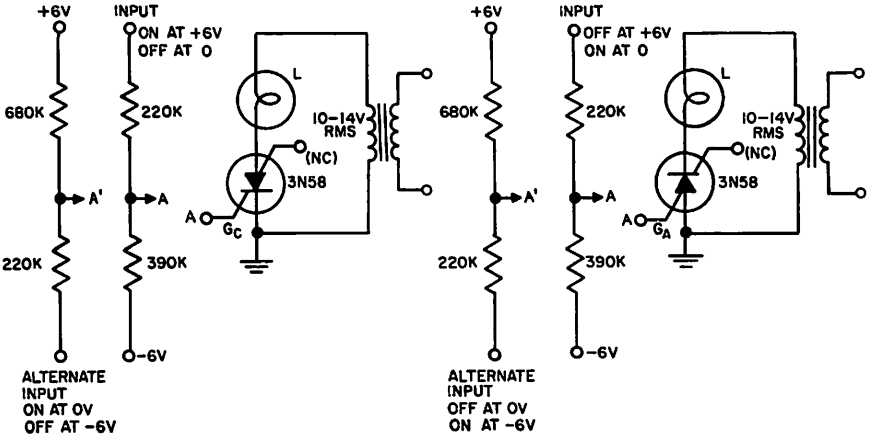
**Figure 19.35**

When the switch touches the lower position, $C_2$ discharges driving the unit into conduction again. At the same time, $C_1$ charges again so that the cycle may be repeated.

Note that the turn-off time, $t_o$, is defined as that time when the anode voltage reaches zero or ground potential. This is illustrated in the waveform accompanying the circuit. For precision one must use a decade capacitor with small incremental steps as $C_1$. As an example of suitable values, the following were found to give adequate results.

| | |
|---|---|
| $I_A = 1$ ma, $R_L = 10$K: | $C_1 = 0 - 200\ \mu\mu f$ |
| $I_A = 10$ ma, $R_L = 1$K: | $C_1 = .009 - 0.015\ \mu f$ |
| $I_A = 100$ ma, $R_L = 100\Omega$: | $C_2 = 0.1 - 0.25\ \mu f$ |

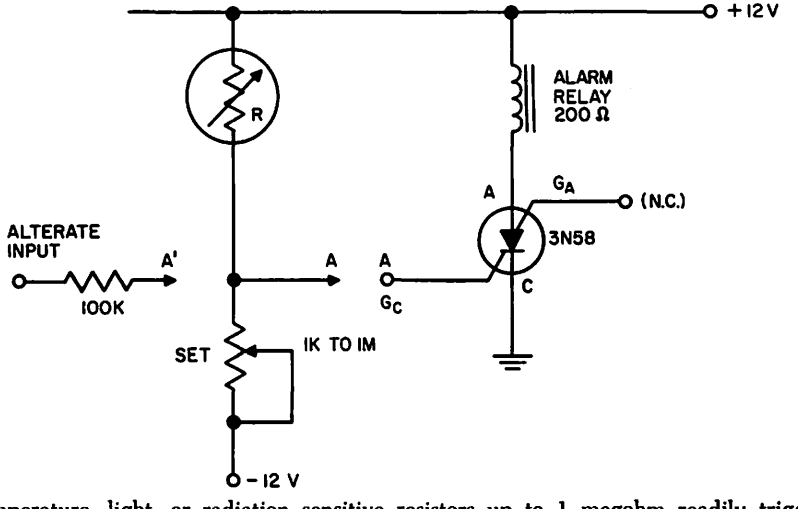
## SCS APPLICATIONS




NOTE – Connecting A or A' to the appropriate gate permits lamp control by positive or negative inputs. Lamp #344, 10 volts, 15 ma – Lamp #330, 14 volts, 80 ma.

**LAMP DRIVER**
**(INCANDESCENT LAMP OPERATE ON AC WITH 30μA MAXIMUM INPUT LOADING)**

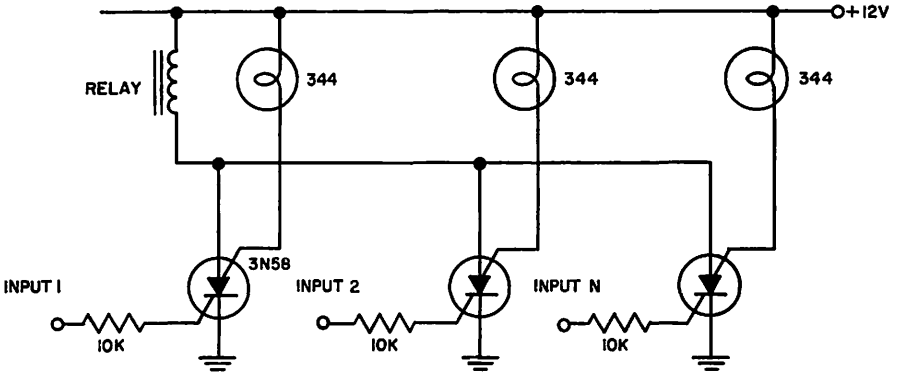
**Figure 19.36**




Temperature, light, or radiation sensitive resistors up to 1 megohm readily trigger alarm when they drop below value of preset potentiometer. Alternately, 0.75V at input to 100K triggers alarm. Connecting SCS between ground and —12V permits triggering on negative input to $G_A$.

**BASIC ALARM — VOLTAGE SENSING CIRCUIT**

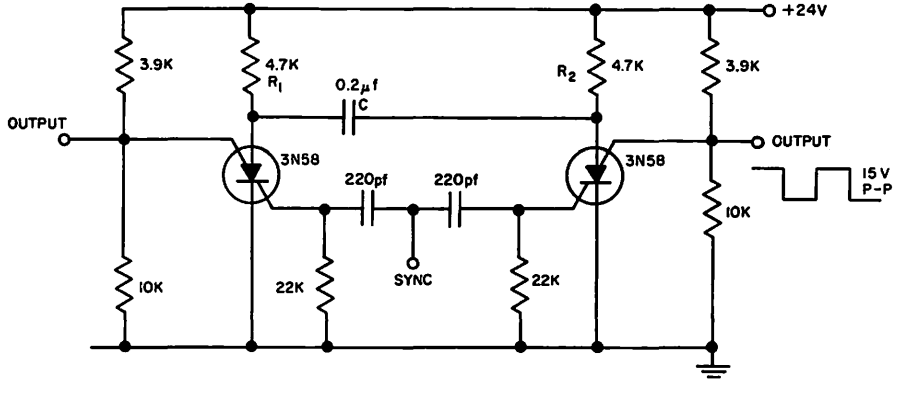
**Figure 19.37**




Any of several inputs pulls in common alarm relay with lamps giving visual indication of triggering input. Low resistance lamps decrease input sensitivity. (See Figure 19.19.)

**MULTIPLE ALARM CIRCUIT**

**Figure 19.38**



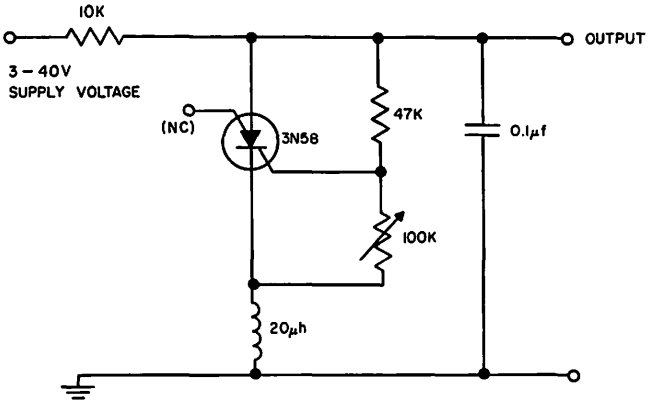

NOTE — $R_1C$ determine half the period; $R_2C$ the remainder.

$R_1 = R_2$ for square wave output.

Transient-free square or rectangular pulses are generated with equal and oppositely phased outputs. Synchronization and phase control readily feasible.

**SQUARE WAVE GENERATOR**

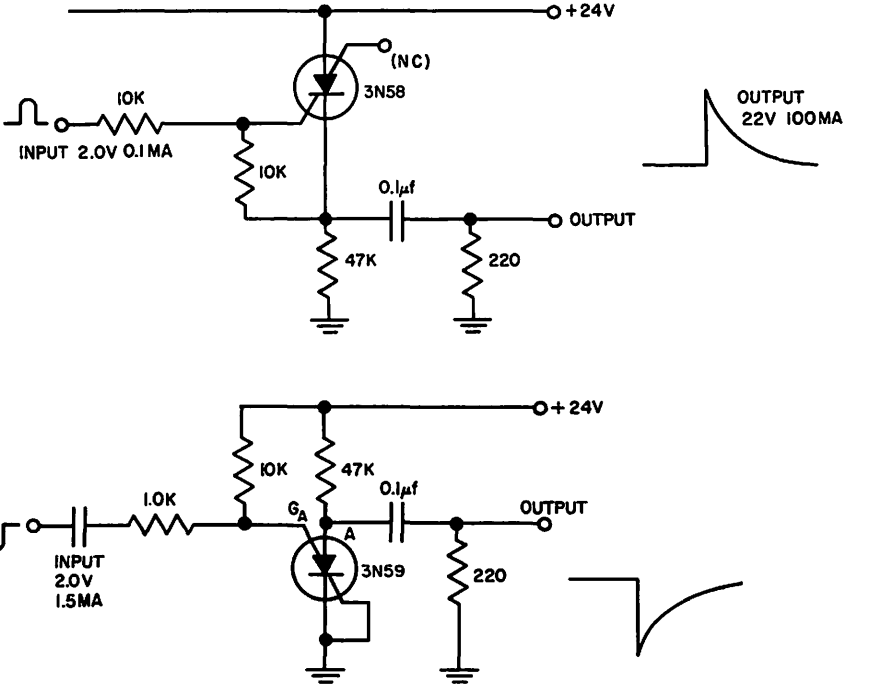
**Figure 19.39**




Amplitude and frequency are variable with potentiometer setting. Frequency alone is variable with supply voltage.

**SAWTOOTH GENERATOR**

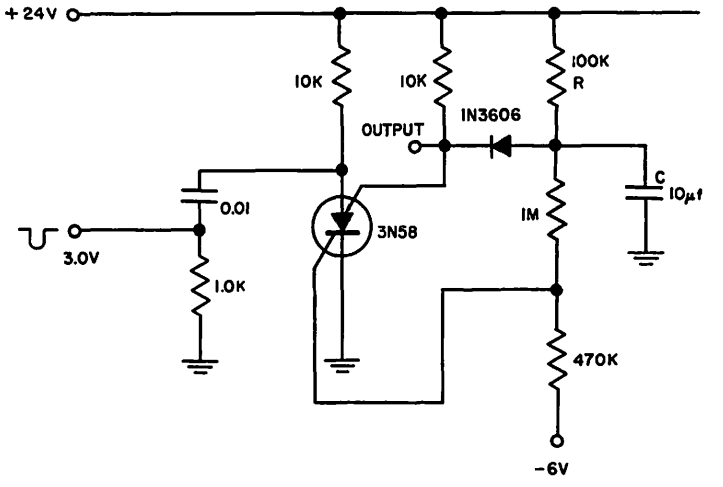
**Figure 19.40**




Positive or negative pulses are amplified without inversion. Low anode current is used to ensure turn off.

**PULSE AMPLIFIERS — STRETCHERS**

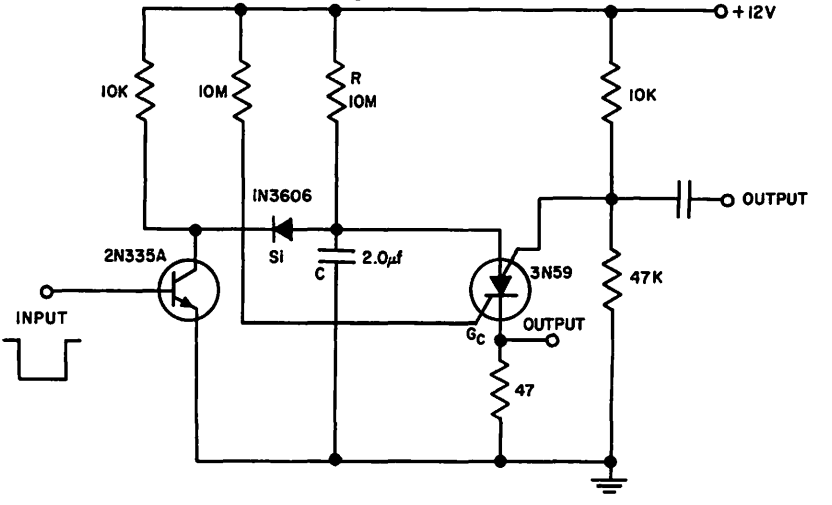
**Figure 19.41**




Short negative pulse initiates delay. When $G_C$ becomes forward biased by voltage divider connected to timing network RC the SCS fires terminating the delay. R, C, or —6V bias can be varied to modulate delay. Replacing 1M resistor with zener diode will minimize dependence of delay on bias voltage. A transient free output is available at $G_A$.

**TIME DELAY GENERATOR — PULSE ACTUATED**

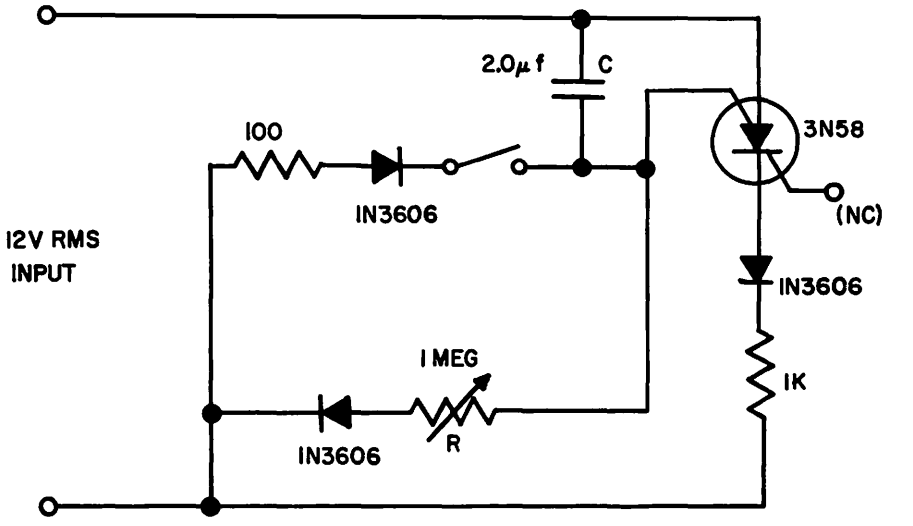
**Figure 19.42**




A negative gate to NPN transistor permits C to charge through R. When the anode becomes forward biased C discharges yielding negative and positive outputs. The 10 megohm resistor connected to $G_C$ insures firing regardless of how large R is. Maximum R is determined only by delay stability requirements with temperature.

**TIME DELAY GENERATOR — GATE ACTUATED**

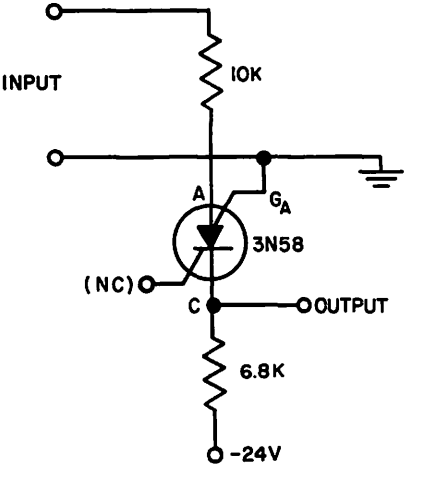
**Figure 19.43**




The switch is normally closed charging C and causing the SCS to block. Delay is initiated by opening the switch and discharging C through R. Since R is connected for only half of each cycle the delay is lengthened beyond the RC time constant. Following the delay the SCS conducts alternate half cycles.

**TIME DELAY GENERATOR — AC OPERATED**

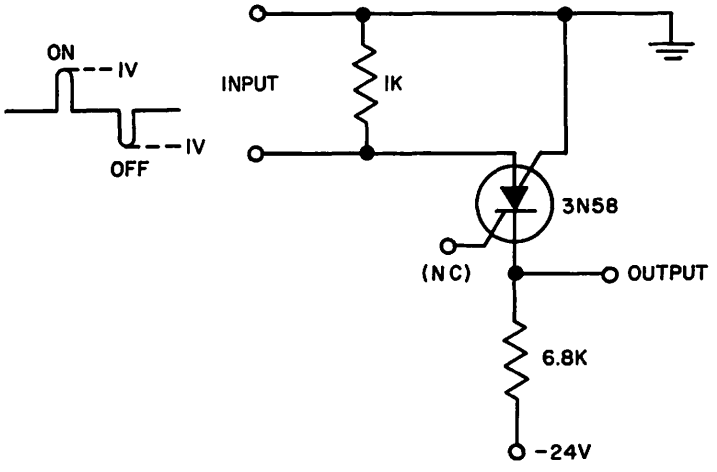
**Figure 19.44**




SCS conducts when input exceeds +1V. It stays on if $I_{in} = 0.1$ ma. It turns off when $I_{in} = 0$. On turning on, $V_A$ is approximately −0.25V for 6.8K load. $V_A = -3V$ for 1K load.

**SCHMITT TRIGGER**
**(OUTPUT IS IN PHASE WITH INPUT)**

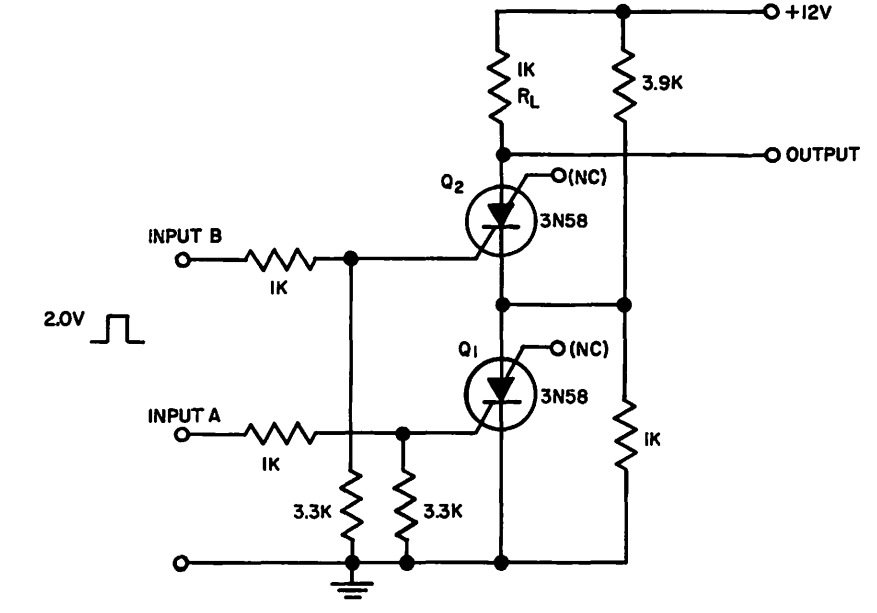
**Figure 19.45**




The output is in phase with the input signal.

**BISTABLE MEMORY ELEMENT**

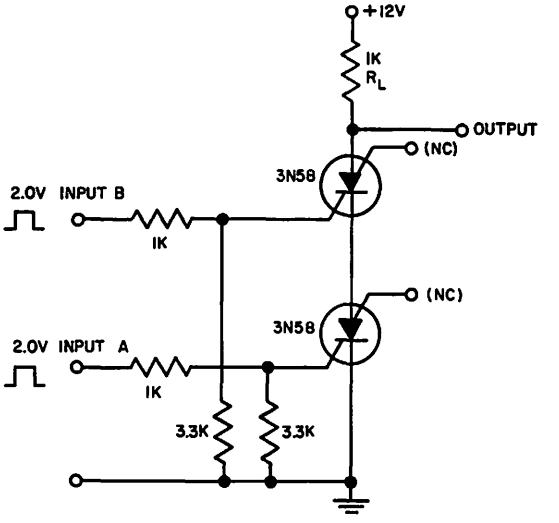
**Figure 19.46**




The resistor divider connected between $Q_1$ and $Q_2$ supplies $I_B$ to $Q_1$ after input A triggers it. It also prevents input B from triggering $Q_2$ until $Q_1$ conducts. Consequently the first B input pulse after input A is applied will supply current to $R_L$.

**PULSE SEQUENCE DETECTOR**

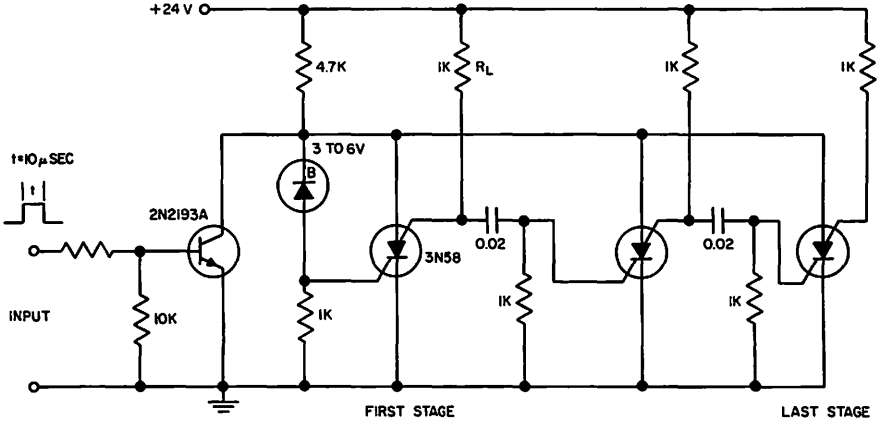
**Figure 19.47**




Unless inputs A and B (2 to 3V amplitude) occur simultaneously no voltage exists across $R_L$. Less than 1 microsecond overlap is sufficient to trigger the SCS. Coincidence of negative inputs is detected with gates $G_A$ instead of $G_C$ by using the SCS in a complementary SCR configuration.

**PULSE COINCIDENCE DETECTOR**

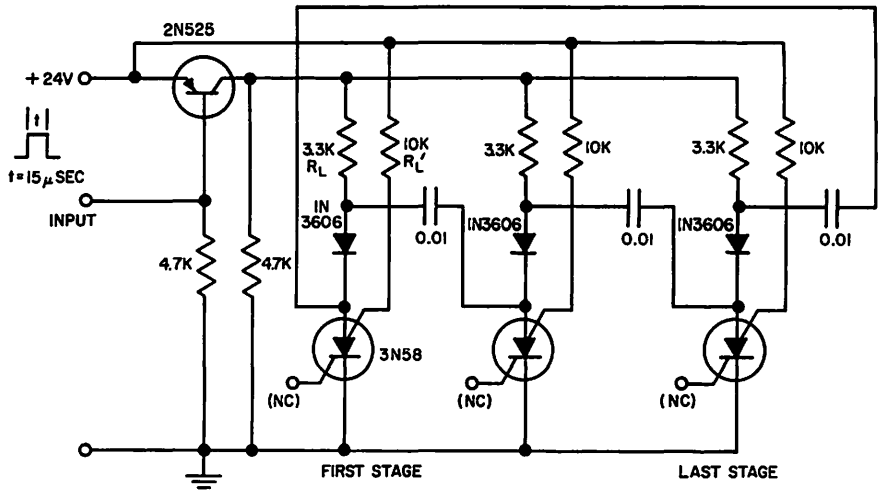
**Figure 19.48**




Low input power triggers counter. During normal counting the common anode voltage never exceeds 3 volts. When the last stage turns off the anode rises towards +24 volts turning on the first stage. The zener also resets the counter.

**RING COUNTER — INCLUDING RESET**

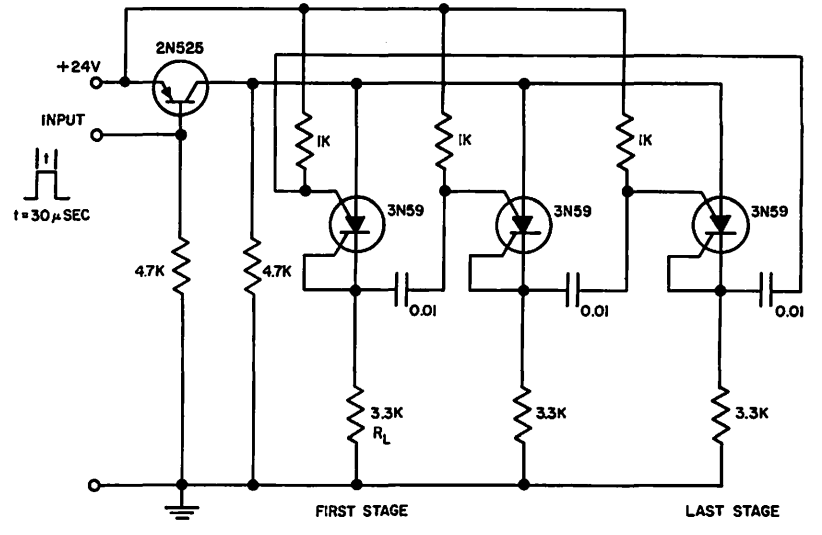
**Figure 19.49**




Two independent load resistors $R_L$ and $R_L'$ are available at each stage. The output at $R_L'$ is free from commutating transients. The input pulse provides a dead band equal to its width.

**RING COUNTER WITH INDEPENDENT OUTPUTS PER STAGE**

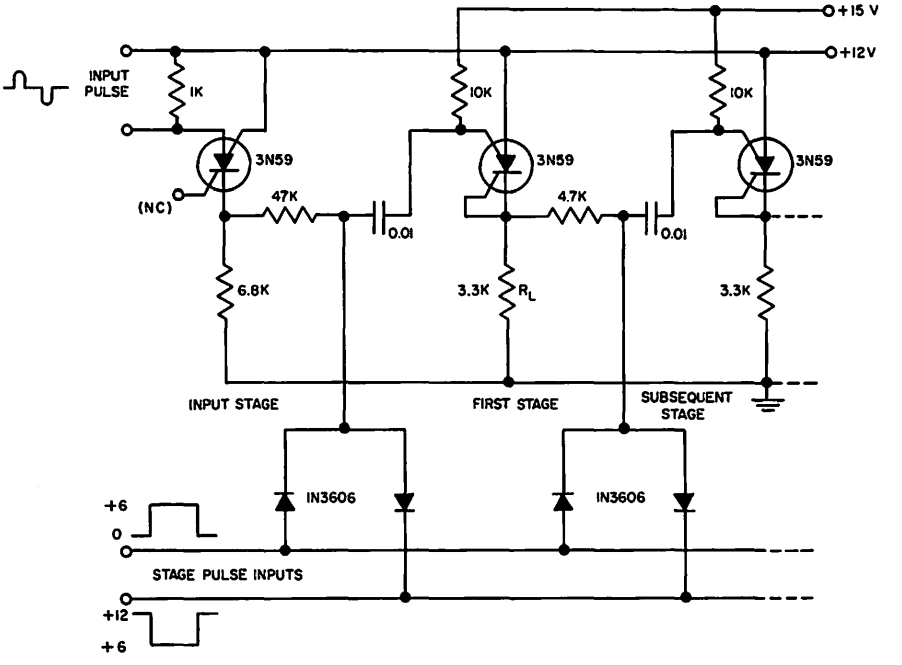
**Figure 19.50**




Triggering at $G_A$ permits loads with common ground.

**RING COUNTER — LOADS WITH COMMON GROUND**

**Figure 19.51**



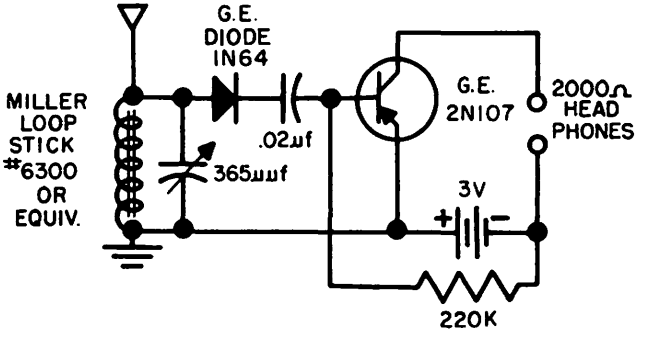

The bistable input stage drives the first shift register stage. The charge on the coupling capacitor determines which of the coincident shift pulses triggers the SCS producing a shift to the right. Load resistors have a common ground.

**SHIFT REGISTER CONFIGURATION**

**Figure 19.52**

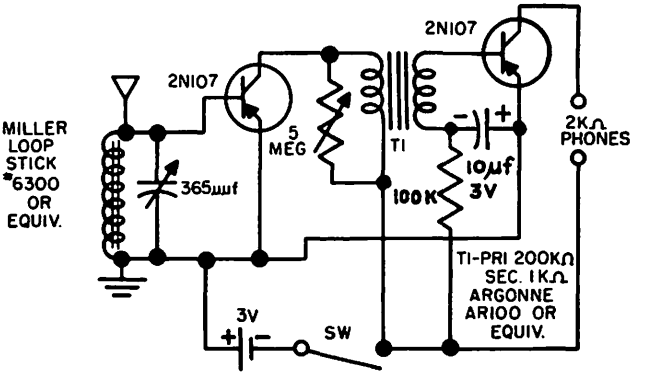
# EXPERIMENTERS CIRCUITS

CHAPTER 20



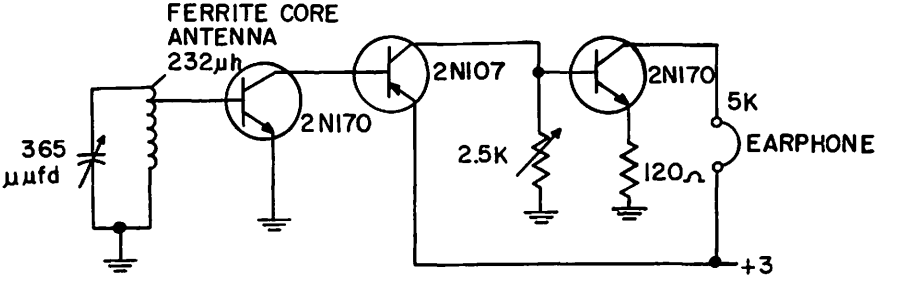

ONE TRANSISTOR RADIO RECEIVER

Figure 20.1



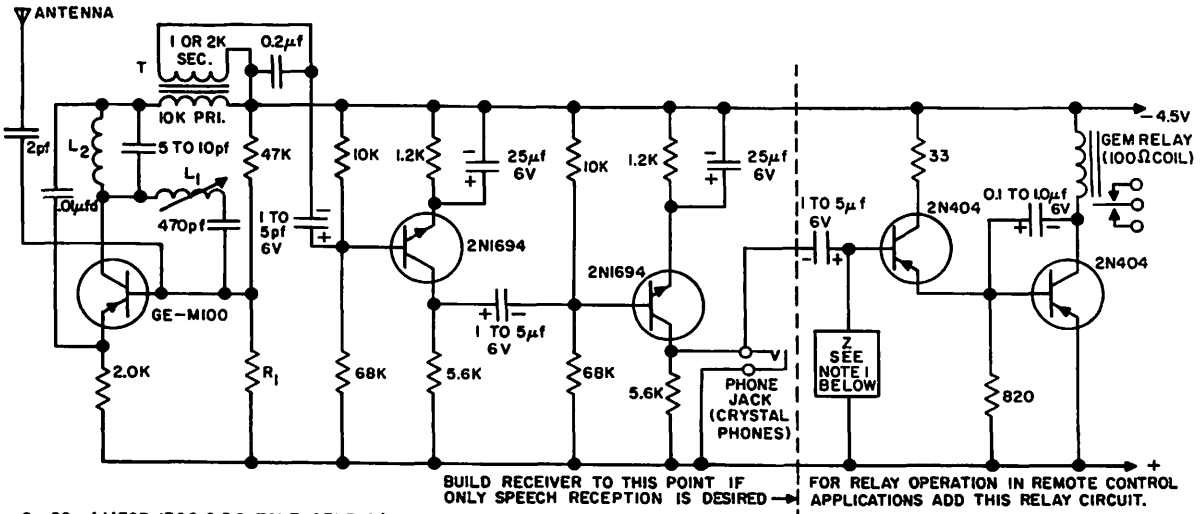

TWO TRANSISTOR RADIO RECEIVER

Figure 20.2




THREE TRANSISTOR RADIO RECEIVER

Figure 20.3




$C_1$ – .02 μfd (FOR 1300 C.P.S. TONE SELECT)

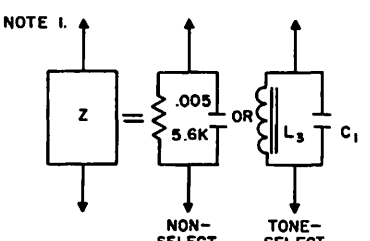
$R_1$ – 15 TO 47K (ADJUST TO OPTIMUM SENSITIVITY)

T – LAFAYETTE TR-98 INTERSTAGE TRANSFORMER OR TELEX T-42 (PART # C-8642) DRIVER TRANSFORMER, OR EQUIVALENT.

$L_1$ – 25 TURNS # 26 WIRE ON CTC (CAMBRIDGE THERMIONICS CORP.) TYPE LS6 (1/4" DIA.) CERAMIC FORM WITH RED AND WHITE DOT CORE.

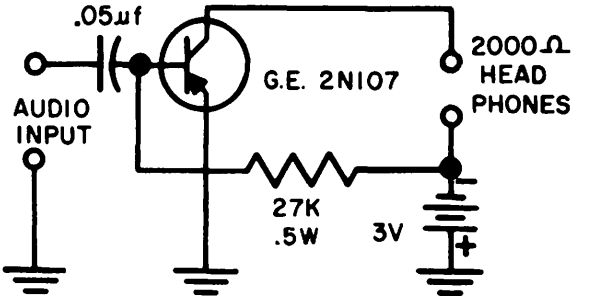
$L_2$ – 50μh RF CHOKE. NATIONAL CO. TYPE R33-50

$L_3$ – TYPE U50-21 TOROID COIL. (TOROTEL, INC., 5512 E. 110TH. KANSAS CITY 37, MO.)



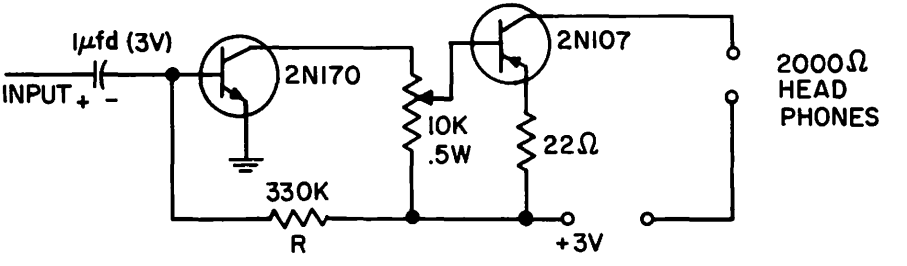

**CITIZENS BAND RECEIVER**

**Figure 20.4**




SIMPLE AUDIO AMPLIFIER

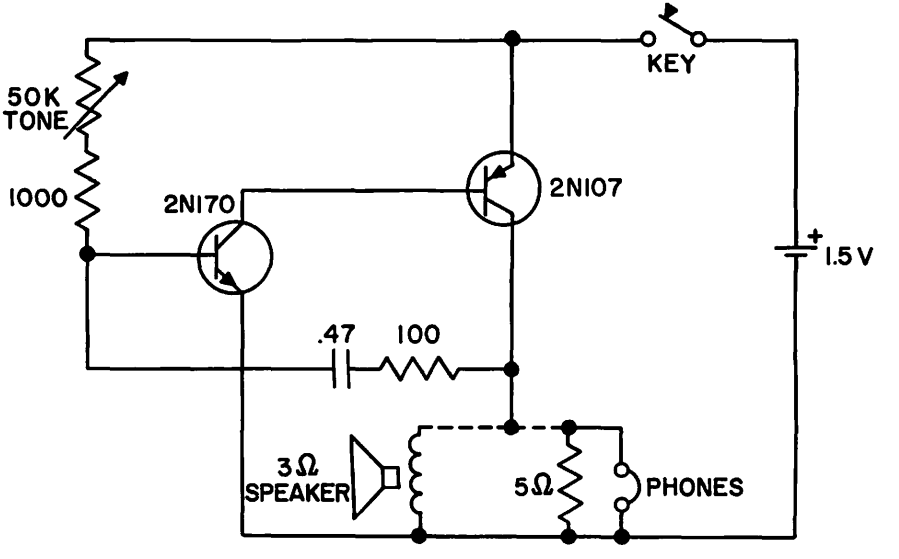
Figure 20.5




NOTE: ADJUST R FOR OPTIMUM RESULTS

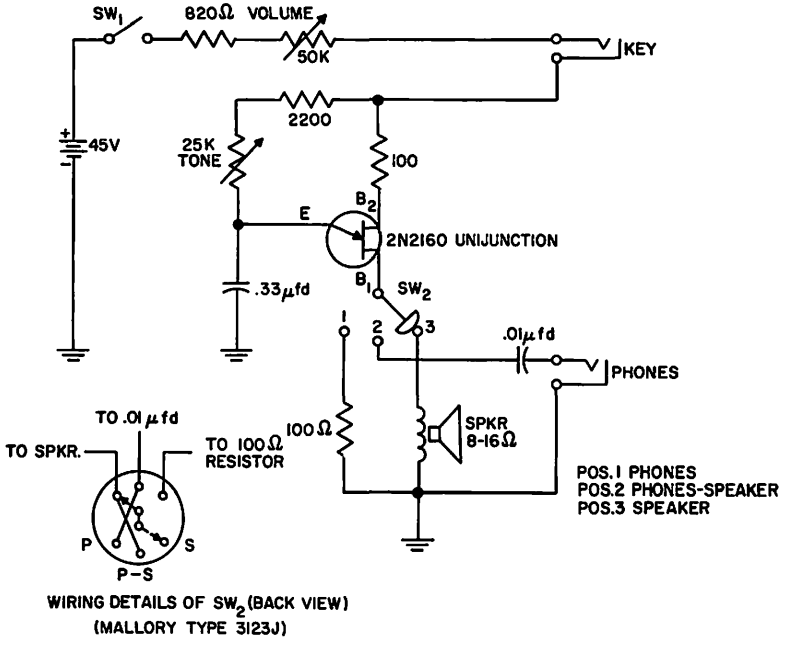
DIRECT COUPLED "BATTERY SAVER" AMPLIFIER

Figure 20.6




CODE PRACTICE OSCILLATOR

Figure 20.7




WIRING DETAILS OF $SW_2$ (BACK VIEW)
(MALLORY TYPE 3123J)

**UNIJUNCTION TRANSISTOR CODE PRACTICE OSCILLATOR**

**Figure 20.8**

NOTES:

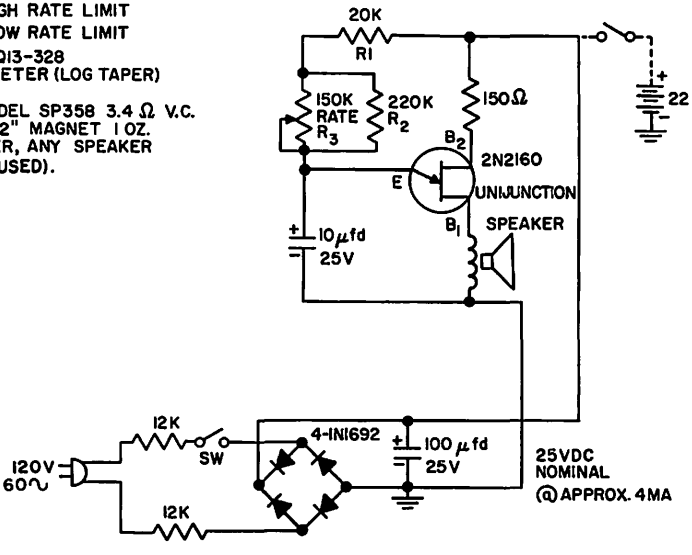
RATE-ADJUSTABLE FROM 40(LOW LARGO) TO 220(HIGH PRESTO) BEATS PER MINUTE

$R_1$-ADJUSTS HIGH RATE LIMIT

$R_2$-ADJUSTS LOW RATE LIMIT

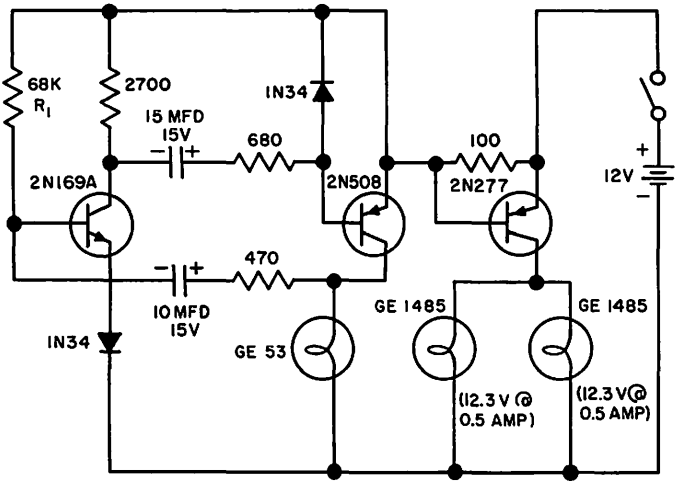
$R_3$-IRC TYPE Q13-328 POTENTIOMETER (LOG TAPER)

SPKR-UTAH MODEL SP358 3.4 Ω V.C. SIZE 3 1/2" MAGNET 1 OZ. (HOWEVER, ANY SPEAKER CAN BE USED).




**UNIJUNCTION TRANSISTOR METRONOME**

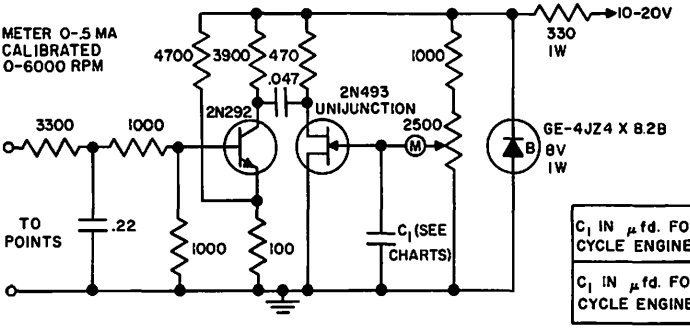
**Figure 20.9**




$R_1$ – VARY FROM 47K TO 82K FOR DESIRED FLASH RATE

**HIGH POWER LIGHT FLASHER**
**(FOR BOATS, AIRCRAFT, EMERGENCY VEHICLES, BARRICADES)**

**Figure 20.10**

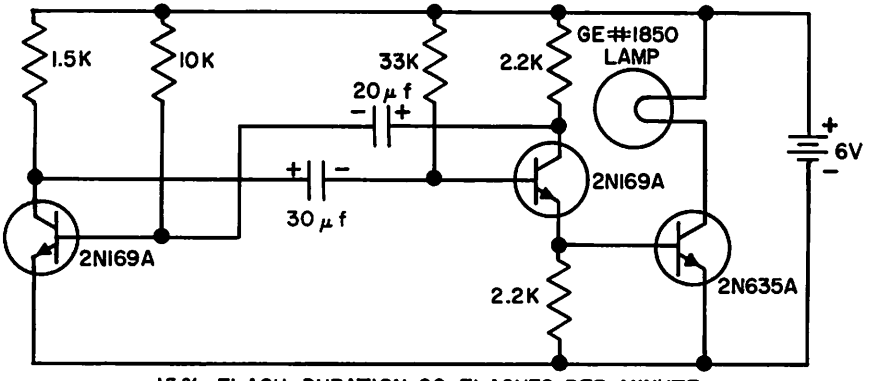



| NO. OF CYLINDERS | 4 | 6 | 8 |
|---|---|---|---|
| $C_1$ IN μfd. FOR 2 CYCLE ENGINE | .33 | .22 | .15 |
| $C_1$ IN μfd. FOR 4 CYCLE ENGINE | .68 | .47 | .33 |

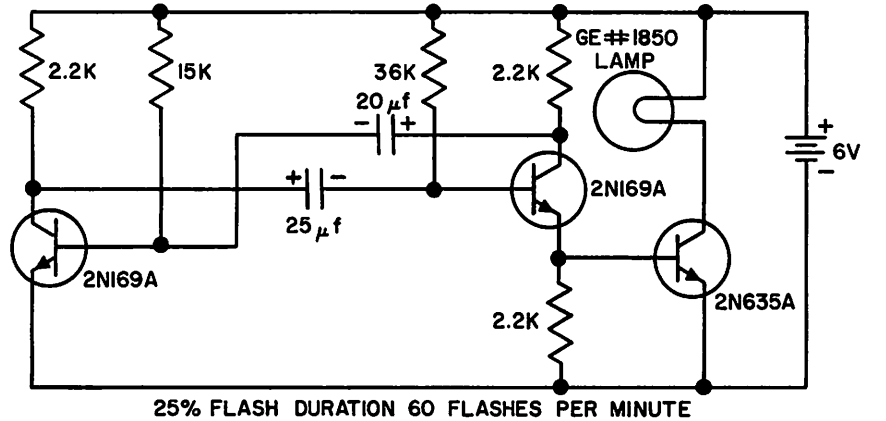
| GENERAL AUTOMOTIVE IGNITION INFORMATION | | | | | | |
|---|---|---|---|---|---|---|
| | TWO CYCLE | | | FOUR CYCLE | | |
| | 4 CYL. | 6 CYL. | 8 CYL. | 4 CYL. | 6 CYL. | 8 CYL. |
| SPARKS/REV. | 4 | 6 | 8 | 2 | 3 | 4 |
| SPARKS/SEC. AT 600 RPM | 40 | 60 | 80 | 20 | 30 | 40 |
| TIME/SPARK AT 600 RPM | 25 MS | 16.7 | 12.5 | 50 | 33.3 | 25 |
| SPARK/SEC. AT 6000 RPM | 400 | 600 | 800 | 200 | 300 | 400 |
| TIME/SPARK AT 6000 RPM | 2.5MS | 1.67 | 1.25 | 5.0 | 3.33 | 2.5 |
| CAMSHAFT SPEED TO CRANKSHAFT SPEED | EQUAL | EQUAL | EQUAL | HALF | HALF | HALF |
| CAM DEGREES/SPARK | 90° | 60° | 45° | 90° | 60° | 45° |
| CRANK DEGREES/SPARK | 90° | 60° | 45° | 180° | 120° | 90° |

**ULTRA-LINEAR HIGH PRECISION TACHOMETER**
**(FOR AUTOMOTIVE TYPE IGNITION SYSTEMS)**

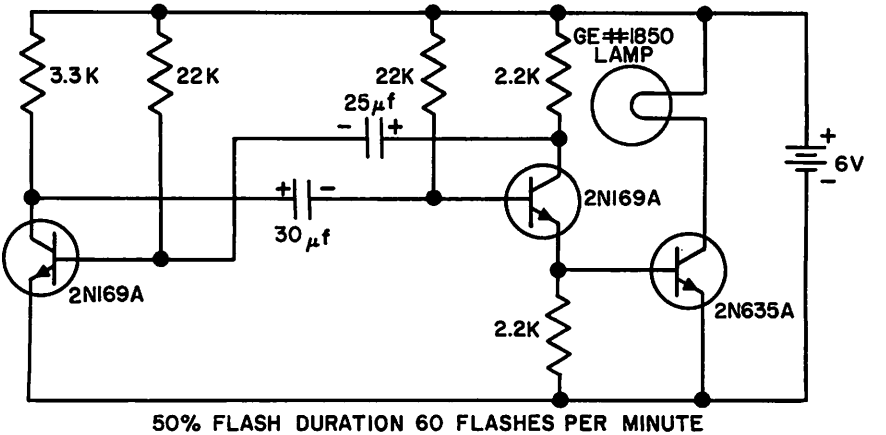
**Figure 20.11**




15% FLASH DURATION 60 FLASHES PER MINUTE



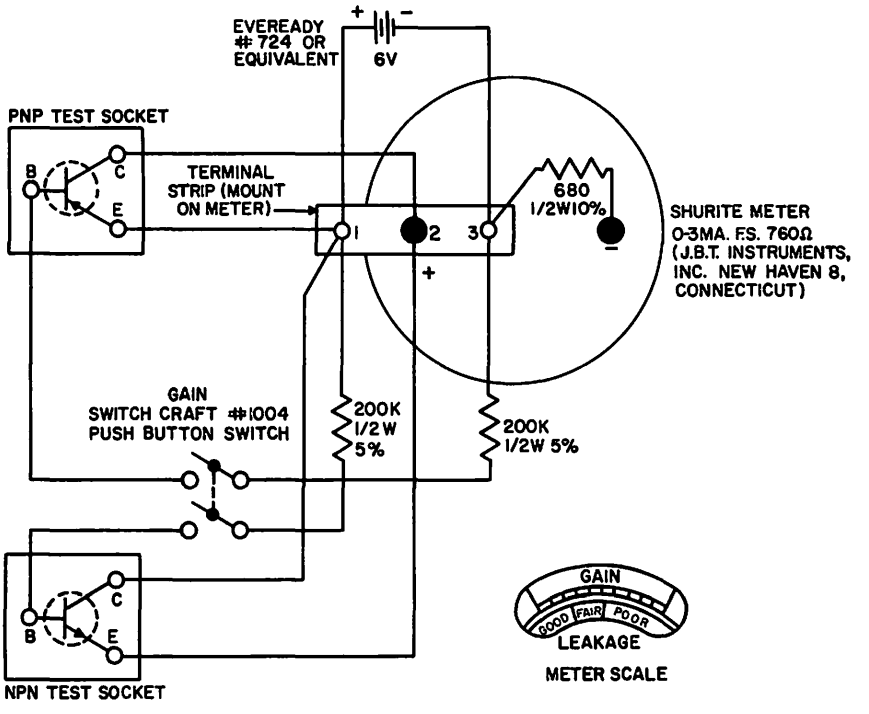

25% FLASH DURATION 60 FLASHES PER MINUTE




50% FLASH DURATION 60 FLASHES PER MINUTE

**FLASHER CIRCUITS**

**Figure 20.12**




INSTRUCTIONS FOR TRANSISTOR TEST SET

BATTERY CHECK: INSERT 560 OHM RESISTOR BETWEEN E AND C (EITHER SOCKET). IF METER DOES NOT READ FULL SCALE, REPLACE BATTERY (EVEREADY TYPE 724 OR EQUIVALENT)

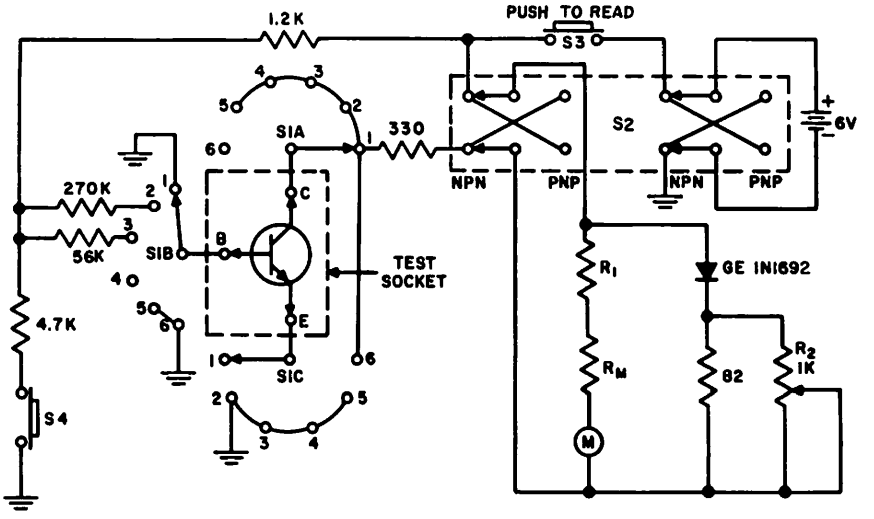
LEAKAGE TEST: INSERT TRANSISTOR IN APPROPRIATE SOCKET. METER READING INDICATES CONDITION WITH RESPECT TO LEAKAGE.

GAIN TEST: DEPRESS GAIN BUTTON AND NOTE INCREASE IN METER DEFLECTION. AN INCREASED DEFLECTION TO THE RIGHT EQUAL TO AT LEAST ONE DIVISION ON THE GAIN SCALE COMPARED TO THE DEFLECTION DURING LEAKAGE TEST INDICATES ACCEPTABLE CURRENT GAIN.

OPENS AND SHORTS TEST: A SHORTED TRANSISTOR WILL BE INDICATED BY A FULL SCALE METER DEFLECTION IN LEAKAGE TEST. AN OPEN TRANSISTOR WILL BE INDICATED BY NO METER DEFLECTION IN BOTH LEAKAGE AND GAIN TESTS.

**TRANSISTOR TEST SET**

**Figure 20.13**




PARTS

S1-3 POLE 6 POSITION NON-SHORTING SELECTOR SWITCH

S2-4 POLE 2 POSITION SWITCH

S3-S4 NORMALLY OPEN PUSH-SWITCHES

M-100μA FULL SCALE METER

$R_M$-METER S INTERNAL RESISTANCE

| TO TEST | WHEN | ADJUST SELECTOR SWITCH S1 TO POSITION | RESULT | |
|---|---|---|---|---|
| $I_{CO}$ | $V_{CB}$ = 6V | 1 | READ METER DIRECT | |
| $I_C$ | $I_B$ = 20μA | 2 | READ METER DIRECT | |
| $I_C$ | $I_B$ = 100μA | 3 | READ METER DIRECT | |
| $I_{CEO}$ | $V_{CE}$ = 6V | 4 | READ METER DIRECT | |
| $I_{CES}$ | $V_{CE}$ = 6V | 5 | READ METER DIRECT | |
| $I_{EO}$ | $V_{EO}$ = 6V | 6 | READ METER DIRECT | |
| $h_{FE}$ | $I_B$ = 20μA | 2 | CALCULATE: $h_{FE} = \frac{I_C}{I_B} = \frac{\text{METER READING}}{20\mu A}$ | |
| $h_{FE}$ | $I_B$ = 100μA | 3 | CALCULATE: $h_{FE} = \frac{I_C}{I_B} = \frac{\text{METER READING}}{100\mu A}$ | |
| $h_{fe}$ | $I_B$ = 20μA | 2 | CALCULATE: $h_{fe} = \frac{I_{C1} - I_{C2}}{4 \times 10^{-6}}$ | WHERE: $I_{C1}$ = METER READING; $I_{C2}$ = METER READING WITH $S_4$ CLOSED |
| $h_{fe}$ | $I_B$ = 100μA | 3 | CALCULATE: $h_{fe} = \frac{I_{C1} - I_{C2}}{20 \times 10^{-6}}$ | |
| 6V. BATTERY | —— | 4 | WITH 150Ω RESISTOR CONNECTED TO C-E OF TEST SOCKET, FULL-SCALE METER DEFLECTION WILL RESULT WHEN $S_3$ IS PRESSED. | |

SAFE AND SIMPLE TRANSISTOR TESTER

**Figure 20.14**

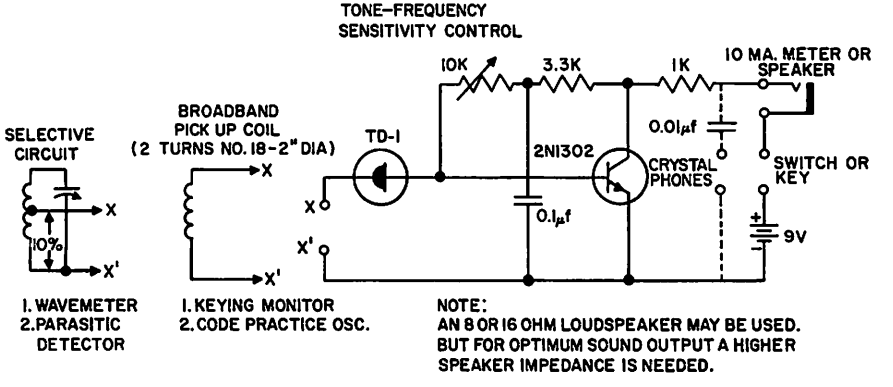
The 100 $\mu$a meter is in a network which results in a nearly linear scale to 20 $\mu$a, a highly compressed scale from 20 $\mu$a to 1 ma and a nearly linear scale to full scale at 10 ma. The network permits reading $I_{CO}$, $I_{EO}$, $I_{CES}$, and $I_{CEO}$ to within 10% on all transistors from mesas to power alloys without switching meter ranges or danger to the meter movement.

By making $R_m + R_1$ equal to 12K the scale will be compressed only 1 $\mu$a at 20 $\mu$a. Potentiometer $R_2$ should be adjusted to give 10 ma full scale deflection. The scale can then be calibrated by comparison with a standard conventional meter.

If the NPN-PNP switch is in the wrong position, the collector and emitter junctions will be forward biased during the $I_{CO}$ and $I_{EO}$ tests respectively. The high resulting current can be used as a check for open or intermittent connections within the transistor.

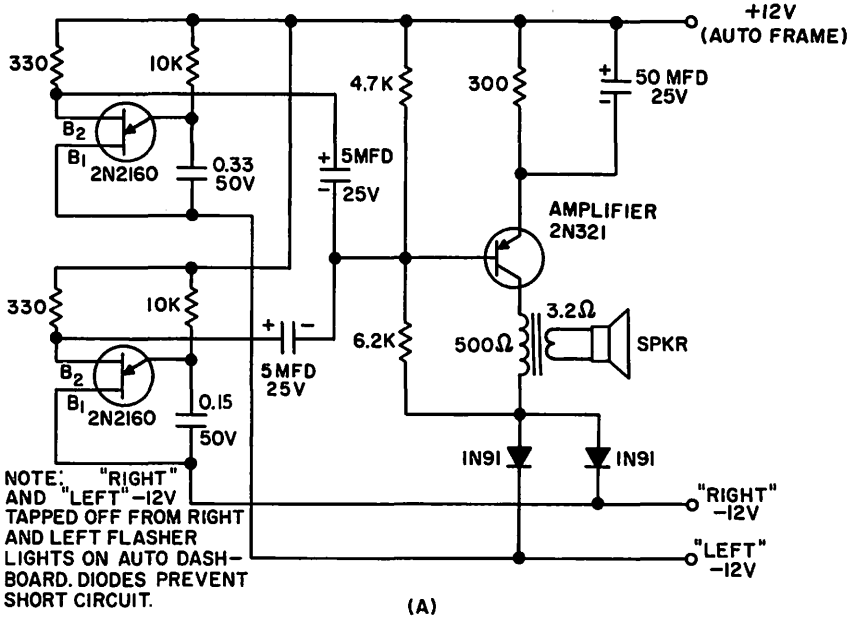
The test set also measures $h_{FE}$ with 20 $\mu$a and 100 $\mu$a base current. Depressing the $h_{fe}$ button decreases the base drive 20% permitting $h_{fe}$ to be estimated from the corresponding change in collector current. The tests are done with a 330Ω resistor limiting the collector current to approximately 12 ma and maximum transistor dissipation to approximately 20 mw. Therefore, this test set can not harm a transistor regardless of how it is plugged in or how the switches are set.

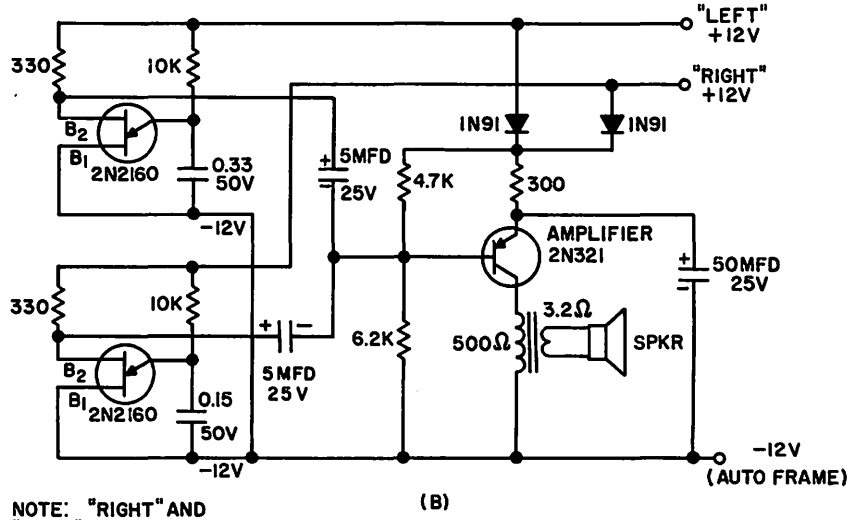
"Battery test" has been designed to give full scale meter deflection of 10 ma when the battery voltage is 6 volts. This is achieved by connecting 150 ohms from C to E of the test socket. This test assumes precision resistors.




**SENSITIVE BROADBAND CW KEYING MONITOR — CODE PRACTICE OSCILLATOR — SENSITIVE AURAL/VISUAL PARASITIC DETECTOR OR WAVEMETER**

**Figure 20.15**




Provides audible turn signal indication to insure signals are off after turn. Allows driver to keep attention on road at all times. Dash indicator lights need never be consulted.

**AUDIBLE AUTO SIGNAL MINDER**

**Figure 20.16**

# READER'S LIST

CHAPTER 21

The following list of publications includes books pertaining only to semiconductors and closely related subjects. This list has been compiled so the interested reader can see just what books are available to him, the price, and where further information regarding the books may be obtained. Prices as shown may or may not be accurate since prices are always subject to change.

Some books here listed contain quite extensive bibliographies. For example, the *Handbook of Semiconductor Electronics,* edited by Lloyd P. Hunter contains 68 pages of references covering the period from 1936 through 1955. Such books as *Principles of Transistor Circuits* and *Transistor Circuit Engineering* edited by Richard F. Shea also contain extensive reference lists.

*ABC's of Transistors*
Sams $1.25

*Advances in Semi-conductor Science*
Brook, H., – General Editor
Pergamon (1959) $15.00

*An International Journal for Transistor and other Solid-State Devices*
Crawford, F., Editor-in-Chief
Pergamon $40.00/annum

*An Introduction to the Theory and Practice of Transistors*
Tillman, J. R., and Roberts, F. F.
Wiley (1961) $8.00

*Basic Electronics* – Vol. 6
VanValkenburgh, Nooger & Neville
Rider (1960) $2.90

*Basic Radio* – Vol. 5 (Transistors)
Tepper, M.
Rider (1960) $1.90

*Basic Theory and Application of Transistors*
Technical Manual 11 – 690
Department of the Army –
U. S. Govt. (1959) $1.25

*Basic Transistors*
Schure, A.
Rider (1961) $5.50

*British Transistor Manual*
Bradley, E. N.
Norman Price Pub. Ltd. (1959) 12s6d
also Wehman $3.00

*Crystal Rectifiers*
Torrey, H. C. and Whitmer, C. H.
McGraw (1948) $8.50

*Crystal Rectifiers and Transistors*
Molloy, E., Editor
British Book Service (1954) $3.60

*Design of Transistorized Circuits for Digital Computers*
Pressman, A. I.
Rider (1959) $9.95

*Electrical Engineering Materials*
Dekkar, A. J.
Prentice-Hall (1959) $6.50

*Electric Conduction in Semiconductors and Metals*
Ehrenberg, W.
Oxford (1959) $10.10

*Electronic Semiconductors*
Spenke, E.
McGraw (1958) $11.00

*Electronic Tubes and Semiconductor Elements – Universal Vade-Mecum*
Pergamon Vol. 1 (1961) approx. $20.00
Vol. 2 (1962) approx. $20.00

*Electrons and Holes in Semiconductors*
Shockley, W.
VanNostrand (1950) $9.75

*Electron Tubes and Semiconductors*
DeFrance, J. J.
Prentice-Hall (1958) $9.00

*Experiments in Electronics*
Evans, W. H.
Prentice-Hall (1959) $6.75

*Feedback and Stability of Junction Transistor Circuits*
Ioawa State College of Agriculture & Mechanical Arts,
(Engineering Experimental Station, Ames, Iowa) (1954) $1.25

*Fundamental Principles of Transistors*
Evans, J.
VanNostrand (1958) $6.75

*Fundamentals of Transistor Physics*
Gottlieb, I. M.
Rider (1958) $3.50

*Fundamentals of Transistors*
(2nd. Edition Revised & Enlarged)
Krugman, L. M.
Rider (1958) $3.50

*Handbook of Semiconductor Electronics*
Hunter, L. P., Editor
McGraw (1956) $14.00

*Handbook of Transistor Circuit Design*
Pullen, K. A.
Prentice-Hall (1961) $13.00

*International Transistor Substitution Guidebook*
Pullen, K. A.
Rider (1961) $1.50

*Introduction to Junction Transistor Theory*
Middlebrook, R. D.
Wiley (1957) $8.50

*Introduction to Semiconductors*
Dunlap, W. C.
Wiley (1957) $11.75

*Introduction to the Theory and Practice of Semiconductors*
Shepard, A. A.
Ungar (1959) $4.75

*Introduction to Transistor Circuits*
(2nd. Edition)
Cooke-Yarborough, E.H.
Interscience (1960) $3.50

*Industrial Transistor and Semiconductor Handbook*
Tomer, R. B.
Sams (1961) $4.95

*Junction Transistor and Its Applications*
Wolfendale, E., Editor
Macmillan (1958) $7.50

*Junction Transistor Electronics*
Hurley, R. B.
Wiley (1958) $12.50

*Junction Transistors in Pulse Circuits*
Neeteson, P. A.
Macmillan (1960) $5.50

*Metallic Rectifiers and Crystal Diodes*
Conti, T.
Rider (1958) $2.95

*Modern Transistor Circuits*
Carroll, J. M .
McGraw (1959) $8.50

*Philips Gloeilampenfabrieken, Semi-conductors*
Philips (1959) 3.50 fl

*Photo and Thermoelectric Effects in Semiconductors*
Tanc, J.
Pergamon

*Physics of Semiconductors*
(revised & enlarged edition)
Ioffe, A. F.
Academic Press (1960) $12.50

*Pin-Point Transistor Troubles in 12 Minutes*
Garner, L. E.
Coyne (1959) $5.95

*Practical Transistors and Circuits*
Kendall
Wehman $1.00

*Practical Transistor Servicing*
Caldwell, W. C.
Sams (1960) $2.95

*Preparation of Single Crystals*
Lawson, W. D., and Nielson, S.
Academic Press (1958) $8.80

*Principles of Transistor Circuits*
Shea, R. F.
Wiley (1953) $12.75

*Principles of Semiconductor Device Operation*
Jonscher, A. K.
Wiley (1960) $5.00

*Principles of Semiconductors*
Scroggie, M. G.
Iliffe (1961) 21s

*Principles of Transistor Circuits*
(2nd. Edition)
Amos, S. W.
British Book Service (1961) $5.25
also Rider (1959) $3.90

*Progress in Semiconductors*
Gibson, Alan F. and others
Wiley (1956) Vol. 1 $8.00
(1957) Vol. 2 $10.50
(1958) Vol. 3 $8.50
(1960) Vol. 4 $10.50
(1961) Vol. 5 $11.00

*Properties, Physics, and Design of Semiconductor Devices*
Shive, J. N.
VanNostrand (1959) $9.75

*Radio, Television, Industrial Tube, Transistor and Diode Equivalents Handbook*
Babani, B. B.
Bernards (1960) 9s6d

*Rectifying Semiconductor Contacts*
Henisch, H. K.
Oxford U. P. (1957) $11.20

*Reference Manual of Transistor Circuits*
Mullard Overseas Ltd. (1960) 12s6d

*Repairing Transistor Radios*
Libes, S.
Rider (1960) $3.50

*Selected Semiconductor Circuits Handbook*
Schwartz, S., Editor
Wiley (1960) $12.00

*Semiconducting III-V Compounds*
Hilsum, C. and Rose-Innes, A. C.
Pergamon (1961) $10.00

*Semiconductor Device Physics*
Nussbaum
Prentice-Hall (1962) $8.25

*Semiconductor Devices*
Turner, R. P.
Holt (1961) $6.95

*Semiconductor Devices and Applications*
Greiner, R. A.
McGraw (1961) $12.50

*Semiconductor-Diode Parametric Amplifiers*
Blackwell, L. A., and Kotzebue, K. L.
Prentice-Hall (1961) $6.75

*Semiconductor Reliability*
Shwap, J. E., and Sullivan, H. J., Editors
Eng. Pubs. (1961) $8.50

*Semiconductors*
Hannay, N. B., Editor
Reinhold (1959) $15.00

*Semiconductors*
Schön, M., and Welker, H.
Interscience (1958) $16.50

*Semiconductors*
Smith, R. A.
Cambridge (1959) $12.50

*Semiconductors* – Vol. 1
Desirant, M., and Michaels, J. L., Editors
Academic Press

*Semiconductors and Transistors*
Schure, A.
Rider (1961) $2.90

*Semiconductors and Transistors*
Warschaver, D. M.
McGraw (1959) $7.00

*Semiconductors* – 3rd. Edition
Wright, D. A.
Methuen (1958) 8s6d

*Semiconductor Surface Physics*
Kingston, R. H., Editor
Univ. of Pa. (1956) $8.50

*Semiconductors: Their Theory and Practice*
Gaudet, G., and Meuleau, C.
Essential Books (1957) $18.90

*Servicing Transistor Radios*
8 Volumes
Sams $2.95 each

*Servicing Transistor TV Receivers*
Sams (1961) $4.50

*Solid State Physical Electronics*
VanDerZiel, A.
Prentice-Hall (1957) $9.75

*The Physical Theory of Transistors*
Valdes, L. B.
McGraw (1961) $10.95

*Theory of Noise in a Multidimensional Semi-conductor with a P-N Junction*
Solow, M.
Catholic University of Am. Press (1957) $1.25

*The Surface Chemistry of Metals and Semiconductors*
Gatos, H. C., Editor
Wiley $12.50

*The Transistor*
Bell Telephone Laboratories, Inc. (1951)

*Transistor Audio Amplifiers*
Shea, R. F.
Wiley (1955) $7.00

*Transistor (Audio Frequency) A. F. Amplifiers*
Jones, D. D., and Helbourne, R. A.
Philosophical Library (1957) $6.00

*Transistor Circuit Analysis*
Joyce, M. V., and Clarke, K. K.
Addison-Wesley (1961) $10.75

*Transistor Circuit Analysis & Design*
Fitchen, F. C.
VanNostrand (1960) $7.50

*Transistor Circuits*
Cattermole, K. W.
Macmillan (1959) $14.00

*Transistor Circuits*
Turner, R. P.
Gernsback (1957) $2.75

*Transistor Circuits and Applications*
Carroll, J. M.
McGraw (1957) $8.00

*Transistor Circuit Engineering*
Shea, R. F., Editor
Wiley (1957) $12.00

*Transistor Circuit Handbook*
Garner, L. E., Jr.
Coyne $4.95

*Transistor Circuit Manual*
Lytel, A.
Sams (1961) $4.95

*Transistor Electronics*
DeWitt, D., and Rossoff, A. L.
McGraw (1957) $8.00

*Transistor Electronics*
Lo, A. W., and others
Prentice-Hall (1955) $12.00

*Transistor Engineering Reference Handbook*
Marrous, H. E.
Rider (1957) $9.95

*Transistor Handbook*
Bevitt, W. D.
Prentice-Hall (1956) $9.00

*Transistor Logic Circuits*
Hurley, R. B.
Wiley (1961) $10.00

*Transistor Physics and Circuits*
Riddle, R. L., and Ristenbatt, M. P.
Prentice-Hall (1957) $10.00

*Transistor Projects*
Radio-Electronics Magazine
Gernsback (1960) $2.90

*Transistors*
Coblenz, A., and Owens, H. L.
McGraw (1955) $6.50

*Transistors*
Gärtner, W. W.
VanNostrand (1961) $12.50

*Transistors*
Gillie, A.
Prentice-Hall (1959) $7.95

*Transistors*
Staff-Gernsback Library, Inc.
Gernsback (1961) $1.95

*Transistors*
RCA Laboratories (1956) $4.50

*Transistors and Active Circuits*
Linvill, J. G., and Gibbons, J. F.
McGraw (1961) $14.50

*Transistors and Crystal Diodes*
Bettridge, B. R.
Wehman (1954) $1.00

*Transistors and Other Crystal Values*
Scott, T. R.
Oxford U. P. (1955) $7.20

*Transistors and Their Applications in TV and Radio-Electronics*
Coyne $1.50

*Transistors in Radio, Television and Electronics* – 2nd. Edition
Kiver, M. S.
McGraw (1959) $7.95

*Transistor Substitution Handbook – Revised*
Sams (1961) $1.50

*Transistor Techniques*
Staff-Gernsback Library, Inc.
Gernsback (1956) $1.50

*Transistor Techniques*
Leahrman, H.
Gernsback (1957) $1.50

*Transistor Technology*
Biondi, F. J., Editor
Bell Telephone Laboratories
VanNostrand Vol. 1 & 2 $17.50 each
(1958) Vol. 3 $12.50

*Transistor Theory and Circuits Made Simple*
Pollack, H.
Am. Electronics (1958) $1.75

*Transistor Theory and Practice*
(2nd. revised edition)
Turner, R. P.
Gernsback (1958) $2.95

*Transistors Work Like This*
Lehrburger, E.
Roys Publishing (1957) $2.50

*Tube and Semiconductor Selection Guide*
Kroes, T. J.
Cleaver-Hume (1961) 12s6d

*Vacuum Tube and Semiconductor Electronics*
Millman, J.
McGraw (1958) $10.75

*Vacuum-Tube Circuits and Transistors*
Arguimbau, L. R.
Wiley (1956) $10.25

## DIRECTORY OF PUBLISHERS

Academic Press, Inc.
111 Fifth Avenue
New York 3, New York

Addison-Wesley Publishing Co., Inc.
Reading, Massachusetts

American Electronics Co.
1203-05 Bryant Avenue
New York 59, New York

(Roy) A. N. Roy Publishers
30 East 74th Street
New York 21, New York

Bernards (Pub.) Ltd.
77 The Grampians
Western Gate,
London, W. 6

Bobbs-Merrill Co., Inc.
1720 East 38th Street
Indianapolis 6, Ind.
(see Howard W. Sams Co., Inc.)

British Book Service Ltd.
Kingswood House
1068 Broadview Avenue
Toronto 6, Canada

Cambridge University Press
32 East 57th Street
New York 22, New York

Catholic University of America Press
620 Michigan Avenue, N. E.
Washington 17, D.C.

Cleaver-Hume Press, Ltd.
Publishing Division
31 Wrights Lane
Kensington, London, W. 8

Constable & Co., Ltd.
10-12 Orange Street
London, W. C. 2

Coyne Electrical School
1501 Congress Parkway
Chicago 7, Illinois

D. VanNostrand Company, Inc.
120 Alexander Street
Princeton, New Jersey

Engineering Publishers
350 Morris Avenue — Box 2
Elizabeth, N. J.
(Books distributed by Reinhold)

Essential Books, Inc.
1600 Pollitt Drive
Fair Lawn, N. J.

(Ungar) Frederick Ungar Publishing Co.
131 East 23rd Street
New York 10, New York

Gernsback Library, Inc.
154 West 14th Street
New York 11, New York

Holt, Rinehart & Winston, Inc.
383 Madison Avenue
New York 17, New York

(Sams) Howard W. Sams Co., Inc.
1720 East 38th Street
Indianapolis 6, Ind.
(See Bobbs-Merrill Co., Inc.)

Iliffe Books Ltd.
Dorset House
Stamford Street
London, S. E. 1

Interscience Publishers, Inc.
250 5th Avenue
New York 1, New York

(Rider) John F. Rider, Publisher, Inc.
116 West 14th Street
New York 11, New York

(Wiley) John Wiley & Sons, Inc.
440 4th Avenue
New York 16, New York

Macmillan Co., Publishers
60 5th Avenue
New York 11, New York

McGraw-Hill Book Co., Inc.
330 West 42nd Street
New York 36, New York

Methuen & Co., Ltd.
36 Essex Street, Strand
London, W. C. 2

Mullard Overseas, Ltd.
Mullard House
Torrington Place
London, W. C. 1

Norman Price Publications, Ltd.
283 City Road
London, E. C. 1

Oxford University Press
1600 Pollitt Drive
Fair Lawn, New Jersey

Pergamon Press, Inc.
122 East 55th Street
New York 22, New York

Philip's Gloeilampenfabrieken,
Tech. & Scientific Lit. Dept.
Kastanjelaan,
Eindhoven, Netherlands

Philosophical Library, Inc.
15 East 40th Street
New York 16, New York

Prentice-Hall, Inc.
Route 9 W.
Englewood Cliffs, N. J.

Reinhold Publishing Corp.
430 Park Avenue
New York 22, New York

University of Pennsylvania Press
3436 Walnut Street
Philadelphia 4, Pa.

U. S. Govt. Printing Office
Washington 25, D. C.

Wehman Bros.
712 Broadway
New York 3, New York

**Additional Book Listings:**

*Basic Transistor Course*
Kenian, P. R.
Gernsback

*Fundamentals of Semiconductors*
Scroggie, M. G.
Gernsback $2.95

*How to Fix Transistor Radios and Printed Circuits* – 2 Vols.
Lane, L. C.
Gernsback $3.20 per Vol.
or $5.90 both.

*Servicing Transistor Radios*
D'Airo, L.
Gernsback $2.95

*Simplified Analysis and Application of the Junction Transistor as a Circuit Element*
Crib, B. F.
Philamon Laboratories, Inc.
(Westbury, L. I., N. Y.) (1957) $ .50

# TRANSISTOR SPECIFICATIONS

CHAPTER 22

## INTRODUCTION

This chapter consists of three parts:



Part 1 begins with a numerical type index of the more than 280 General Electric transistors and diodes as described in the Selection Charts that follow. The index gives the page where more complete electrical specifications can be found. Mechanical and physical specifications of any General Electric transistor or diode herein listed will be found in Part 2, Outline Drawings. Outline drawing numbers appear either directly under Selection Chart titles, or directly following the type number.

Part 3, the Registered JEDEC (Joint Electron Devices Engineering Council) Transistor Types Section has been completely revised and brought up to date. The chart contains over 1200 transistors numerically listed with pertinent electrical data given for each transistor. Comparable General Electric replacement type numbers along with outline drawing numbers will be found in the far right column.

Additional electrical and physical information for any General Electric Transistor or Diode is available on individual specification sheets (See Chapter 3). Such information may be obtained on request from the Semiconductor Products Department of the General Electric Company.

TO FIND GENERAL ELECTRIC — TURN TO PAGE

# TYPE INDEX



*See Preferred Types Chart on Page 122

# SILICON UNIJUNCTION TRANSISTORS[2]

See Outline Drawing No. 5

| Type | Interbase Resistance $R_{BB}$ $V_{BB}$=3v $I_E$=0 K ohms | Intrinsic Standoff Ratio $\eta$ $V_{BB}$=10v | Max. Emitter Reverse Current $I_{EO}$ $T_J$=150°C $V_{BE2}$ | $\mu a$ | Max. Peak Point Emitter Current $I_P$ $V_{BB}$=25v $\mu a$ | Max. Emitter Saturation Voltage $V_{E(SAT)}$ $I_E$=50 ma $V_{BB}$=10v Volts | Min. Emitter Reverse Voltage $T_J$<150°C Volts | Min. Base One Peak Pulse Voltage $V_{OB1}$ Volts | Comments |
|---|---|---|---|---|---|---|---|---|---|
| 2N489[1] | 4.7-6.8 | .51-.62 | *10* | 20 | 20 | 5.0 | 60 | – | Applications include the following:<br>• Frequency Dividers<br>• High Sensitivity Trigger Circuits<br>• Hybrid Multivibrator Circuits<br>• Lowest Cost SCR[3] Firing Circuits<br>• One Shot Multivibrators<br>• Pulse Generators<br>• Precision Voltage Sensing Circuits<br>• Regenerative Pulse Amplifiers<br>• Ring Counters<br>• Sawtooth Oscillators<br>• SCR[3] Phase Control Circuits<br>• SCR[3] Regulated Power Supplies<br>• Stable Relaxation Oscillators<br>• Stable Time Delay Circuits<br>• Staircase Wave Generators<br>• Solid State Time Delay Circuits |
| 2N489A | 4.7-6.8 | .51-.62 | *10* | 20 | 15 | 4.0 | 60 | 3.0 | |
| 2N489B | 4.7-6.8 | .51-.62 | *30* | 5 | 6 | 4.0 | 60 | 3.0 | |
| 2N490[1] | 6.2-9.1 | .51-.62 | *10* | 20 | 20 | 5.0 | 60 | – | |
| 2N490A | 6.2-9.1 | .51-.62 | *10* | 20 | 15 | 4.0 | 60 | 3.0 | |
| 2N490B | 6.2-9.1 | .51-.62 | *30* | 5 | 6 | 4.0 | 60 | 3.0 | |
| 2N491[1] | 4.7-6.8 | .56-.68 | *10* | 20 | 20 | 5.0 | 60 | – | |
| 2N491A | 4.7-6.8 | .56-.68 | *10* | 20 | 15 | 4.3 | 60 | 3.0 | |
| 2N491B | 4.7-6.8 | .56-.68 | *30* | 5 | 6 | 4.3 | 60 | 3.0 | |
| 2N492[1] | 6.2-9.1 | .56-.68 | *10* | 20 | 20 | 5.0 | 60 | – | |
| 2N492A | 6.2-9.1 | .56-.68 | *10* | 20 | 15 | 4.3 | 60 | 3.0 | |
| 2N492B | 6.2-9.1 | .56-.68 | *30* | 5 | 6 | 4.3 | 60 | 3.0 | |
| 2N493[1] | 4.7-6.8 | .62-.75 | *10* | 20 | 20 | 5.0 | 60 | – | |
| 2N493A | 4.7-6.8 | .62-.75 | *10* | 20 | 15 | 4.6 | 60 | 3.0 | |
| 2N493B | 4.7-6.8 | .62-.75 | *30* | 5 | 6 | 4.6 | 60 | 3.0 | |
| 2N494[1] | 6.2-9.1 | .62-.75 | *10* | 20 | 20 | 5.0 | 60 | – | |
| 2N494A | 6.2-9.1 | .62-.75 | *10* | 20 | 15 | 4.6 | 60 | 3.0 | |
| 2N494B | 6.2-9.1 | .62-.75 | *30* | 5 | 6 | 4.6 | 60 | 3.0 | |
| 2N1671 | 4.7-9.1 | .47-.62 | *30* | 12[4] | 25 | 5.0 | 30 | – | |
| 2N1671A | 4.7-9.1 | .47-.62 | *30* | 12[4] | 25 | 5.0 | 30 | 3.0 | |
| 2N1671B | 4.7-9.1 | .47-.62 | *30* | 5 | 6.0 | 5.0 | 30 | 3.0 | |
| 2N2160 | 4.0-12.0 | .47-.80 | *30* | 12[4] | 25 | – | 30 | 3.0 | |

**NOTES:** [1] Available as USAF TYPES (MIL-T-19500/75) [2] See also Chapter 13 [3] See General Electric *Silicon Controlled Rectifier Manual* [4] $T_J$ = 25°C
Test conditions in italics

# SILICON PLANAR PASSIVATED TRANSISTORS[1,4]

## TO-5 Package (See Outline Drawing No. 4)

| Type[3] | $h_{FE}$ $I_C$=150 ma $V_{CE}$=10v | Min. $V_{CER}$ $R_{BE}$≦10Ω $I_C$=100 ma | Max. $V_{CE}$ (SAT) $I_C$=150 ma $I_B$=15 ma | Max. $V_{BE}$ (SAT) $I_C$=150 ma $I_B$=15 ma | $h_{fe}$ f=1 kc $I_C$=1 ma $V_{CE}$=5v | MAXIMUM $I_{CBO}$ $V_{CB}$ $T_J$=150°C | MAXIMUM $I_{CBO}$ $V_{CB}$ $T_J$=150°C | $V_{EBO}$ $I_E$=100 μa | POWER DISS. $P_T$ Free Air @25°C | POWER DISS. $P_T$ Case Temp. @100°C | MINIMUM $h_{FE}$ $I_C$=10 ma $V_{CE}$=10v | MINIMUM $h_{FE}$ $I_C$=10 ma $V_{CE}$=10v $T_J$=−55°C | MINIMUM $h_{FE}$ $I_C$=0.1 ma $V_{CE}$=10v | MINIMUM $h_{FE}$ $I_C$=500 ma $V_{CE}$=10v | MINIMUM $h_{FE}$ $I_C$=1000 ma $V_{CE}$=10v | Comments | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Volts | Volts | Volts | Min. Max. | Volts | μa | Volts | Watts | Watts | | | | | | | |
| 2N696[7] | 20-60 | 40 | 1.5 | 1.3 | — | *30* | 100 | 5 | 0.6 | 1.0 | — | — | — | — | — | | |
| 2N697[7] | 40-120 | 40 | 1.5 | 1.3 | — | *30* | 100 | 5 | 0.6 | 1.0 | — | — | — | — | — | | |
| 2N698 | 20-60 | 80 | 5.0 | 1.3 | 15- | *75* | 15 | 7 | 0.8 | 1.7 | — | — | — | — | — | High Voltage 2N696 | |
| 2N699 | 40-120 | 80 | 5.0 | 1.3 | 35-100 | *60* | 200 | 5 | 0.6 | 1.0 | — | — | — | — | — | High Voltage 2N697. | |
| 2N1613 | 40-120 | 50 | 1.5 | 1.3 | 30-100 | *60* | 10 | 7 | 0.8 | 1.7 | 35 | 20 | 20 | 20 | — | Lower leakage 2N697. | |
| 2N1711 | 100-300 | 50 | 1.5 | 1.3 | 50-200 | *60* | 10 | 7 | 0.8 | 1.7 | 75 | 35 | 35 | 40 | — | High beta 2N1613. | |
| 2N1889 | 40-120 | 80 | 5.0 | 1.3 | 30-100 | *75* | 15 | 7 | 0.8 | 1.7 | 35 | 20 | 20 | — | — | High Voltage 2N1613. | |
| 2N1890 | 100-300 | 80 | 50 | 1.3 | 50-200 | | — | 7 | 0.8 | 1.7 | — | — | — | — | — | Higher voltage 2N1711. | |
| 2N1893 | 40-120 | 100 | 5.0 | 1.3 | 30-100 | *90* | 15 | 7 | 0.8 | 1.7 | 35 | 20 | 20 | — | — | High voltage 2N1613. | |
| 2N1983 | — | 30 | 0.25[6] | — | 70-210 | *30* | 200 | 5 | 0.6 | 1.0 | — | — | — | — | — | Very high beta for high gain, low noise amplifier circuits. | Industrial Types |
| 2N1984 | — | 30 | 0.25[6] | — | 35-100 | *30* | 200 | 5 | 0.6 | 1.0 | — | — | — | — | — | Amplifier Circuits. | |
| 2N1985 | — | 30 | 0.25[6] | — | 15-45 | *30* | 200 | 5 | 0.6 | 1.0 | — | — | — | — | — | Amplifier Circuits. | |
| 2N2049 | — | 50 | 0.4[5] | 0.8[5] | 75- | *60* | 10 | 7 | 0.8 | 1.7 | — | — | 60 | — | — | Very high beta for high gain, Low noise amplifier circuits. NF=3db Max. | |

# SILICON PLANAR EPITAXIAL PASSIVATED (PEP) TRANSISTORS[1,4]

## TO-5 Package (See Outline Drawing No. 4)

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N2192 | 100-300 | 40[2] | 0.35 | 1.3 | — | *30* | 15 | 5 | 0.8 | 1.6 | 75 | 35 | 15 | 35 | 15 | Similar to 2N1711, but lower $V_{CE\ (SAT)}$. |
| 2N2192A | 100-300 | 40[2] | 0.25 | 1.3 | — | *30* | 15 | 5 | 0.8 | 1.6 | 75 | 35 | 15 | 35 | 15 | |
| 2N2193 | 40-120 | 50[2] | 0.35 | 1.3 | — | *60* | 25 | 8 | 0.8 | 1.6 | 30 | 20 | 15 | 20 | 15 | Similar to 2N1613, but lower $V_{CE\ (SAT)}$. |
| 2N2193A | 40-120 | 50[2] | 0.25 | 1.3 | — | *60* | 25 | 8 | 0.8 | 1.6 | 30 | 20 | 15 | 20 | 15 | |
| 2N2194 | 20-60 | 40[2] | 0.35 | 1.3 | — | *30* | 25 | 5 | 0.8 | 1.6 | 15 | — | — | 12 | — | Similar to 2N696, but lower $V_{CE\ (SAT)}$. |
| 2N2194A | 20-60 | 40[2] | 0.25 | 1.3 | — | *30* | 25 | 5 | 0.8 | 1.6 | 15 | — | — | 12 | — | |
| 2N2195 | 20 Min. | 25[2] | 0.35 | 1.3 | — | *30* | 50 | 5 | 0.6 | 1.6 | — | — | — | — | — | Industrial types. |
| 2N2195A | 20 Min. | 25[2] | 0.25 | 1.3 | — | *30* | 50 | 5 | 0.6 | 1.6 | — | — | — | — | — | |
| 2N2243 | 40-120 | 80[2] | 0.35 | 1.3 | — | *60* | 15 | 7 | 0.8 | 1.6 | 30 | 20 | 15 | 15 | — | Similar to 2N1893 but lower $V_{CE(SAT.)}$ |
| 2N2243A | 40-120 | 80[2] | 0.25 | 1.3 | — | *60* | 15 | 7 | 0.8 | 1.6 | 30 | 20 | 15 | 15 | — | |

**NOTES:** Test Conditions in Italics.

(1) Typical $f_t$ for all types $\approx$ 130 Mc. (2) $V_{CEO}$

(3) Storage temperature on all types is −65 to +300° C. Operating junction temperature on all types is −65 to +200° C, except on 2N696, 2N697, and 2N699. On these types the rating is −65 to +175° C.

(4) For switching and amplifier applications. (5) $I_C$ = 10 ma, and $I_b$ = 1 ma. (6) $I_C$ = 5 ma. and $I_b$ = .5 ma.

(7) Also available in military types.

## SILICON PLANAR EPITAXIAL PASSIVATED (PEP) HIGH SPEED SWITCHES[3]

### TO-18 Package (See Outline Drawing No. 8)

| Type | $h_{FE}$ Min. @ $I_C$ ma | $h_{FE}$ Max. @ $V_{CE}$ Volts | MINIMUM $V_{CER}$ Volts @ $I_C$ ma @ $R_{BB}$ ohms | MINIMUM $V_{CEO}$ Volts @ $I_C$ ma | MINIMUM $V_{EBO}$ Volts @ $I_E$ μa | MAXIMUM $V_{BE}$ (SAT) $I_C$=10 ma $I_B$=1 ma Volts | MAXIMUM $V_{CE}$ (SAT) $I_C$=10 ma $I_B$=1 ma Volts | MAXIMUM $I_{CBO}$ $T_J$=150°C @ $V_{CB}$ Volts | MAXIMUM $I_{CBO}$ $T_J$=150°C @ $V_{CB}$ μa | $t_{on}$ nsec | $t_{off}$ nsec | $C_{ob}$ @ $V_{CB}$ pf | $C_{ob}$ @ $V_{CB}$ Volts | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N706 | 10 | 1.0 | 30 10 | — | 100 | 0.9 | 0.6 | 15 | | — | — | 6 | 10 | Economy Units. |
| | 20 Min. | | 20 | | 3 | | | | 30 | | | | | |
| 2N706A | 10 | 1.0 | 10 10 | 10 | 10 | 0.9 | 0.6 | 15 | | 40 | 75 | 5 | 5 | Economy units. High speed. |
| | 20-60 | | 20 | 15 | 5 | | | | 30 | | | | | |
| 2N708 | 10 | 1.0 | 30 10 | 30 | 10 | 0.8 | 0.4 | 20 | | 40 | 70 | 6 | 10 | Low leakage current. High speed. |
| | 30-120 | | 20 | 15 | 5 | | | | 15 | | | | | |
| 2N753 | 10 | 1.0 | 10 10 | 10 | 10 | 0.9 | 0.6 | 15 | | 40 | 75 | 5 | 5 | High beta. High speed. |
| | 40-120 | | 20 | 15 | 5 | | | | 30 | | | | | |
| 2N834 | 10 | 1.0 | 10μa 0 | — | 100 | 0.9 | 0.25 | 20 | | 35 | 75 | 4 | 10 | Low saturation voltage. |
| | 25 Min. | | 30[1] | — | 5 | | | | 30 | | | | | |
| 2N914 | 10 | 1.0 | 30 10 | 30 | 10 | 0.8 | 0.25 | 20 | | 40 | 40 | 6 | 10 | Ultra-high speed. Low saturation voltage. |
| | 30-120 | | 20 | 15 | 5 | | | | 15 | | | | | |

## SILICON PLANAR PASSIVATED AMPLIFIERS — TYPICAL $f_t \approx 300$ MC.

### TO-18 Package (See Outline Drawing No. 8)

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N759 | 1.0 | 5.0 | — | 1.0 | 100 | — | 1.0 | 30 | | — | — | 8 | 5 | These devices are well suited for applications where the 2N335 and 2N336 have been used and higher frequency devices or smaller packages are required. |
| | 36-90[2] | | | 45 | 8 | | | | 10 | | | | | |
| 2N760 | 1.0 | 5.0 | — | 1.0 | 100 | — | 1.0 | 30 | | — | — | 8 | 5 | |
| | 76-333[2] | | | 45 | 8 | | | | 10 | | | | | |
| 2N915 | 10 | 5.0 | — | 10 | 100 | 0.9 | 1.0 | 60 | | — | — | 3.5 | 10 | These devices are intended for non-saturating switching circuits, amplifier and and oscillator circuits. |
| | 40-160 | | | 50 | 5 | | | | 30 | | | | | |
| 2N916 | 10 | 1.0 | — | 30 | 10 | 0.9 | 0.5 | 15 | | — | — | 6 | 5 | |
| | 50-200 | | | 25 | 5 | | | | 10 | | | | | |

# SILICON PLANAR PASSIVATED SWITCHES[3]

## TO-18 Package (See Outline Drawing No. 8)

| | | | | | $I_C$=150 ma $I_B$=15 ma | $I_C$=150 ma $I_B$=15 ma | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N717 | *150* 20-60 | *10* | *100* 40 | *10* | — | — | *1 ma* 5 | 1.3 | 1.5 | *30* 100 | — | — | 35 | 10 | Electrically equivalent to 2N696. |
| 2N718 | *150* 40-120 | *10* | *100* 40 | *10* | — | — | *1 ma* 5 | 1.3 | 1.5 | *30* 100 | — | — | 35 | 10 | Electrically equivalent to 2N697. |
| 2N718A | *150* 40-120 | *10* | *100* 50 | *10* | — | — | *100* 7 | 1.3 | 1.5 | *60* 10 | — | — | 25 | 10 | Electrically equivalent to 2N1613. |
| 2N719 | *150* 20-60 | *10* | *100* 80 | *10* | — | — | *1 ma* 5 | 1.3 | 5 | *60* 200 | — | — | 20 | 10 | Electrically equivalent to 2N698. |
| 2N719A | *150* 20-60 | *10* | *100* 80 | *10* | *30* 60 | | *100* 7 | 1.3 | 5 | *75* 15 | — | — | 15 | 10 | Electrically equivalent to 2N698. |
| 2N720 | *150* 40-120 | *10* | *100* 80 | *10* | — | — | *1 ma* 5 | 1.3 | 5 | *60* 200 | — | — | 20 | 10 | Electrically equivalent to 2N699. |
| 2N720A | *150* 40-120 | *10* | *100* 100 | *10* | *30* 80 | | *100* 7 | 1.3 | 5 | *90* 15 | — | — | 15 | 10 | Electrically equivalent to 2N1893. |
| 2N956 | *150* 100-300 | *10* | *100* 50 | *10* | — | — | *100* 7 | 1.3 | 1.5 | *60* 15 | — | — | 25 | 10 | Electrically equivalent to 2N1711. |

**NOTES:** Test conditions in Italics. (1) $V_{CES}$ (2) $h_{fe}$ @ 1 Kc. (3) Typical $f_t$ for all types ≈ 350 mc.

### POWER DISSIPATION

$P_T$ (Free Air @ 25°C)

| 300 MW | 360 MW | 400 MW | 500 MW |
|---|---|---|---|
| 2N706 | 2N708 | 2N717 | 2N718A |
| 2N706A | 2N914 | 2N718 | 2N720A |
| 2N719A | 2N915 | 2N719 | 2N759 |
| 2N753 | 2N916 | 2N720 | 2N760 |
| 2N834 | | | 2N956 |

## SILICON MESA NPN POWER TRANSISTORS[5]

| Type | Drwg. No. | $h_{FE}$ $V_{CE}$=10v $I_C$=200 ma | MINIMUM $V_{CEO}$ $I_C$=250μa Volts | MINIMUM $V_{CEX}$ $I_C$=250μa $V_{BE}$=−1.5v $T_J$=150°C Volts | MAXIMUM $I_{CBO}$ $V_{CB}$=30v $T_J$=150°C μa | MAXIMUM Power $P_T$ Free Air @25°C Watts | MAXIMUM Dissipation $P_T$ Case Temp @25°C Watts | MAXIMUM $V_{CE\ (SAT)}$ $I_C$=200 ma $I_B$=40 ma Volts | Comments |
|---|---|---|---|---|---|---|---|---|---|
| 2N497[6] | 2 | 12-36 | 60 | | 250 | 0.8 | 4 | 5 | |
| 2N497A | 2 | 12-36 | 60 | | 250 | 1.0 | 5 | 2 | Applications include the following:<br>• Audio Amplifiers<br>• Blocking Oscillators<br>• DC to AC Inverters<br>• Linear Amplifiers<br>• Magnetic Tape Bias and Erase Oscillators<br>• Power Oscillators<br>• Power Switching Circuits<br>• Pulse Amplifiers<br>• Regulated Power Supplies<br>• Servo Amplifiers<br>• Servo Drivers<br>• Solenoid Drivers |
| 2N498[6] | 2 | 12-36 | 100 | | 250 | 0.8 | 4 | 5 | |
| 2N498A | 2 | 12-36 | 100 | | 250 | 1.0 | 5 | 2 | |
| 2N656[6] | 2 | 30-90 | 60 | | 250 | 0.8 | 4 | 5 | |
| 2N656A | 2 | 30-90 | 60 | | 250 | 1.0 | 5 | 2 | |
| 2N657[6] | 2 | 30-90 | 100 | | 250 | 0.8 | 4 | 5 | |
| 2N657A | 2 | 30-90 | 100 | | 250 | 1.0 | 5 | 2 | |
| 2N2017 | 2 | 50-200 | 60 | | 250 | 1.0 | 5 | 2 | |
| 2N2106 | 2 | 12-36 | 60[1] | | 200[2] | 1.0 | — | 5 | |
| 2N2107 | 2 | 30-90 | 60[1] | | 200[2] | 1.0 | — | 2 | |
| 2N2108 | 2 | 75-200 | 60[1] | | 200[2] | 1.0 | — | 2[3] | |

| | | | | | | | Case Temp.[4] @100°C | |
|---|---|---|---|---|---|---|---|---|
| 2N2196 | 9 | 30-90 | 60[1] | 80 | 250 | 2.0 | 10 | 2 |
| 2N2197 | 9 | 75-200 | 60[1] | 80 | 250 | 2.0 | 10 | 2[3] |
| 2N2201 | 9 | 30-90 | 100 | 120 | 200 | 2.0 | 10 | 1.7 |
| 2N2202 | 10 | 30-90 | 100 | 120 | 200 | 1.0 | 10 | 1.7 |
| 2N2203 | 11 | 30-90 | 100 | 120 | 200 | 1.0 | 10 | 1.7 |
| 2N2204 | 12 | 30-90 | 100 | 120 | 200 | 1.0 | 10 | 1.7 |
| 7B1 | 9 | 12-36 | 60 | 80 | 200 | 2.0 | 10 | 1.7 |
| 7B2 | 9 | 30-90 | 60 | 80 | 200 | 2.0 | 10 | 1.7 |
| 7B3 | 9 | 12-36 | 100 | 120 | 200 | 2.0 | 10 | 1.7 |
| 7C1 | 10 | 12-36 | 60 | 80 | 200 | 1.0 | 10 | 1.7 |
| 7C2 | 10 | 30-90 | 60 | 80 | 200 | 1.0 | 10 | 1.7 |
| 7C3 | 10 | 12-36 | 100 | 120 | 200 | 1.0 | 10 | 1.7 |
| 7D1 | 11 | 12-36 | 60 | 80 | 200 | 1.0 | 10 | 1.7 |
| 7D2 | 11 | 30-90 | 60 | 80 | 200 | 1.0 | 10 | 1.7 |
| 7D3 | 11 | 12-36 | 100 | 120 | 200 | 1.0 | 10 | 1.7 |
| 7E1 | 12 | 12-36 | 60 | 80 | 200 | 1.0 | 10 | 1.7 |
| 7E2 | 12 | 30-90 | 60 | 80 | 200 | 1.0 | 10 | 1.7 |
| 7E3 | 12 | 12-36 | 100 | 120 | 200 | 1.0 | 10 | 1.7 |
| 7F1 | 13 | 12-36 | 60 | 80 | 200 | 1.0 | 4.0 | 1.7 |
| 7F2 | 13 | 30-90 | 60 | 80 | 200 | 1.0 | 4.0 | 1.7 |
| 7F3 | 13 | 12-36 | 100 | 120 | 200 | 1.0 | 4.0 | 1.7 |
| 7F4 | 13 | 30-90 | 100 | 120 | 200 | 1.0 | 4.0 | 1.7 |

(Same applications as above but at higher power conditions)

**NOTES:** (1) $V_{CER}$ ($I_C$ = 16 ma, R = 1K) (2) $T_J$ = 125°C (3) $I_B$ = 10 ma (4) See outline drawing for attachment to heatsink. (5) Typ. $f_t$ for all types ≈ 15 MC
(6) Also available in military types.

# SILICON GROWN DIFFUSED NPN TRANSISTORS

## TO-5 Package (See Outline Drawing No. 4)

| Type | $h_{fe}$ $V_{CB}$=5 v $I_E$=1 ma f=1 kc | MINIMUM $BV_{CBO}$ $I_{CBO}$= 50 μa $I_E$=0 volts | MAXIMUM $I_{CBO}$ $V_{CB}$=30 v $I_E$=0 $T_A$=250C° μa | TYPICAL $f_{hfb}$ $V_{CB}$=5 v $I_E$=1 ma mc | MAXIMUM Power Diss. mw | TYPICAL $h_{FE}$ $V_{CE}$=5 v $I_C$=1 ma | Comments |
|---|---|---|---|---|---|---|---|
| 4C28 | 9-19 | 40(4) | 2.0 | 12 | 150 | 15 | |
| 4C29 | 18-40 | 40(4) | 2.0 | 12 | 150 | 30 | |
| 4C30 | 37-80 | 40(4) | 2.0 | 12 | 150 | 55 | |
| 4C31 | 76-300 | 40 | 2.0 | 12 | 150 | 115 | |
| 4D20 | See $h_{FE}$ | 40(4) | 1.0(8) | — | 150 | 15-50(10) | Applications include the following:<br>• Audio amplifiers<br>• Low cost industrial switches |
| 4D21 | See $h_{FE}$ | 40(4) | 1.0(8) | — | 150 | 40-135(10) | |
| 4D22 | See $h_{FE}$ | 40(4) | 1.0(8) | — | 150 | 120-250(10) | |
| 4D24 | See $h_{FE}$ | 15(5) | 1.0(7) | — | 125 | 15-50(10) | |
| 4D25 | See $h_{FE}$ | 15(5) | 1.0(7) | — | 125 | 40-135(10) | |
| 4D26 | See $h_{FE}$ | 15(5) | 1.0(7) | — | 125 | 120-250(10) | |
| 2N332(12) | 9-22 | 45 | 1.0 | 10 | 150 | 14 | |
| 2N332A | 9-22 | 45 | 0.5 | 10 | 500 | 16 | Applications include the following:<br>• Audio Amplifiers<br>• Astable Oscillators<br>• Chopper Circuits<br>• Flip-flop Circuits<br>• Logic Circuits<br>• RF Amplifiers |
| 2N333(12) | 18-44 | 45 | 1.0 | 12 | 140 | 31 | |
| 2N333A | 18-44 | 45 | 0.5 | 11 | 500 | 27 | |
| 2N334(12) | 18-90 | 45 | 1.0 | 13 | 150 | 38 | |
| 2N334A | 18-90 | 45 | 0.5 | 12 | 500 | 36 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 2N335[13] | 37-90 | 45 | 1.0 | 14 | 150 | 56 | |
| 2N335A | 37-90 | 45 | 0.5 | 13 | 500 | 45 | |
| 2N335B | 37-90 | 60 | 0.5 | 13 | 500 | 45[12] | |
| 2N336 | 76-333 | 45 | 1.0 | 15 | 150 | 100 | |
| 2N336A | 76-333 | 45 | 0.5 | 15 | 500 | 75 | |
| 2N337[13] | 55[1] | 45 | 1.0[6] | 30 | 125 | 55[11] | (Same comments as above) |
| 2N337A | 55[2] | 45 | 0.5 | 30[9] | 500 | 35[11] | |
| 2N338[13] | 99[1] | 45 | 1.0[6] | 45[9] | 125 | 99[11] | |
| 2N338A | 99[2] | 45 | 0.5 | 45[9] | 500 | 75[11] | |
| 2N1277 | 18-44 | 40 | 1.0 | 30[9] | 150 | 20[11] | |
| 2N1278 | 37-90 | 40 | 1.0 | 30[9] | 150 | 33[11] | |
| 2N1279 | 76-333 | 40 | 1.0 | 34[9] | 150 | 80[11] | |

**NOTES:**

(1) Typical $h_{fe}$ @ $V_{CB}=20$ V, $I_E=1$ ma.
(2) Typical $h_{fe}$ @ $V_{CB}=20$ V, $I_C=1$ ma.
(4) $I_{CBO}=100$ $\mu$a, $I_E=0$.
(5) $BV_{CEO}$ @ $I_{CBO}=100$ $\mu$a.
(6) $V_{CB}=20$ V, $I_E=0$
(7) $V_{CB}=15$ V, $I_E=0$
(8) $V_{CB}=12$ V, $I_E=0$
(9) $V_{CB}=20$ V, $I_E=1$ ma.
(10) Pulsed measurement.
(11) $V_{CE}=5$V, $I_C=10$ ma.
(12) $V_{CE}=10$ V, $I_C=5$ ma.
(13) Also available in military types.

# SILICON NPNP LOW CURRENT CONTROLLED SWITCHES[4]

## TO-5 Package Isolated Case (See Outline Drawing No. 6)

| | | | | | | MAX. ANODE RATINGS | | | | MAX. GATE RATINGS | | | GATE INPUT TO FIRE | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Type | Anode Blocking Voltage | Continuous DC Forward Current 100°C Ambient | Peak Recurrent Forward Current 100 μsec 100°C | Peak Gate Current | Dissipation[5] | $I_B$ $V_{AC}$=+40v $R_{AC}$=10K, 150°C | $I_R$ $V_{AC}$=−40v $R_{AC}$=10K, 150°C | $V_F$ $I_A$=50 ma | $I_H$ $V_{AC}$=40v, $R_{AC}$=10K | $I_{GC}$ $V_{GC}$=−2.5v | $I_{GA}$ $V_{GA}$=40v | Max. $I_{GFA}$ $V_{AC}$=40v, $R_{AC}$=0, $R_L$=800 ohms | $V_{GFA}$ $V_{AC}$=40v, $R_{AC}$=0, $R_L$=800 ohms | Max. $I_{GFC}$ $V_{AC}$=40v, $R_L$=800 ohms | $V_{GFC}$ $V_{AC}$=40v, $R_L$=800 ohms |
| | Volts | ma | amp | ma | mw | μa | μa | Volts | ma | μa | μa | ma | Volts | μa | Volts |
| 3N58[1] | 40 | 100 | 0.5 | 50 | 300 | 20 | 20 | 1.5 | 1.5 | 20 | | | | 1.0 | 0.4 to 0.65 |
| 3N59[2] | 40 | 100 | 0.5 | 50 | 300 | 20 | | 1.5 | 1.5 | | 20 (150°C) | 1.5 | −0.6 to −1.2 | | |
| 3N60[3] | 40 | 100 | 0.5 | 50 | 300 | 20 | 20 | 1.5 | 1.5 | 20 | 0.2 (25°C) | 1.5 | −0.6 to −1.2 | 1.0 | 0.4 to 0.65 |

**NOTES:**

(1) For this characterization $G_A$ is electrically open, This corresponds to the conventional SCR[6] configuration.
(2) For this characterization, $G_C$ is connected to C. This correspnds to the complementary SCR[6] configuration.
(3) This characterization is for SCR, complementary SCR[6], and Binistor circuit configurations. The 3N60 meets all specifications for the 3N58 and 3N59.
(4) See also Chapter 19.
(5) Derate at 2.4 mw per °C.
(6) See General Electric *Silicon Controlled Rectifier Manual*.

# GERMANIUM MESA TRANSISTORS

## TO-18 Package (See Outline Drawing No. 8)

| Type | $h_{FE}$ @Ic ma | @$V_{CE}$ Volts | MAXIMUM Ic ma | Diss. (1) mw | MINIMUM $V_{CBO}$ Volts | $V_{CES}$ Volts | $V_{EBO}$ Volts | $I_{CBO}$ μa | MAXIMUM $V_{CE(SAT)}$ Volts @Ic ma | @$I_B$ ma | $V_{CE(SAT)}$ Volts @Ic ma | @$I_B$ ma | $V_{BE}$ Volts @Ic ma | @$I_B$ ma | MAXIMUM $t_{on}$ nsec | $t_{off}$ nsec | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N705(2) | *10* 25 min. | *.3* | 50 | 150 | 15 | 15 | 3.5 | 3 | *10* .30 | *.4* | — | — | *10* .34-.44 | *.4* | 75 | 200 | Low current, relatively slow speed, economy units, relatively high saturation voltage, high voltage. |
| 2N710 | *10* 25 min. | *.5* | 50 | 150 | 15 | 15 | 2.0 | 3 | *10* .50 | *.4* | — | — | *10* .34-.50 | *.4* | 75 | 200 | |
| 2N711 | *10* 20-250 | *.5* | 100 | 150 | 12 | 12 | 1.0 | 3 | *10* .50 | *.5* | — | — | *10* .35-.50 | *.4* | 100 | 350 | Low current, relatively slow speed, economy units, relatively high saturation voltage, low voltage, low beta. |
| 2N711A | *10* 25-150 | *.5* | 100 | 150 | 15 | 14 | 1.5 | 1.5 | *10* .30 | *.5* | *50* .55 | *2* | *10* .34-.50 | *.4* | 75 | 230 | Economy units, relatively slow, medium current, low $I_{CBO}$. |
| 2N711B | *10* 30-150 | *.5* | 100 | 150 | 18 | 15 | 2.0 | 1.5 | *10* .25 | *.4* | *50* .45 | *2* | *10* .34-.45 | *.4* | 75 | 200 | Low $I_{CBO}$ relatively slow speed, medium current, higher beta. |
| 2N725 | *10* 20 min. | *.5* | 50 | 150 | 15 | 12 | 2.0 | 3 | *10* .50 | *.5* | — | — | *15* .34-.60 | *1.2* | 75 | 200 | Low current, relatively slow speed, economy units, relatively high saturation voltage, lower voltage, low beta. |
| 2N781 | *10* 25 min. | *.22* | 200 | 150 | 15 | 15 | 2.5 | 3 | *10* .16 | *1* | *100* .25 | *10* | *10* .34-.44 | *.4* | 60 | 70 | High current, very low saturation, high voltage, medium to high speed. |
| 2N782 | *10* 20 min. | *.25* | 200 | 150 | 12 | 12 | 1.0 | 3 | *10* .20 | *1* | *100* .45 | *10* | *10* .34-.50 | *.4* | 75 | 110 | High current, medium saturation, lower voltage, medium speed. |
| 2N828 | *10* 25 min. | *.3* | 200 | 150 | 15 | 15 | 2.5 | 3 | *10* .25 | *1* | *50* .25 | *5* | *10* .34-.44 | *1* | 70 | 100 | High current, very low saturation, high voltage, medium to high speed. |
| 2N960 | *10* 20 min. | *1* | 150 | 150 | 15 | 15 | 2.5 | 3 | *10* .20 | *1* | *100* .70 | *10* | *10* .30-.50 | *1* | 50 | 90 | Medium current, high speed, low beta, high voltage. |
| 2N961 | *10* 20 min. | *1* | 150 | 150 | 12 | 12 | 2.0 | 3 | *10* .20 | *1* | *100* .70 | *10* | *10* .30-.50 | *1* | 50 | 90 | High speed, low beta, lower voltage, medium current. |
| 2N962 | *10* 20 min. | *1* | 150 | 150 | 12 | 12 | 1.25 | 3 | *10* .20 | *1* | *100* .70 | *10* | *10* .30-.50 | *1* | 50 | 90 | High speed, high beta, high voltage, medium current. |
| 2N964 | *10* 40 min. | *1* | 150 | 150 | 15 | 15 | 2.5 | 3 | *10* .18 | *1* | *100* .60 | *10* | *10* .30-.50 | *1* | 50 | 90 | |
| 2N965 | *10* 40 min. | *1* | 150 | 150 | 12 | 12 | 2.0 | 3 | *10* .18 | *1* | *100* .60 | *10* | *10* .30-.50 | *1* | 50 | 90 | High speed, high beta, lower voltage, medium current. |
| 2N966 | *10* 40 min. | *1* | 150 | 150 | 12 | 12 | 1.25 | 3 | *10* .18 | *1* | *100* .60 | *10* | *10* .30-.50 | *1* | 50 | 90 | |
| 2N994 | *10* 45-140 | *.25* | 150 | 200 | 15 | 15 | 4.0 | 3 | *10* .18 | *.4* | *100* .45 | *8* | *10* .34-.44 | *.4* | 35 | 45 | Very high speed, high dissipation, high voltage, medium current, high beta, low saturation. |

**NOTES:** Test Conditions in Italics. (1) 25°C Ambient Free Air. (2) Also available in military types.

# GERMANIUM ALLOY PNP TRANSISTORS[1]

| Types | Drwg. No. | $h_{FE}$ $V_{CE}$=1v $I_C$=20 ma | TYPICAL $f_{\alpha fb}$ mc | MINIMUM $BV_{CER}$ @ $I_C$=600 μa $R_{BE}$=10K Volts | MAXIMUM $I_{CBO}$ @ $V_{CB}$ μa | Volts | Power Diss. mw | Comments |
|---|---|---|---|---|---|---|---|---|
| 2N43A[10] | 1 | 34-65 | 1.3 | 30 | 16 | 45 | 240 | See 2N525. |
| 2N44A[10] | 1 | 18-43 | 1.0 | 30 | 16 | 45 | 240 | See 2N524. |
| 2N45 | 1 | 11-23 | 1.0 | 30 | 16 | 45 | 155 | See 2N508, 2N1175 and 2N1413 series. Not recommended for new designs. |
| 2N186A | 1 | 19-31 | 0.8 | 25 | 16 | 25 | 200 | |
| 2N187A | 1 | 25-42 | 1.0 | 25 | 16 | 25 | 200 | |
| 2N188A | 1 | 34-65 | 1.2 | 25 | 16 | 25 | 200 | |
| 2N189 | 1 | 25-42 | 0.8 | 25 | 16 | 25 | 200 | |
| 2N190 | 1 | 34-65 | 1.0 | 25 | 16 | 25 | 200 | |
| 2N191 | 1 | 53-121 | 1.2 | 25 | 16 | 25 | 200 | |
| 2N192 | 1 | 72-176 | 1.5 | 25 | 16 | 25 | 200 | |
| 2N241A | 1 | 50-125 | 1.3 | 25 | 16 | 25 | 200 | |
| 2N319 | 2 | 25-42 | 2.0 | 20 | 16 | 25 | 225 | Audio driver and audio output. |
| 2N320 | 2 | 34-65 | 2.5 | 20 | 16 | 25 | 225 | |
| 2N321 | 2 | 53-121 | 3.0 | 20 | 16 | 25 | 225 | |
| 2N322 | 2 | 34-65 | 3.0 | 16 | 16 | 16 | 200 | |
| 2N323 | 2 | 53-121 | 3.5 | 16 | 16 | 16 | 200 | |
| 2N324 | 2 | 72-198 | 4.0 | 16 | 16 | 16 | 200 | |
| 2N394 | 2 | 20-150[2] | 7.0 | 15 | 6 | 10 | 150 | Medium speed switch. |
| 2N394A | 2 | 30-120[2] | 7.0 | 15 | 6 | 12 | 150 | Medium speed switch and audio amplifier. |
| 2N395 | 2 | 20-150[2] | 6.0 | 15 | 6 | 15 | 200 | Medium speed switch. |
| 2N396 | 2 | 30-150[2] | 8.0 | 20 | 6 | 20 | 200 | Industrial/Military-medium beta, medium speed switch. |
| 2N396A[10] | 2 | 30-150[2] | 8.0 | 20[8] | 6 | 20 | 200 | Same as 2N396. Mil-S-19500/64B. |
| 2N397 | 2 | 40-150[2] | 12.0 | 15 | 6 | 15 | 200 | Industrial/Military-medium speed switch. |
| 2N404[10] | 2 | — | 8.0 | 24[6] | 5 | 12 | 150 | Medium speed switch—wide beta spread. MIL-T 19500/20. |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 2N404A | 2 | — | 8.0 | 35[6] | 5 | *20* | 150 | Same as 2N404. |
| 2N413 | 2 | 20-100[2] | 6.0 | 18[5] | 5 | *12* | 150 | General purpose medium speed switch. |
| 2N414 | 2 | 30-120[2] | 7.0 | 15[5] | 5 | *12* | 150 | Same as 2N413. |
| 2N427 | 2 | 40-80[3] | 10.0 | 15[5] | 4 | *1.5* | 150 | Medium speed switch and amplifier. Narrow beta spread. |
| 2N428[10] | 2 | 60 Min.[3] | 15.0 | 12[5] | 4 | *1.5* | 150 | Medium speed switch. High beta. MIL-S-19500/44B. |
| 2N461 | 2 | 32-199[4] | 4.0 | 35[9] | 15 | *45* | 200 | General purpose. |
| 2N508 | 2 | 99-198 | 4.5 | 16 | 7 | *16* | 200 | High gain, low noise preamplifiers. |
| 2N524 | 2 | 25-42 | 2.5 | 30 | 10 | *30* | 225 | Military/industrial.—Audio amplifier and medium speed switch. Specified $h_{FE}$ hold-up, high temperature $I_{CO}$, and low temperature $h_{FE}$. Guaranteed reliability index. MIL-T-19500/60B. |
| 2N525 | 2 | 34-65 | 3.0 | 30 | 10 | *30* | 225 | |
| 2N526[10] | 2 | 53-90 | 3.5 | 30 | 10 | *30* | 225 | |
| 2N527 | 2 | 72-121 | 4.0 | 30 | 10 | *30* | 225 | |
| 2N1057 | 1 | 34-90 | 1.3 | 30[7] | 16 | *45* | 240 | See 2N1924 series. Not recommended for new designs. |
| 2N1097 | 2 | 34-90 | 3.0 | 16 | 16 | *16* | 200 | Audio driver and audio output. |
| 2N1098 | 2 | 25-90 | 3.0 | 16 | 16 | *16* | 200 | |
| 2N1144 | 1 | 34-90 | 1.3 | 16 | 16 | *16* | 175 | See 2N1097, 2N1098, or 2N1413 series. Not recommended for new designs. |
| 2N1145 | 1 | 25-90 | 1.3 | 16 | 16 | *16* | 175 | |
| 2N1175 | 2 | 70-140 | 4.0 | 25 | 12 | *30* | 200 | General purpose industrial and consumer preamplifier. |
| 2N1175A | 2 | 70-140 | 4.0 | 25 | 12 | *30* | 200 | General purpose industrial and consumer, high gain, low noise preamplifiers. Guaranteed noise figure. |
| 2N1303[10] | 2 | 20 Min.[2] | 7.0 | 25[6] | 6 | *25* | 150 | Medium speed switch. MIL-S-19500/126A. |
| 2N1305[10] | 2 | 40-200[2] | 8.0 | 20[6] | 6 | *25* | 150 | |
| 2N1307[10] | 2 | 60-300[2] | 12.0 | 15[6] | 6 | *25* | 150 | |
| 2N1413 | 2 | 25-42 | 3.2 | 25 | 12 | *30* | 200 | General purpose industrial and consumer audio amplifier and medium speed switch. |
| 2N1414 | 2 | 34-65 | 3.6 | 25 | 12 | *30* | 200 | |
| 2N1415 | 2 | 53-90 | 4.0 | 25 | 12 | *30* | 200 | |
| 2N1614 | 1 | 18-43 | 1.3 | 40[8] | 25 | *65* | 240 | See 2N1924 series. Not recommended for new designs. |
| 2N1924 | 2 | 34-65 | 3.0 | 40 | 10 | *45* | 225 | Military/industrial audio amplifier and medium speed switch. High voltage, specified $h_{FE}$ hold-up, low temperature $h_{FE}$, and high temperature $I_{CO}$. Guaranteed reliability index. |
| 2N1925 | 2 | 53-90 | 3.5 | 40 | 10 | *45* | 225 | |
| 2N1926 | 2 | 72-121 | 4.0 | 40 | 10 | *45* | 225 | |

**NOTES:** Test conditions in Italics.

(1) All specs. at 25°C unless noted otherwise

(2) $V_{CE}$ = 1V, $I_C$ = 10 Ma.

(3) $V_{CE}$ = .25V, $I_B$ = 1 Ma.

(4) $V_{CE}$ = 5V, $I_E$ = 1 ma, f = 1 Kc.

(5) $BV_{CEO}$.

(6) $V_{RT}$.

(7) $V_{RT}$ = 45V.

(8) $V_{RT}$ = 60 V.

(9) R = 1 K.

(10) Also available as military types.

# GERMANIUM ALLOY NPN TRANSISTORS

## TO-5 Package (See Outline Drawing No. 2)

| Type | $h_{FE}$ $I_C$=10 ma $V_{CE}$=1v | TYPICAL $f_{hfb}$ mc | MINIMUM $BV_{CER}$ R=10 K $I_C$=600 μa Volts | MAXIMUM $I_{CBO}$ @$V_{CB}$=25v μa | MAXIMUM Power Diss. mw | Comments |
|---|---|---|---|---|---|---|
| 2N377 | 20-60(5) | 6 | 20(8) | 20(3) | 150 | Not recommended for new designs. See 2N634A. |
| 2N385 | 30-110(4) | 6 | 25(9) | 35 | 150 | Not recommended for new designs. See 2N634A. |
| 2N388 | 60-180(2) | 12 | 20(8) | 10 | 150 | Medium Speed Switch. Guaranteed Maximum Switching Speed. |
| USN2N388 | 60-180(2) | 12 | 20(8) | 10 | 150 | Medium Speed Switch To MIL-T-19500/65. |
| 2N634 | 15 Min.(1) | 8 | 20 | 10(3) | 150 | Not recommended for new designs. See 2N634A. |
| 2N634A | 40-120 | 8 | 20(10) | 6 | 150 | Medium speed switch and audio amplifier having close control of $h_{FE}$ from 10 ma to 200 ma, guaranteed minimum $h_{FE}$ at −55°C, maximum $I_{CBO}$ at 71°C. |
| 2N635 | 25 Min.(1) | 12 | 20 | 10(3) | 150 | Not recommended for new designs. See 2N635A. |
| 2N635A | 80-240 | 12 | 20(10) | 6 | 150 | Medium speed switch and audio amplifier having close control of $h_{FE}$ from 10 ma to 200 ma, guaranteed minimum $h_{FE}$ at −55°C, maximum $I_{CBO}$ at 71°C. |
| 2N636 | 35 Min.(1) | 17 | 15 | 10(3) | 150 | Not recommended for new designs. See 2N636A. |
| 2N636A | 100-300 | 17 | 15(10) | 6 | 150 | Medium speed switch and audio amplifier having close control of $h_{FE}$ from 10 ma to 200 ma, guaranteed minimum $h_{FE}$ at −55°C, maximum $I_{CBO}$ at 71°C. |
| 2N1302 | 20 Min. | 4.5 | 25(8) | 6 | 150 | Medium Speed Switch. |
| 2N1304 | 40-200 | 8 | 20(11) | 6 | 150 | Medium Speed Switch. |
| 2N1306 | 60-300 | 12 | 15(11) | 6 | 150 | Medium Speed Switch. |
| 2N1308(12) | 80 Min. | 17 | 15(11) | 6 | 150 | Medium Speed Switch. |
| 2N1605 | 42 Min.(7) | 16 | 24(11) | 5(6) | 150 | Medium Speed Switch. |

**NOTES:**

(1) $I_C$=200 ma, $V_{CE}$=.75 V.
(2) $I_C$=30 ma, $V_{CE}$=.5 V.
(3) $V_{CB}$=20 V.
(4) $I_C$=30 ma, $V_{CE}$=.75 V.
(5) $I_C$=30 ma, $V_{CE}$=1.0 V.
(6) $V_{CB}$=12 V.
(7) $I_C$=20 ma, $V_{CE}$=.25 V.
(8) $I_C$=50μa.
(9) $I_C$=400 μa.
(10) $I_C$=100 μa.
(11) $V_{RT}$.
(12) Also available in military types.

# GERMANIUM RATE GROWN NPN TRANSISTORS

## (See Outline Drawing No. 3)

| Type | $h_{FE}$ $V_{CE}$=1 v $I_C$=1 ma | MINIMUM $B_{CEO}$ $I_C$=300 μa volts | MAXIMUM $I_{CBO}$ $I_E$=0 $V_{CB}$=15 v μa | Power Gain @ 455 kc db | MAXIMUM Power Dissipation mw | TYPICAL $f_{hfb}$ mc | Comments |
|---|---|---|---|---|---|---|---|
| 2N78 | 45-135 | 15 | 3 | 26.0-31.0 | 65 | 9 | Preamplifier Switch. Lamp driver. Schmitt trigger. Waveform restoration. DC level detection. |
| 2N78A(7) | 45-135 | 20 | 3 | 26.0-31.0 | 65 | 9 | Applications same as 2N78. |
| 2N167A | 17-90(1) | 30 | 1.5 | — | 75 | 9 | Trigger circuits. Gate circuits. Logic circuits. |
| USAF2N167A | 17-90(1) | 30 | 1.5 | — | 75 | 9 | Mil. Spec. MIL-S-19500/11. |
| 2N169 | 34-200 | 15(3) | 5 | 24.0-31.0 | 65 | 8 | Reflex circuits. IF amplifiers. DC coupled Audio amplifiers. |
| 2N169A | 34-200 | 25(3) | 5 | 23.5-31.0 | 65 | 9 | General Purpose Low Level switch(4). |
| 2N292 | 8-51 | 15(3) | 5 | 21.0-26.0 | 65 | 5 | IF Amplifiers. |
| 2N293 | 8-51 | 15(3) | 5 | 23.5-28.0 | 65 | 8 | IF Amplifiers. |
| 2N448 | 8-51 | 15(3) | 5 | 18.5-23.0 | 65 | 5 | IF Amplifiers. *Obsolete-Use 2N292.* |
| 2N449 | 34-200 | 15(3) | 5 | 21.5-25.0 | 65 | 8 | IF Amplifiers. *Obsolete-Use 2N169.* |
| 2N1086 | 17-200 | 9(3) | 3(5) | 23.0-29.0(6) | 65 | 9 | Autodyne Converter. |
| 2N1086A | 17-200 | 9(3) | 3(5) | 23.0-27.0(6) | 65 | 9 | Autodyne Converter. |
| 2N1087 | 17-200 | 9(3) | 3(5) | 25.0-29.0(6) | 65 | 9 | Autodyne Converter. |
| 2N1121 | 34-200 | 15 | 5 | 26.5-30.5 | 65 | 8 | Reflex circuits. IF Amplifiers. DC coupled Audio Amplifiers. |
| 2N1217 | 40-100(2) | 20 | 1.5 | — | 75 | 9 | Starvation Switch. |
| 2N1510 | 8-90 | 70(3) | 5 | — | 75 | 9 | High Voltage Neon Indicator Circuits. |
| 2N1694 | 15-45(2) | 20 | 1.5 | — | 75 | 9 | Decade Counter. Low Level Switch. Amplifiers. |

**NOTES:** (1) $I_C$ = 8 ma., $V_{CE}$ = 1 V. (2) $I_C$ = 2 ma., $V_{CE}$ = 1 V. (3) $BV_{CERL}$ R = 10K. (4) MAX $V_{CE(SAT)}$ = .4 V. (5) $V_{CB}$ = 5 V. (6) Conversion Gain @ 1600 Kc. (7) Also available in military types.

## SILICON SIGNAL DIODES

| Type | Drwg. No. | MAXIMUM Forward Voltage $V_F$ Volts | MAXIMUM Reverse Current $I_R$ 25°C μa | MAXIMUM Reverse Current $I_R$ 150°C μa | Min. Breakdown Voltage V $I_R=5\mu a$ Volts | Total Capacitance $V_R=0$ pf | MAXIMUM Reverse Recovery Time $t_{rr}$ $I_F=10$ ma, $V_R=-6v$ $R_L=100\Omega$ nsec | MAXIMUM Power Dissipation mw | MAXIMUM Forward Current Steady State DC ma | Comments |
|---|---|---|---|---|---|---|---|---|---|---|
| 1N3604 | 14 | 1.0 @ 50 ma | .05 @ 50V | 50 @ 50V | 75 | 2 | 2 | 250 | 115 | Very high speed, high conductance, computer diode. Subminiature package. |
| 1N3605 | 14 | See Table I | .05 @ 30V | 50 @ 30V | 40 | 2 | 2 | 250 | 115 | Controlled conductance, very high speed diode. Subminiature glass package. |
| 1N3606 | 14 | See Table I | .05 @ 50V | 50 @ 50V | 75 | 2 | 2 | 250 | 115 | |
| 1N3063 | 14 | See Table II | .1 @ 50V | 100 @ 50V | 75 | 2 | 2 | 250 | 115 | |
| 1N3607 | 15 | 1.0 @ 50 ma | .05 @ 50V | 50 @ 50V | 75 | 2 | 2 | 150 | 115 | Very high speed, high conductance diode in microminiature package. |
| 1N3608 | 15 | See Table I | .05 @ 30V | 50 @ 30V | 40 | 2 | 2 | 150 | 115 | Controlled conductance, very high speed diode in microminiature package. |
| 1N3609 | 15 | See Table I | .05 @ 50V | 50 @ 50V | 75 | 2 | 2 | 150 | 115 | |

Note— above ratings also apply to diodes in pairs, and quads.

| | | | | | | $\Delta V_F$—Max. Forward Voltage difference between diodes in pairs or quads ($T_A$=−55°C to +125°C) | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $I_F$=0.1 to 10 ma mv | $I_F$=10 to 50 ma mv | | |
| 4JF4-MP-1 | 16 | 1.0 @ 50 ma | .05 @ 50V | 50 @ 50V | 75 | 10 | 20 | | Matched pairs in molded package. |
| 4JF4-MP-2 | 16 | 1.0 @ 10 ma | .10 @ 30V | 100 @ 30V | 40 | 10 | 50 | | |
| 4JF4-MQ-1 | 16 | 1.0 @ 50 ma | .05 @ 50V | 50 @ 50V | 75 | 10 | 20 | | Matched quads in molded package. |
| 4JF4-MQ-2 | 16 | 1.0 @ 10 ma | .10 @ 30V | 100 @ 30V | 40 | 10 | 50 | | |

**TABLE 1**

| $I_F$ ma | Forward Voltage $V_F$ Min. mv | Max. mv |
|---|---|---|
| 0.1 | 0.490 | 0.550 |
| 0.25 | 0.530 | 0.590 |
| 1.0 | 0.590 | 0.670 |
| 2.0 | 0.620 | 0.700 |
| 10.0 | 0.700 | 0.810 |
| 20.0 | 0.740 | 0.880 |

**TABLE 2**

| $I_F$ ma | Forward Voltage $V_F$ Min. mv | Max. mv |
|---|---|---|
| .25 | .505 | .575 |
| 1.0 | .550 | .650 |
| 2.0 | .610 | .710 |
| 10.0 | .700 | .850 |

# TUNNEL DIODES[1]

| Type | Drwg. No. | Peak Point Current $I_P$ ma | MAXIMUM Valley Point Current $I_V$ ma | MAXIMUM Capacitance C pf | Peak Voltage $V_P$ mv | Max. Series Resist. $R_S$ ohms | Negative Conductance −G mhos × $10^{-6}$ | Typical Resistive Cutoff Frequency $f_{ro}$ Kmc | Comments |
|---|---|---|---|---|---|---|---|---|---|
| 4JF1-TD-1 | 17 | 1.0 ± 10% | 0.18 | 10 | 65 Typ. | 4.0 | 8 Typ. | 2.3 | Low cost, general purpose switching oscillator, amplifier, and converter, circuits below 1 Kmc. Subminiature axial package. |
| TD-1A | 17 | 1.0 ± 2.5% | 0.14 | 5 | 65 ± 7 | 4.0 | 8.5 ± 1 | 3.2 | |
| TD-2 | 17 | 2.2 ± 10% | 0.48 | 25 | 65 Typ. | 3.0 | 18 Typ. | 2.2 | |
| TD-2A | 17 | 2.2 ± 2.5% | 0.31 | 10 | 65 ± 7 | 3.0 | 19 ± 3 | 3.0 | |
| TD-3 | 17 | 4.7 ± 10% | 1.04 | 50 | 65 Typ. | 2.0 | 40 Typ. | 1.8 | |
| TD-3A | 17 | 4.7 ± 2.5% | 0.60 | 25 | 65± 7 | 2.0 | 41 ± 5 | 3.4 | |
| TD-4 | 17 | 10.0 ± 10% | 2.20 | 90 | 65 Typ. | 1.5 | 80 Typ. | 1.6 | |
| TD-4A | 17 | 10.0 ± 2.5% | 1.40 | 50 | 65 ± 7 | 1.5 | 85 ± 10 | 2.8 | |
| TD-5 | 17 | 22.0 ± 10% | 4.80 | 150 | 65 Typ. | 1.0 | 180 Typ. | 1.6 | |
| TD-5A | 17 | 22.0 ± 2.5% | 3.10 | 100 | 65 ± 7 | 1.0 | 190 ± 30 | 2.6 | |
| 1N3218 | 19 | 1.0 ± 10% | 0.22 | 10 | 60 Typ. | 4.0 | 8.5 ± 3.5 | 1.5 | Microwave oscillator amplifier and converter circuits. Ultra high speed computer circuits. Microwave package. |
| 1N3218A | 19 | 1.0 ± 10% | 0.22 | 5 | 60 Typ. | 4.0 | 8.5 ± 3.5 | 3.0 | |
| 1N3219 | 19 | 2.2 ± 10% | 0.48 | 20 | 60 Typ. | 3.0 | 17.5 ± 7.5 | 1.8 | |
| 1N3219A | 19 | 2.2 ± 10% | 0.48 | 10 | 60 Typ. | 3.0 | 17.5 ± 7.5 | 3.4 | |
| 4JF1-TD-310 | 19 | 4.7 ± 10% | 1.04 | 10 | 100 Typ. | 2.5 | 30 Typ. | 2.7 | |
| TD-310A | 19 | 4.7 ± 10% | 1.04 | 5 | 100 Typ. | 2.5 | 30 Typ. | 5.5 | |
| TD-311 | 19 | 10.0 ± 10% | 2.2 | 20 | 90 Typ. | 2.0 | 70 Typ. | 2.7 | |
| TD-311A | 19 | 10.0 ± 10% | 2.2 | 10 | 90 Typ. | 2.0 | 70 Typ. | 5.4 | |
| TD-311B | 19 | 10.0 ± 4% | 1.3 | 9 | 86 ± 11 | 1.5 | 70 Typ. | 6.1 | |
| 4JF1-MTD-1 | 15 | 1.0 ± 10% | 0.22 | 10 | 65 Typ. | 4.0 | 8 Typ. | 2.3 | Microminiature, very low inductance package for thin film circuits and microminiature equipments. |
| MTD-2 | 15 | 2.2 ± 10% | 0.48 | 25 | 65 Typ. | 3.0 | 16 Typ. | 2.5 | |
| MTD-3 | 15 | 4.7 ± 10% | 1.04 | 50 | 65 Typ. | 2.0 | 30 Typ. | 2.6 | |
| MTD-4 | 15 | 10.0 ± 10% | 2.2 | 100 | 65 Typ. | 1.5 | 60 Typ. | 2.3 | |

**NOTES:** (1) See General Electric *Tunnel Diode Manual.*

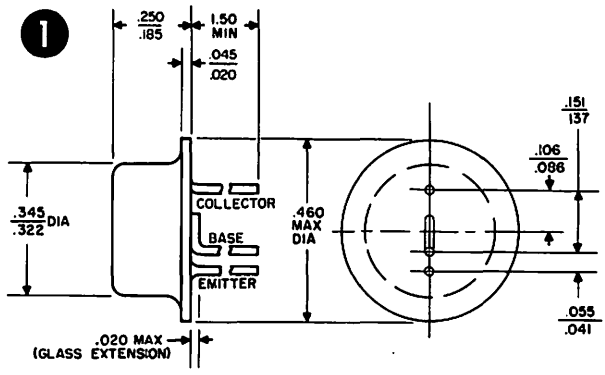
# BACK DIODES[1]

| Type | Drwg. No. | Forward Voltage $V_{F1}$=90 mv ±10 mv when $I_{F1}$= ma | Forward Voltage $V_{F2}$ (at $I_{F2}$=3 $I_{F1}$) mv | Max. Reverse Peak Point Current $I_P$ ma | Min. Reverse Voltage $V_{R1}$ ($I_R$=$I_P$ max) mv | Min. Reverse Voltage $V_{R2}$ ($I_R$=1 ma) mv | Max. Total Capac. C pf | Comments |
|---|---|---|---|---|---|---|---|---|
| 4JF2-BD-1 | 18 | 10.0 | 120 | 1.0 | 440 | 440 | 20 | Germanium. Very low forward drop, high speed switching diode. Subminiature axial package. |
| -BD-2 | 18 | 5.0 | 130 | 0.5 | 420 | 465 | 10 | |
| -BD-3 | 18 | 2.0 | 170 | 0.2 | 400 | 465 | 10 | |
| -BD-4 | 18 | 1.0 | 170 | 0.1 | 380 | 465 | 10 | |
| -BD-5 | 18 | .5 | 160 | 0.05 | 350 | 465 | 10 | |
| -BD-6 | 18 | .2 | 160 | 0.02 | 330 | 465 | 10 | |
| -BD-7 | 18 | .1 | 160 | 0.01 | 300 | 465 | 10 | |
| | | $V_{F1}$=200 mv ±20 mv when $I_{F1}$= (ma) | | | | | | |
| 4JF2-BD-501 | 17 | 10.0 | 325 | 1.0 | 800 | — | 8 | Gallium Arsenide. Low forward drop, high speed switching diode. Subminiature axial package. |
| -BD-502 | 17 | 5.0 | 325 | .5 | 800 | — | 8 | |
| -BD-503 | 17 | 2.0 | 325 | .2 | 800 | — | 8 | |

**NOTES:**

(1) See General Electric *Tunnel Diode Manual.*

## OUTLINE DRAWINGS



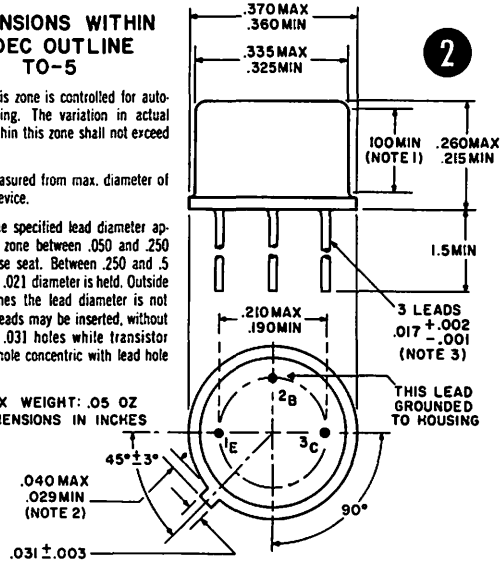

### DIMENSIONS WITHIN JEDEC OUTLINE TO-5

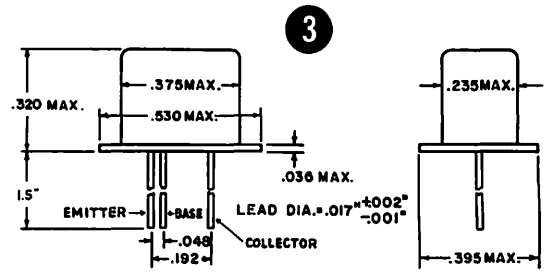
**NOTE 1:** This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

**NOTE 2:** Measured from max. diameter of the actual device.

**NOTE 3:** The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and .5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled. Leads may be inserted, without damage, in .031 holes white transistor enters .371 hole concentric with lead hole circle.

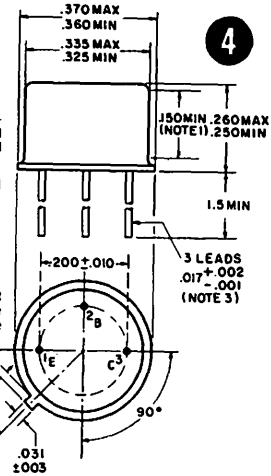
APPROX WEIGHT: .05 OZ
ALL DIMENSIONS IN INCHES



## DIMENSIONS WITHIN JEDEC OUTLINE TO-5

4



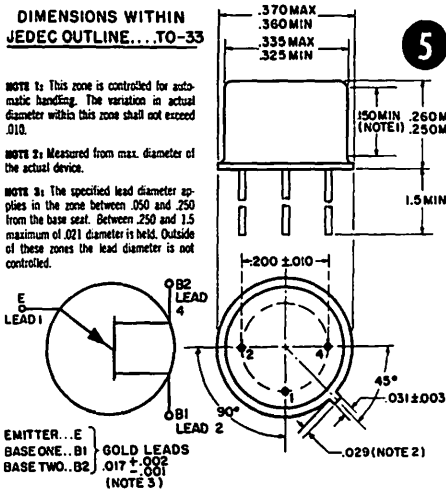

NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

NOTE 2: Measured from max. diameter of the actual device.

NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and 1.5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled. Leads may be inserted, without damage, in .031 holes while transistor enters .371 hole concentric with lead hole circle.

## DIMENSIONS WITHIN JEDEC OUTLINE....TO-33

5

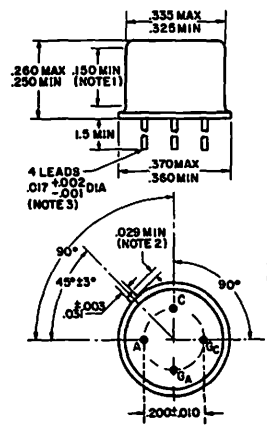



NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

NOTE 2: Measured from max. diameter of the actual device.

NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and 1.5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled.

## DIMENSIONS WITHIN JEDEC OUTLINE TO-5

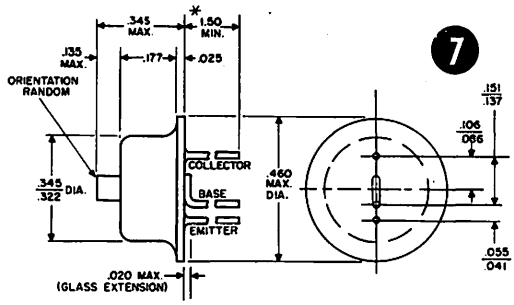



NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

NOTE 2: Measured from max. diameter of the actual device.

NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and .5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled.

6




* CUT TO 0.200" FOR USE IN SOCKETS.
LEADS TINNED DIA. .018
MOUNTING POSITION - ANY
WEIGHT: .05 OZ.
BASE CONNECTED TO TRANSISTOR SHELL.
DIMENSIONS IN INCHES.

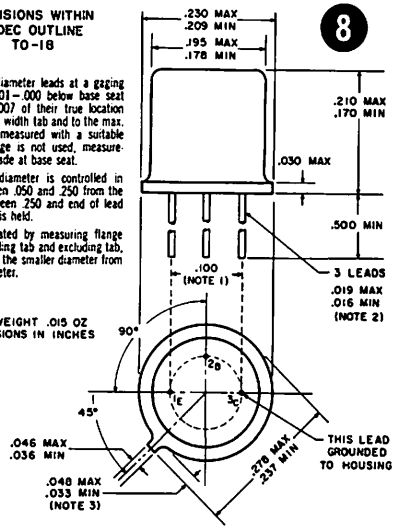
DIMENSIONS WITHIN JEDEC OUTLINE TO-18

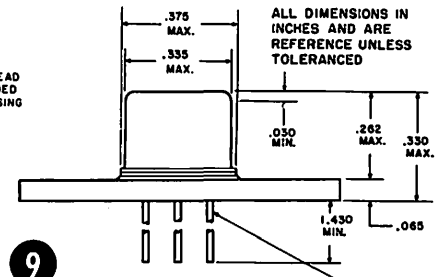
**NOTE 1:** Max. diameter leads at a gaging plane .054 + .001 − .000 below base seat to be within .007 of their true location relative to max. width tab and to the max. .230 diameter measured with a suitable gage. When gage is not used, measurement will be made at base seat.

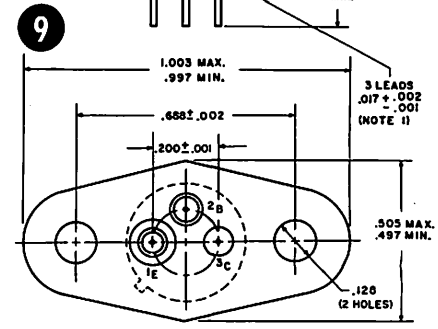
**NOTE 2:** Lead diameter is controlled in the zone between .050 and .250 from the base seat. Between .250 and end of lead a max. of .021 is held.

**NOTE 3:** Calculated by measuring flange diameter, including tab and excluding tab, and subtracting the smaller diameter from the larger diameter.

APPROX WEIGHT .015 OZ
ALL DIMENSIONS IN INCHES

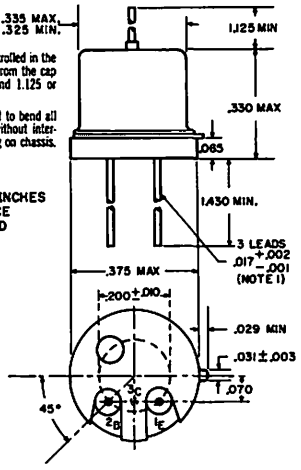



**NOTE 1:** Lead diameter is controlled in the zone between .050 and .250 from the base seat. Between .250 and end of lead a max. of .021 is held.

**10**

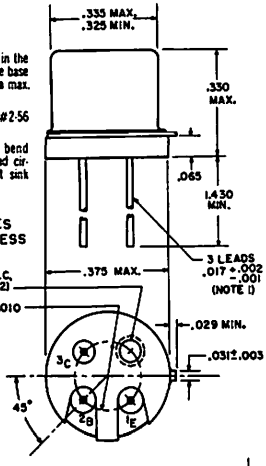



NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the cap or base seat. Between .250 and 1.125 or 1.430 a max. of .021 is held.

NOTE 2: Clearance is provided to bend all leads for overhead circuitry without interfering with heat sink mounting on chassis.

ALL DIMENSIONS IN INCHES AND ARE REFERENCE UNLESS TOLERANCED

**11**



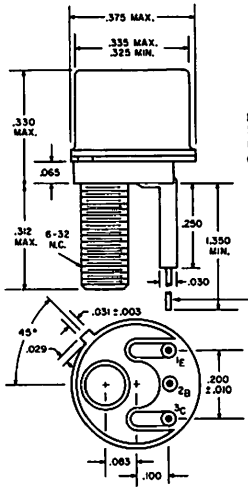

NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the base seat. Between .250 and end of lead a max. .021 is held.

NOTE 2: Do not attempt to insert a #2-56 stud in excess of .045.

NOTE 3: Clearance is provided to bend base and emitter leads for overhead circuitry without interfering with heat sink mounting on chassis.

ALL DIMENSIONS IN INCHES AND ARE REFERENCE UNLESS TOLERANCED

**12**

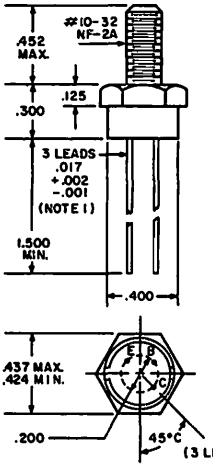



NOTE 1: All leads are protected from grounding on mounting panel up to ¼" thick. Between .250 and end of lead a max. of .021 is held.

NOTE 2: Clearance is provided to bend all leads for overhead circuitry without interfering with heat sink mounting on chassis.

NOTE 3: All dimensions in inches and are reference unless toleranced.

## 13

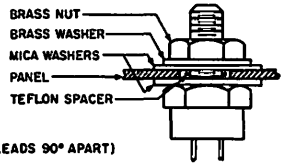



**NOTE 1:** Lead diameter is controlled in the zone between .050 and .250 from the cap or base seat. Between .250 and end of lead a max. of .021 is held.

**NOTE 2:** Provision is made for the device to be electrically insulated from mounting surface as shown below. For this service a clearance hole of .281 is recommended.

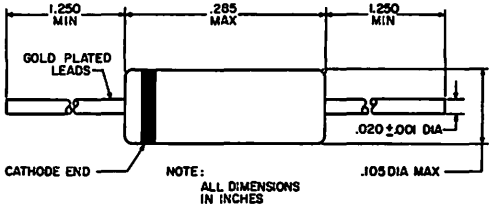
**NOTE 3:** All exposed metal parts, including hardware, but not including leads, are nickel plated.

TYPICAL INSULATED MOUNTING (NOTE 2)

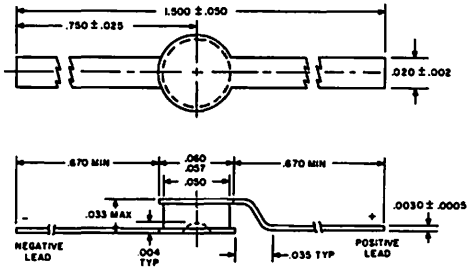



ALL DIMENSIONS ARE REFERENCE UNLESS TOLERANCED

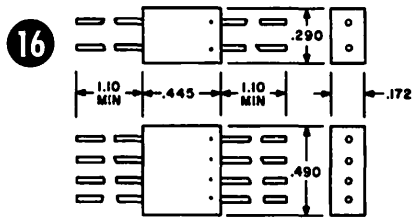
## 14




## 15

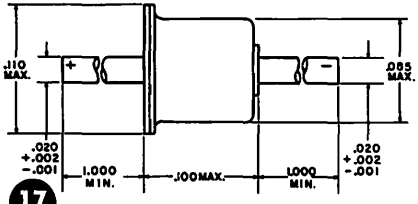



ALL DIMENSIONS IN INCHES
DIMENSIONS ARE REFERENCE UNLESS TOLERANCED

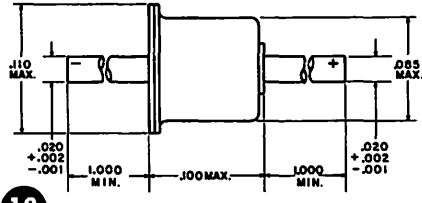



16

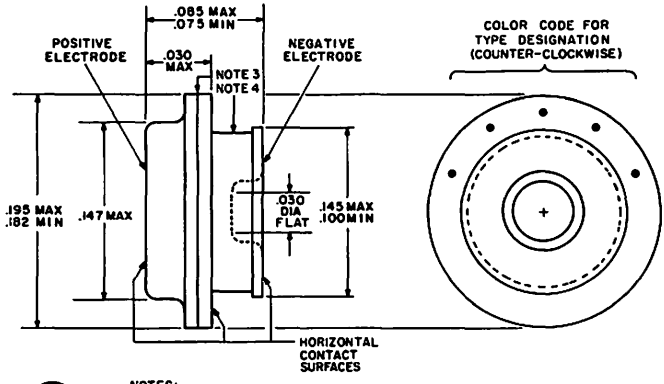
1. DIMENSIONS ARE NOMINAL (INCHES)
2. DOTS OR LINE INDICATE CATHODE END
3. LEADS ARE GOLD PLATED, DIAMETER .020 ± .001, SPACING .100 NOMINAL




17 ALL DIMENSIONS IN INCHES.
DIMENSIONS ARE REFERENCE UNLESS TOLERANCED.




18 ALL DIMENSIONS IN INCHES.
DIMENSIONS ARE REFERENCE UNLESS TOLERANCED.




19

NOTES:
1. ALL DIMENSIONS IN INCHES.
2. DIMENSIONS ARE REFERENCES UNLESS TOLERANCED.
3. WELD FLASH ALLOWED (THIS IS NOT A CONTACT SURFACE).
4. INSULATION - DO NOT ALLOW CLAMPS.

# REGISTERED JEDEC TRANSISTOR TYPES



For explanation of abbreviations, see page 440

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVce BVcb* | Ic ma | Tj°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ Vcb | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N22 | Pt | | 120 | −100 | −20 | 55 | 1.9α | | | | | | | |
| 2N23 | Pt | | 80 | −50 | −40 | 55 | 1.9α | | | | | | | |
| 2N24 | Pt | | 120 | −30 | −25 | 50 | 2.2α | | | | | | | |
| 2N25 | Pt | | 200 | −50 | −30 | 60 | 2.5α | | | | | | | |
| 2N26 | Pt | | 90 | −30 | −40 | 55 | | | | | | | | |
| 2N27 | NPN | | 50 | 35* | 100 | 85 | 100 | | 1 | | | | | |
| 2N28 | NPN | | 50 | 30* | 100 | 85 | 100 | | .5 | | | | | |
| 2N29 | NPN | | 50 | 35* | 30 | 85 | 100 | | 1 | | 15 | 30 | | |
| 2N30 | Pt | Obsolete | 100 | 30 | 7 | 40 | 2.2α | | 2T | 17T | | | Old G11 | |
| 2N31 | Pt | Obsolete | 100 | 30 | 7 | 40 | 2.2α | | 2T | | 150 | 25 | Old G11A | |
| 2N32 | Pt | Obsolete | 50 | −40 | −8 | 40 | 2.2α | | 2.7 | 21T | | | | |
| 2N32A | Pt | Obsolete | 50 | −40 | −8 | 40 | 2.2α | | 2.7 | 21T | | | | |
| 2N33 | Pt | Obsolete | 30 | −8.5 | −7 | 40 | | | | | | | | |
| 2N34 | PNP | Obsolete | 50 | −25 | −8 | 50 | 40 | | .6 | 40T | | | 2N190 | 1 |
| 2N34A | PNP | Obsolete | 50 | −25 | −8 | 50 | 40 | | .6 | 40T | | | 2N190 | 1 |
| 2N35 | NPN | | 50 | 25 | 8 | 50 | 40 | | .8 | 40T | | | 2N169 | 3 |
| 2N36 | PNP | | 50 | −20 | −8 | 50 | 45T | | | 40T | | | 2N191 | 1 |
| 2N37 | PNP | | 50 | −20 | −8 | 50 | 30T | | | 36T | | | 2N190 | 1 |
| 2N38 | PNP | | 50 | −20 | −8 | 50 | 15T | | | 32T | | | 2N189 | 1 |
| 2N38A | PNP | | 50 | −20 | −8 | 50 | 18T | | | 34 | −12 | −3 | 2N189 | 1 |
| 2N41 | PNP | | 50 | −25 | −15 | 50 | 40T | | | 40T | −10 | −12 | 2N190 | 1 |
| 2N43 | PNP | AF | 240 | −30 | −300 | 100 | 30 | 1 | .5 | | −16 | −45 | 2N43, 2N525 | 1, 2 |
| 2N43A | PNP | AF | 240 | −30 | −300 | 100 | 30 | 1 | .15 | | −16 | −45 | 2N43A, 2N525 | 1, 2 |
| 2N44 | PNP | AF | 240 | −30 | −300 | 100 | 25T | 1 | .5 | | −16 | −45 | 2N44, 2N524 | 1, 2 |
| 2N45 | PNP | Obsolete | 155 | −25 | −10 | 100 | 25T | | .5 | 34 | −16 | −45 | 2N44 | 1 |
| 2N46 | PNP | | 50 | −25 | −15 | 50 | 40T | | | 4T | −10 | −12 | 2N1414 | 2 |
| 2N47 | PNP | | 50 | −35* | −20 | 65 | .975α | | | | −5 | −12 | 2N1414 | 2 |
| 2N48 | PNP | | 50 | −35* | −20 | 65 | .970α | | | | −5 | −12 | 2N1414 | 2 |
| 2N49 | PNP | | 50 | −35* | −20 | 65 | .975 | | | | −5 | −12 | 2N1414 | 2 |
| 2N50 | Pt | | 50 | −15 | −1 | 50 | 2α | | 3T | | | | | |
| 2N51 | Pt | | 100 | −50 | −8 | 50 | 2.2α | | | | −350 | −7 | | |
| 2N52 | Pt | | 120 | −50 | −8 | 50 | | | | | | | | |
| 2N53 | Pt | | | −50 | −8 | | | | | | | | | |
| 2N54 | PNP | | 200 | −45 | −10 | 60 | .95α | | | 40T | | | 2N1098 16V | 2 |
| 2N55 | PNP | | 200 | −45 | −10 | 60 | .92α | | | 39T | | | 2N1097 16V | 2 |
| 2N56 | PNP | | 200 | −45 | −10 | 60 | .90α | | | 38T | | | 2N320 | 4 |
| 2N59 | PNP | | 180 | −25* | −200 | 85 | 90T* | −100 | | 35T | −15 | −20 | 2N1415 | 2 |
| 2N59A | PNP | | 180 | −40* | −200 | 85 | 90T* | −100 | | 35T | −15 | −20 | 2N1415 | 2 |
| 2N59B | PNP | | 180 | −50* | −200 | 85 | 90T* | −100 | | 35T | −15 | −20 | | |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCB BVCB* | Ic ma | TJ °C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N59C | PNP | | 180 | −60* | −200 | 85 | 90T* | −100 | | 35T | −15 | −20 | | |
| 2N60 | PNP | | 180 | −25* | −200 | 85 | 65T* | −100 | | 35T | −15 | −20 | 2N1415 | 2 |
| 2N60A | PNP | | 180 | −40* | −200 | 85 | 65T* | −100 | | 35T | −15 | −20 | 2N1415 | 2 |
| 2N60B | PNP | | 180 | −50* | −200 | 85 | 65T* | −100 | | 35T | −15 | −20 | 2N1925 | 2 |
| 2N60C | PNP | | 180 | −60* | −200 | 85 | 65T* | 100 | | 35T | −15 | −20 | 2N1926 | 2 |
| 2N61 | PNP | | 180 | −25* | −200 | 85 | 45T* | 100 | | 35T | −15 | −20 | 2N1415 | 2 |
| 2N61A | PNP | | 180 | −40* | −200 | 85 | 45T* | 100 | | 35T | −15 | −20 | 2N1415 | 2 |
| 2N61B | PNP | | 180 | −50* | −200 | 85 | 45T* | 100 | | 35T | −15 | −20 | 2N1924 | 2 |
| 2N61C | PNP | | 180 | −60* | −200 | 85 | 45T* | 100 | | 35T | −15 | −20 | 2N1924 | 2 |
| 2N62 | PNP | | 50 | −35* | −20 | | .975αT | | | | | | | |
| 2N63 | PNP | | 100 | −22 | −10 | 85 | 22T | 1 | | 39T | −6 | −6 | 2N1924 | 2 |
| 2N64 | PNP | | 100 | −15 | −10 | 85 | 45T | 1 | | 41T | −6 | −6 | 2N1415 | 2 |
| 2N65 | PNP | | 100 | −12 | −10 | 85 | 90T | 1 | | 92T | −6 | −6 | 2N324 | 4 |
| 2N66 | PNP | | 1W | −40 | .8A | 80 | | | .2 | | −300 | −40 | | |
| 2N67 | PNP | | 2W | −25* | −1.5A | 70 | | | | 23T | | | | |
| 2N68 | PNP | | 2W | −25* | −1.5A | | | | | 23 | −150 ma | | | |
| 2N71 | PNP | | 1W | −50 | −250 | 60 | | | .25 | 20 | | | | |
| 2N72 | Pt | | 50 | −40 | −20 | 55 | | | 2.5 | | | | | |
| 2N73 | PNP | | 200 | −50 | | | | | | | | | 2N1614 | 1 |
| 2N74 | PNP | | 200 | −50 | | | | | | | | | 2N1614 | 1 |
| 2N75 | PNP | | 200 | −20 | | | | | | | | | 2N1614 | 1 |
| 2N76 | PNP | Obsolete | 50 | −20* | −10 | 60 | .90α | | 1.0 | 34 | −10 | −20 | 2N322 | 4 |
| 2N77 | PNP | | | −25* | −15 | 85 | 55 | | .70 | 44T | −10 | −12 | 2N324 | 4 |
| 2N78 | NPN | RF/IF | 65 | 15 | 20 | 85 | 45* | 1 | 5 | 27 | 3 | 15 | 2N78 | 3 |
| 2N78A | NPN | RF/IF | 65 | 20 | 20 | 85 | 45* | 1 | 5 | 29 | 3 | 15 | 2N78A | 3 |
| 2N79 | PNP | | 35 | −30 | −50 | | 46 | | .7 | 44 | | | 2N321, 2N323 | 4, 4 |
| 2N80 | PNP | | 50 | −25 | −8 | 100 | 80T | | | | −30 | −10 | 2N508, 2N1175 | 2, 2 |
| 2N81 | PNP | Obsolete | 50 | −20 | −15 | 100 | 20 | 1 | | | −16 | −30 | 2N1098 | 2 |
| 2N82 | PNP | | 35 at 71° C | −20 | −15 | 100 | 20 | 1 | | | −16 | −30 | 2N1098 | 2 |
| 2N94 | NPN | | 30 | 20 | 5 | 75 | 40T | .5 | 3T | 25T | 3 | 10 | 2N634, 2N169A | 2, 3 |
| 2N94A | NPN | | 30 | 20 | 5 | 75 | 40T | .5 | 6T | 25T | 3 | 10 | 2N634, 2N169A | 2, 3 |
| 2N95 | NPN | | 2.5W | 25* | 1.5 | 70 | 40 | | .4T | 23T | | | | |
| 2N96 | PNP | | 50 | −30 | −20 | 55 | 35 | | .5 | | | | 2N1414 | 2 |
| 2N97 | NPN | | 50 | 30 | 10 | 75 | .85α | | .5 | 38T | 10 | 4.5 | 2N169 15V | 3 |
| 2N97A | NPN | | 50 | 40 | 10 | 85 | .85α | | .5 | 38T | 5 | 30 | 2N169A 25V | 3 |
| 2N98 | NPN | | 50 | 40 | 10 | 75 | .95α | | .8 | 47T | 10 | 4.5 | 2N169A 25V | 3 |
| 2N98A | NPN | | 50 | 40 | 10 | 85 | .96α | | .8 | 47T | 10 | 4.5 | 2N169A 25V | 3 |
| 2N99 | NPN | | 50 | 40 | 10 | 75 | .95α | | 2.0 | 47T | 10 | 4.5 | 2N169A 25V | 3 |
| 2N100 | NPN | | 25 | 25 | 5 | 50 | .99α | | 2.5 | 53T | 10 | 4.5 | 2N170 6V | 3 |
| 2N101 | PNP | | 1W | −25* | −1.5 | 70 | | | | 23T | | | | |
| 2N102 | NPN | | 1W | 25* | 1.5 | 70 | | | | 23T | | | | |
| 2N103 | NPN | | 50 | 35 | 10 | 75 | .60α | | .75T | 33T | 50 | 35 | 2N1302 | 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N104 | PNP | | 150 | −30 | −50 | 85 | 44 | | .7 | 33T | −10 | −12 | 2N1415, 2N1414 | 2, 2 |
| 2N105 | PNP | | 35 | −25 | −15 | 85 | 55 | .7 | .75 | 42 | −5 | −12 | 2N1415 | 2 |
| 2N106 | PNP | | 100 | −6 | −10 | 85 | 25 | | .8 | 28 | −12 | −6 | 2N1097, 2N1098 | 2, 2 |
| 2N107 | PNP | AF | 50 | −6 | −10 | 60 | 20 | | .6 | | −10 | −12 | 2N107, 2N1098 | 1, 2 |
| 2N108 | PNP | | 50 | −20 | −15 | | | | | | | | 2N322 | 4 |
| 2N109 | PNP | | 150 | −25 | −70 | 85 | 75* | | | 30T | | | 2N1175 | 2 |
| 2N110 | Pt | | 200 | −50* | −50 | 85 | 32 | | 1.5 | | | | | |
| 2N111 | PNP | | 150 | −15 | 200 | 85 | 15 | | 3T | 33T | −5 | −12 | 2N394 | 2 |
| 2N111A | PNP | | 150 | −15 | −200 | 85 | 15 | | 3T | 33T | −5 | −12 | 2N394 | 2 |
| 2N112 | PNP | | 150 | −15 | −200 | 85 | 15 | | 5T | 35T | −5 | −12 | 2N394 | 2 |
| 2N112A | PNP | | 150 | −15 | −200 | 85 | 15 | | 5T | 35T | −5 | −12 | 2N394 | 2 |
| 2N113 | PNP | | 100 | −6 | −5 | 85 | 45T | | 10T | 33T | | | 2N394 | 2 |
| 2N114 | PNP | | 100 | −6 | −5 | 85 | 65T | | 20T | | | | 2N394 | 2 |
| 2N117 | NPN | | 150 | 30* | 25 | 150 | .90α | 1 | 1 | | 10 | 30 | 2N332, 2N334 | 4, 4 |
| 2N118 | NPN | | 150 | 30* | 25 | 150 | .95α | 1 | 2 | | 10 | 30 | 2N333, 2N335 | 4, 4 |
| 2N118A | NPN-G | | 150 | 45 | 25 | 150J | 54T | | 7.50 | | 10 | | 2N335 | 4 |
| 2N119 | NPN | | 150 | 30* | 25 | 150 | .974α | 1 | 2 | | 10 | 30 | 2N335, 2N336 | 4, 4 |
| 2N120 | NPN | | 150 | 45* | 25 | 175 | .987α | 1 | 7T | | 2 | 30 | | |
| 2N122 | NPN | | 8.75W | | 140A | 150 | 3 | 100 | | | 10 ma | 50 | | |
| 2N123 | PNP | Sw | 150 | −15 | −125 | 85 | 30* | −10 | 5 | | −6 | −20 | 2N123 | 7 |
| 2N124 | NPN | | 50 | 10* | 8 | 75 | 12* | 5 | 3 | | 2 | 5 | 2N293 | 3 |
| 2N125 | NPN | | 50 | 10* | 8 | 75 | 24* | 5 | 5 | | 2 | 5 | 2N167 | 3 |
| 2N126 | NPN | | 50 | 10* | 8 | 75 | 48* | 5 | 5 | | 2 | 5 | 2N167, 2N169 | 3, 3 |
| 2N127 | NPN | | 50 | 10* | 8 | 75 | 100* | 5 | 5 | | 2 | 5 | 2N167, 2N169 | 3, 3 |
| 2N128 | PNP | | 30 | −4.5 | −5 | 85 | .95 | .5 | 45 $f_{max}$ | | −3 | −5 | 2N711 | 8 |
| 2N129 | PNP | | 30 | −4.5 | −5 | 85 | .92 | .5 | 30 $f_{max}$ | | −3 | −5 | 2N711 | 8 |
| 2N130 | PNP | | 85 | −22 | −10 | 85 | 22T | | | 39T | | | 2N1413, 2N1924 | 2, 2 |
| 2N130A | PNP | | 100 | −40 | −100 | 85 | 14 | 1 | .7T | 40T | −15 | −20 | 2N1413, 2N1924 | 2, 2 |
| 2N131 | PNP | | 85 | −15 | −10 | 85 | 45T | | | 41T | | | 2N1413, 2N1415 | 2, 2 |
| 2N131A | PNP | | 100 | −30 | −100 | 85 | 27 | 1 | .8T | 42T | −15 | −20 | 2N1413, 2N1924 | 2, 2 |
| 2N132 | PNP | | 85 | −12 | −10 | 85 | 90T | | | 42T | | | 2N1175 | 2 |
| 2N132A | PNP | | 100 | −20 | −100 | 85 | 56 | 1 | 1T | 44T | −15 | −20 | 2N1415 | 2 |
| 2N133 | PNP | | 85 | −15 | −10 | 85 | 25 | | | 36T | −12 | −15 | 2N1414 | 3 |
| 2N133A | PNP | | 100 | −20 | −100 | 85 | 50T | 1 | .8T | 38T | −15 | −20 | 2N1414, 2N1175 | 3, 2 |
| 2N135 | PNP | Obsolete | 100 | −12 | −50 | 85 | 20T | | 4.5T | 29T | | | 2N394 | 2 |
| 2N136 | PNP | Obsolete | 100 | −12 | −50 | 85 | 40T | | 6.5T | 31T | | | 2N394 | 2 |
| 2N137 | PNP | Obsolete | 100 | −6 | −50 | 85 | 60T | | 10T | 33T | | | 2N394 | 2 |
| 2N138 | PNP | | 50 | −12 | −20 | 50 | 140T | | | 30T | | | 2N508 | 2 |
| 2N138A | PNP | | 150 | −30 | −100 | 85 | | | | 29T | | | 2N1098 | 2 |
| 2N138B | PNP | | 100 | −30 | −100 | 85 | | | | 29T | | | 2N1098 | 2 |
| 2N139 | PNP | | 80 | −16 | −15 | 85 | 48 | 1 | 6.8 | 30 | −6 | −12 | 2N394 | 2 |
| 2N140 | PNP | | 35 | −16 | −15 | 85 | 45 | .4 | 7 | 27 | −6 | −12 | 2N394, 2N395 | 2, 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVce BVcb* | Ic ma | TJ °C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ Vcb | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N141 | PNP | | 4W | −30 | −.8A | 65 | .975αT | 50 | .4T | 18T | −100 | −20 | | |
| 2N142 | NPN | | 4W | 30 | .8A | 65 | .975αT | −50 | .4T | 26T | −100 | 20 | | |
| 2N143 | PNP | | 4W | −30 | −.8A | 65 | .975αT | 50 | .4T | 26T | −100 | −20 | | |
| 2N144 | NPN | | 4W | 30 | .8A | 65 | .975αT | 50 | .4T | 26T | 100 | 20 | | |
| 2N145 | NPN | | 65 | 20 | 5 | 75 | 30 | | | 30 | 3 | 9 | 2N293, 2N1121 | 3, 3 |
| 2N146 | NPN | | 65 | 20 | 5 | 75 | 33 | | | 33 | 3 | 9 | 2N1121 | 3 |
| 2N147 | NPN | | 65 | 20 | 5 | 75 | 36 | | | 36 | 3 | 9 | 2N1121 | 3 |
| 2N148 | NPN | | 65 | 16 | 5 | 75 | | | | 32 | 3 | 12 | 2N169 | 3 |
| 2N148A | NPN | | 65 | 32 | 5 | 75 | | | | 32 | 3 | 12 | 2N169 | 3 |
| 2N149 | NPN | | 65 | 16 | 5 | 75 | | | | 35 | 3 | 12 | 2N169 | 3 |
| 2N149A | NPN | | 65 | 32 | 5 | 75 | | | | 35 | 3 | 12 | 2N169 | 3 |
| 2N150 | NPN | | 65 | 16 | 5 | 75 | | | | 38 | 3 | 12 | 2N169 | 3 |
| 2N150A | NPN | | 65 | 32 | 5 | 75 | | | | 38 | 3 | 12 | 2N169 | 3 |
| 2N155 | PNP | | 8.5W | −30* | −3A | 85 | | | .15T | 30 | 1 ma | −30 | | |
| 2N156 | PNP | | 8.5W | −30* | −3A | 85 | 24* | .5A | .15T | 33 | 1 ma | −30 | | |
| 2N157 | PNP | | 8.5W | −60* | −3A | 85 | 20* | .5A | .1 | | 1 ma | −60 | | |
| 2N157A | PNP | | 8.5W | −90* | −3A | 85 | 20* | .5A | .1 | | 1 ma | −90 | | |
| 2N158 | PNP | | 8.5W | −60* | −3A | 85 | 21* | .5A | .15T | 37 | 1 ma | −60 | | |
| 2N158A | PNP | | 8.5W | −80* | −3A | 85 | 21* | .5A | .15 | | 1 ma | −80 | | |
| 2N160 | NPN | | 150 | 40* | 25 | 150 | .9α | −1 | 4T | 34T | 5 | 40 | 2N332, 2N1276 | 4, 4 |
| 2N160A | NPN | | 150 | 40* | 25 | 150 | .9α | −1 | 4T | 34T | 5 | 40 | 2N332 | 4 |
| 2N161 | NPN | | 150 | 40* | 25 | 150 | .95α | −1 | 5T | 37T | 5 | 40 | 2N333, 2N1277 | 4, 4 |
| 2N161A | NPN | | 150 | 40* | 25 | 150 | .95α | −1 | 5T | 37T | 5 | 40 | 2N333 | 4 |
| 2N162 | NPN | | 150 | 40* | 25 | 150 | .95α | −1 | 8 | 38T | 5 | 40 | 2N335, 2N1278 | 4, 4 |
| 2N162A | NPN | | 150 | 40* | 25 | 150 | .95α | −1 | 8 | 38T | 5 | 40 | 2N335 | 4 |
| 2N163 | NPN | | 150 | 40* | 25 | 150 | .975α | −1 | 6T | 40T | 5 | 40 | 2N335, 2N1278 | 4, 4 |
| 2N163A | NPN | | 150 | 40* | 25 | 150 | .975α | −1 | 6T | 40T | 5 | 40 | 2N335 | 4 |
| 2N164A | NPN | | 65 | 1.0* | 20 | 85J | 40T | | 8.00 | 30 | | | 2N1121 | 3 |
| 2N165 | PNP-M | | 55 | 1.0* | 20 | 75J | 72T | | 5.00 | 26 | | | 2N169 | 3 |
| 2N166 | NPN | Obsolete | 25 | 6 | 20 | 50 | 32T | 1 | 5T | 24T | 5 | 5 | 2N170 | 3 |
| 2N167 | NPN | Sw | 65 | 30 | 75 | 85 | 17* | 8 | 5 | | 1.5 | 15 | 2N167 | 3 |
| 2N167A | NPN | Sw | 65 | 30 | 75 | 85 | 17* | 8 | 5 | | 1.5 | 15 | 2N167A | 3 |
| 2N168 | NPN | IF | 55 | 15 | 20 | 75 | 20T | 1 | 6T | 28 | 5 | 15 | 2N293 | 3 |
| 2N168A | NPN | Obsolete | 65 | 15 | 20 | 85 | 23* | 1 | 5 | 28 | 5 | 15 | 2N1086, 2N1121 | 3, 3 |
| 2N169 | NPN | IF | 65 | 15 | 20 | 85 | 34* | 1 | 8T | 27 | 5 | 15 | 2N169 | 3 |
| 2N169A | NPN | AF | 65 | 15 | 20 | 85 | 34* | 1 | 8T | 27 | 5 | 15 | 2N169A | 3 |
| 2N170 | NPN | IF | 25 | 6 | 20 | 50 | .95αT | 1 | 4T | 22T | 5 | 5 | 2N170 | 3 |
| 2N172 | NPN | | 65 | 16 | 5 | 75 | | | | 22 | 3 | 9 | 2N293 | 3 |
| 2N173 | PNP | | 40W | −60 | −13A | 95 | 85T* | 1A | .6T | 40T | −.5 ma | −40 | | |
| 2N174 | PNP | | 40W | −80 | −13A | 95 | 40T* | 1A | .2T | 39T | −10 ma | −60 | | |
| 2N174A | PNP | | 85W | −80 | −15A | 95 | 40* | 1.2A | .1 | | −8 ma | −80 | | |
| 2N175 | PNP | | 20 | −10 | −2 | 85 | 65 | .5 | 2 | 43T | −12 | −25 | 2N1175A | 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N176 | PNP | | 3W | −12 | −600 | 80 | | | | 25T | | | | |
| 2N178 | PNP | | 3W | −12 | −600 | 80 | | | | 29T | | | | |
| 2N179 | PNP | | | −20 | −60 | 88 | | | | 32T | | | | |
| 2N180 | PNP | | 150 | −30 | −25 | 75 | 60T | | .7 | 37T | | | 2N1415 | 2 |
| 2N181 | PNP | | 250 | −30 | −38 | 75 | 60T | | .7 | 34T | | | 2N526 | 2 |
| 2N182 | NPN | | 100 | 25* | 10 | 85 | 25T* | | 2.5 | | 3T | 10 | 2N634A | 2 |
| 2N183 | NPN | | 100 | 25* | 10 | 85 | 50T* | | 5 | | 3T | 10 | 2N634A | 2 |
| 2N184 | NPN | | 100 | 25* | 10 | 85 | 100T* | | 10 | | 3T | 10 | 2N635A | 2 |
| 2N185 | PNP | | 150 | −20 | −150 | 75 | 35 | −100 | | 26 | 15 | −20 | 2N323 | 4, 4 |
| 2N186 | PNP | Obsolete | 100 | −25 | 200 | 85 | 24T* | −100 | .8T | 28 | −16 | −25 | 2N186A, 2N1413 | 1, 2 |
| 2N186A | PNP | AF Out | 200 | −25 | 200 | 85 | 24T* | −100 | .8T | 28 | −16 | −25 | 2N186A | 1 |
| 2N187 | PNP | Obsolete | 100 | −25 | 200 | 85 | 36T* | −100 | 1T | 30 | −16 | −25 | 2N187A, 2N1413 | 1, 2 |
| 2N187A | PNP | AF Out | 200 | −25 | 200 | 85 | 36T* | −100 | 1T | 30 | −16 | −25 | 2N187A | 1 |
| 2N188 | PNP | Obsolete | 100 | −25 | −200 | 85 | 54T* | 100 | 1.2T | 32 | −16 | −25 | 2N188A, 2N1413 | 1, 2 |
| 2N188A | PNP | AF Out | 200 | −25 | −200 | 85 | 54T* | 100 | 1.2T | 32 | −16 | −25 | 2N188A | 1 |
| 2N189 | PNP | AF | 75 | −25 | −50 | 85 | 24T* | 1 | .8T | 37 | −16 | −25 | 2N189, 2N1413 | 1, 2 |
| 2N190 | PNP | AF | 75 | −25 | −50 | 85 | 36T* | 1 | 1.0T | 39 | −16 | −25 | 2N190, 2N1414 | 1, 2 |
| 2N191 | PNP | AF | 75 | −25 | −50 | 85 | 54T* | 1 | 1.2T | 41 | −16 | −25 | 2N191, 2N1415 | 1, 2 |
| 2N192 | PNP | AF | 75 | −25 | −50 | 85 | 75T* | 1 | 1.5T | 43 | −16 | −25 | 2N192, 2N1175 | 1, 2 |
| 2N193 | NPN | | 50 | 15 | | 75 | 3.8 | 1 | 2 | | 40 | 15 | 2N1086 | 3 |
| 2N194 | NPN | | 50 | 15 | | 75 | 4.8 | 1 | 2 | 15T | 40 | 15 | 2N1086 | 3 |
| 2N194A | NPN | | 50 | 20 | 100 | 75 | 5 | 1 | 2 | 20 | 50 | 18 | 2N1087 | 3 |
| 2N206 | PNP | | 75 | −30 | −50 | 85 | 47T | | .8 | | | | 2N1414 | 2 |
| 2N207 | PNP | | 50 | −12 | −20 | 65 | 35 | 1 | 2T | | −15 | −12 | 2N1415, 2N323 | 2, 4 |
| 2N207A | PNP | | 50 | −12 | −20 | 65 | 35 | 1 | 2T | | −15 | −12 | 2N1415, 2N1175A | 2, 2 |
| 2N207B | PNP | | 50 | −12 | −20 | 65 | 35 | 1 | 2T | | −15 | −12 | 2N1415, 2N1175A | 2, 2 |
| 2N211 | NPN | | 50 | 10 | 50 | 75 | 3.8 | 1 | 2 | | 20 | 10 | 2N293, 2N1086 | 3, 3 |
| 2N212 | NPN | | 50 | 10 | 50 | 75 | 7 | 1 | 4 | 22T | 20 | 10 | 2N293, 2N1086 | 3, 3 |
| 2N213 | NPN | | 50 | 25 | 100 | 75 | 70 | 1 | | 39 | 200 | 40 | 2N169A | 3 |
| 2N213A | NPN | | 150 | 25 | 100 | 85 | 100 | 1 | 10 Kc | 38 | 50 | 20 | 2N636A | 2 |
| 2N214 | NPN | | 125 | 25 | 75 | 75 | 50 | 35 | .6 | 26 | 200 | 40 | 2N635A | 2 |
| 2N215 | PNP | | 150 | −30 | −50 | 85 | 44 | | .7 | 33T | −10 | −12 | 2N1415 | 2 |
| 2N216 | NPN | | 50 | 15 | 50 | 75 | 3.5 | 1 | 2 | 26T | 40 | 15 | 2N292, 2N1086 | 3, 3 |
| 2N217 | PNP | | 150 | −25 | −70 | 85 | 75* | | | 30T | | | 2N321, 2N396 | 4, 2 |
| 2N218 | PNP | | 80 | −16 | −15 | 85 | 48 | 1 | 6.8 | 30 | −6 | −12 | 2N394 | 2 |
| 2N219 | PNP | | 80 | −16 | −15 | 85 | 75 | .4 | 10 | 32 | −6 | −12 | 2N394 | 2 |
| 2N220 | PNP | | 50 | −10 | −2 | 85 | 65 | | .8 | 43 | | | 2N323, 2N1175A | 4, 2 |
| 2N223 | PNP | | 100 | −18 | −150 | 65 | 39 | −2 | .6T | | −20 | −9 | 2N323 | 4 |
| 2N224 | PNP | | 250 | −25* | 150 | 75 | 60* | −100 | .5T | | −25 | −12 | 2N321, 2N1175 | 4, 2 |
| 2N225 | PNP | | 250 | −25* | 150 | 75 | 60* | −100 | .5T | | −25 | −12 | 2N321, 2N1175 | 4, 2 |
| 2N226 | PNP | | 250 | −30* | 150 | 75 | 35* | −100 | .4T | | −25 | −30 | 2N321, 2N1415 | 4, 2 |
| 2N227 | PNP | | 250 | −30* | 150 | 75 | 35* | −100 | .4T | | −25 | −30 | 2N321, 2N1415 | 4, 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS | | | | ELECTRICAL PARAMETERS | | | | | | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ°C | MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | | |
| 2N228 | NPN | | 50 | 25 | 50 | 75 | 50 | 35 | .6 | 23 | 200 | 40 | 2N169, 2N634A | 3, 2 |
| 2N229 | NPN | | 50 | 12 | 40 | 75 | .9α | 1 | .55 | | 200 | 5 | 2N169 | 3 |
| 2N231 | PNP | | 9 | −4.5 | −3 | 55 | 19 | −.5 | 20 $f_{os}$ | | −3 | −5 | 2N711 | 8 |
| 2N232 | PNP | | 9 | −4.5 | −3 | 55 | 9 | −.5 | 30 $f_{os}$ | | −6 | −5 | 2N711 | 8 |
| 2N233 | NPN | | 50 | 10 | 50 | 75 | 3.0 | 1 | | | 100 | 10 | 2N448, 2N292 | 3, 3 |
| 2N233A | NPN | | 50 | 10 | 50 | 75 | 3.5 | 1 | | | 150 | 15 | 2N448, 2N292 | 3, 3 |
| 2N234 | PNP | | 25W | −30 | −3A | 90 | | | 8 Kc | 25 | −1 ma T | −25 | | |
| 2N234A | PNP | | 25W | −30 | −3A | 90 | | | 8 Kc | 25 | −1 ma T | −25 | | |
| 2N235 | PNP | | 25W | −40 | −3A | 90 | | | 7 Kc | 30 | | | | |
| 2N235A | PNP | | 25W | −40 | −3A | 90 | | | 7 Kc | 30 | | | | |
| 2N235B | PNP | | | 40 | 3.0A | 85 | | | | | 300 | 3 | | |
| 2N236 | PNP | | 25W | −40 | −3A | 95 | | | 6 Kc | 30 | −1 ma | −25 | | |
| 2N236A | PNP | | 25W | −40 | −3A | 95 | | | 6 Kc | 30 | −1 ma | −25 | | |
| 2N236B | PNP | | | 40 | 3.0A | 95 | | | | | 300 | 2 | | |
| 2N237 | PNP | | 150 | 45 | 20 | 85 | 50T | | .50 | | 10 | | 2N525 | 2 |
| 2N238 | PNP | | 50 | −20 | | 75 | | | | 37 | −20 | −20 | 2N323 | 4 |
| 2N240 | PNP | | 10 | −6 | −15 | | 16 | −.5 | 30 $f_{os}$ | | −3 | −5 | 2N711 | 8 |
| 2N241 | PNP | Obsolete | 100 | −25 | 200 | 85 | 73T* | 100 | 1.3T | 35T | −16 | −25 | 2N241A | 1 |
| 2N241A | PNP | AF Out | 200 | −25 | 200 | 85 | 73T* | 100 | 1.3T | 35T | −16 | −25 | 2N241A, 2N1415 | 1, 2 |
| 2N242 | PNP | | 20W | −45 | −2A | 85 | | | 5 Kc | 30 | −5 ma | −45 | | |
| 2N243 | NPN | | 750 | 60* | 60 | 150 | .9 | −5 | | 30 | 1 | 30 | | |
| 2N244 | NPN | | 750 | 60* | 60 | 150 | .961 | −5 | | 30 | 1 | 30 | | |
| 2N247 | PNP | | 80 | −12 | −10 | 85 | 60 | | 30 | 37 | −20 | −12 | | |
| 2N248 | PNP | | 30 | −25 | −5 | 85 | 20T* | .5 | 50T | | −10 | −12 | | |
| 2N249 | PNP | | 350 | −25 | −200 | 85 | 30 | −100 | | | −25 | −25 | | |
| 2N250 | PNP | | 12W | −30 | −2A | 80 | 30* | −.5A | | | −1 ma | −30 | | |
| 2N251 | PNP | | 12W | −60 | −2A | 80 | 30* | −.5A | | 30 | −2 ma | −60 | | |
| 2N252 | PNP | | 30 | −16 | −5 | 55 | | | | 28 | −10 | −12 | | |
| 2N253 | NPN | | 65 | 12 | 5 | 75 | | | | 32 | 3 | 9 | 2N293, 2N1121 | 3, 3 |
| 2N254 | NPN | | 65 | 20 | 5 | 75 | | | | | 3 | 9 | 2N293, 2N1121 | 3, 3 |
| 2N255 | PNP | | 1.5W | −15* | −3 | 85 | | | .2T | 19 | | | | |
| 2N255A | PNP | | 20W | 15 | 4A | 85 | 25* | 450 | | | 5 ma | 15 | | |
| 2N256 | PNP | | 1.5W | −30* | −3 | 85 | | | .2T | 22 | | | | |
| 2N256A | PNP | | 20W | 25 | 4A | 85 | 25* | 450 | | | 5 ma | −25 | | |
| 2N257 | PNP | | 2W | −40* | | 85 | 55T | .5A | 7 Kc | 30 | −2 ma | −40 | | |
| 2N260 | PNP | | 200 | −10* | −50 | 150 | 16T | 1 | 1.8T | 38T | .001T | −6 | 2N332, 2N1276 | 4, 4 |
| 2N260A | PNP | | 200 | −30* | −50 | 150 | 16T | 1 | 1.8T | 38T | .001T | −6 | 2N332 | 4 |
| 2N261 | PNP | | 200 | −75* | −50 | 150 | 10T | 1 | 1.8T | 36T | .001T | −6 | 2N332 | 4 |
| 2N262 | PNP | | 200 | −10* | −50 | 150 | 20T | 1 | 6T | 40T | .001T | −6 | 2N333 | 4 |
| 2N262A | PNP | | 200 | −30* | −50 | 150 | 20T | 1 | 6T | 40T | .001T | −6 | 2N333 | 4 |
| 2N265 | PNP | | 75 | −25 | −50 | 85 | 110T* | 1 | 1.5T | 45 | −16 | −25 | 2N265, 2N508 | 1, 2 |
| 2N267 | PNP | | 80 | −12 | −10 | 85 | 60 | | 30 | 37 | −20 | −12 | | |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVce BVcb* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ Vcb | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N268 | PNP | | 2W | −80* | | 85 | | | 6 Kc | 28 | −2 ma | −80 | | |
| 2N268A | PNP | | 2W | −60 | | 90 | 20* | 2A | | | −2 ma | −80 | | |
| 2N269 | PNP | | 120 | −24 | −100 | 85 | 35 | | 4 | | −5 | −12 | 2N404 | 2 |
| 2N270 | PNP | | 150 | −25 | −75 | 85 | 70 | 150 | | 35 | −10 | −25 | 2N321, 2N1415 | 4, 2 |
| 2N271 | PNP | | 150 | −10 | −200 | 85 | 45T | 1 | 10T | 29T | −5 | −12 | 2N394 | 2 |
| 2N271A | PNP | | 150 | −10 | −200 | 85 | 45T | 1 | 10T | 39T | −5 | −12 | 2N394 | 2 |
| 2N272 | PNP | | 150 | −24 | −100 | 85 | 60 | | 1T | 12T | −6T | −20 | 2N324 | 4 |
| 2N273 | PNP | | 150 | −30 | −100 | 85 | 10 | 50 | | 29 | −6T | −20 | 2N1098 | 2 |
| 2N274 | PNP | | 80 | −12 | −10 | 85 | 60T | 1 | 30T | 45T | −20 | −12 | | |
| 2N277 | PNP | | 55W | −40 | 12A | 95 | 85T | 1.2A | .5T | 34T | −.5 ma T | −30 | | |
| 2N278 | PNP | | 55W | −50 | 12A | 95 | 85T | 1.2A | .5T | 34T | −.5 ma T | −20 | | |
| 2N281 | PNP | | 165 | 32 | 250 | 75J | 70T* | | .90 | | 10 | | 2N1415 | 2 |
| 2N285 | PNP | | 25W | −40 | 3A | 95 | | | 6 Kc | 38 | −1 ma | −25 | | |
| 2N285A | PNP | | 25W | −40 | 3A | 95 | | | 6 Kc | 38 | −1 ma | −25 | | |
| 2N290 | PNP | | 55W | −70 | −12A | 95 | 72T* | 1.2A | .4T | 37T | −1 ma T | −60 | | |
| 2N291 | PNP | | 180 | −25 | −200 | 85 | 30* | 100 | | 31 | −25 | −25 | 2N320, 2N1414 | 4, 2 |
| 2N292 | NPN | IF | 65 | 15 | −20 | 85 | 8 | 1 | 5T | 25.5 | 5 | 15 | 2N292 | 3 |
| 2N293 | NPN | IF | 65 | 15 | −20 | 85 | 8 | 1 | 8T | 28 | 5 | 15 | 2N293 | 3 |
| 2N297 | PNP | | 35W | −50 | −5A | 95 | 40* | .5 | 5 Kc | | 3 ma | −60 | | |
| 2N297A | PNP | | 35W | −50 | −5A | 95 | 40* | .5 | 5 Kc | | 3 ma | −60 | | |
| 2N299 | PNP | | 20 | −4.5 | −5 | 85 | | | 90 $f_{os}$ | 20 | −3 | −5 | | |
| 2N300 | PNP | | 20 | −4.5 | −5 | 85 | 11 | .5 | 85 $f_{os}$ | | −3 | −5 | | |
| 2N301 | PNP | | 11W | −20 | −1.5A | 91 | 70T* | 1A | | 33T | −3 ma | −30 | | |
| 2N301A | PNP | | 11W | −30 | −1.5A | 91 | 70T* | 1A | | 33T | −3 ma | −30 | | |
| 2N302 | PNP | | 150 | −10 | −200 | 85 | 45T | | 7 | | −1T | −.12 | 2N186A | 1 |
| 2N303 | PNP | | 150 | −10 | −200 | 85 | 75T | | 14 | | −1T | −.12 | 2N186A | 1 |
| 2N306 | NPN | | 50 | 15 | | 75 | 25 | 1 | .6 | 34 | 50 | 20 | 2N292 | 3 |
| 2N307 | PNP | | 10W | −35 | −1A | 75 | 20 | 200 | 3 Kc | | 15 ma | −35 | | |
| 2N307A | PNP | | 17W | −35 | −2A | 75 | 20 | 200 | 3.5 Kc | 22 | 7 ma | −35 | | |
| 2N308 | PNP | | 30 | −20 | −5 | 55 | | | | 39 | −10 | −9 | | |
| 2N309 | PNP | | 30 | −20 | −5 | 55 | | | | 41 | −10 | −9 | | |
| 2N310 | PNP | | 30 | −30 | −5 | 55 | 28T | | | 37T | −10 | −9 | | |
| 2N311 | PNP | | 75 | −15 | | 85 | 25 | | | | −60 | −15 | 2N123 | 7 |
| 2N312 | NPN | | 75 | 15 | | 85 | 25 | | | | 60 | 15 | 2N167 | 3 |
| 2N313 | NPN | Obsolete | 65 | 15 | 20 | 85 | 25 | | 5 | 36 max | | | Use 2N292 | 3 |
| 2N314 | NPN | Obsolete | 65 | 15 | 20 | 85 | 25 | | 8 | 39 max | | | Use 2N293 | 3 |
| 2N315 | PNP | | 100 | −15 | −200 | 85 | 15 | 100 | 5T | | −2 | −5 | 2N396 | 2 |
| 2N315A | PNP-A | | 150 | 30 | | 100S | 35T* | | 5.00 | | 25 | | 2N396 | 2 |
| 2N316 | PNP | | 100 | −10 | −200 | 85 | 20 | 200 | 12T | | −2 | −5 | 2N397 | 2 |
| 2N316A | PNP-A | | 150 | 30 | | 100S | 35T* | | 12.0 | | 25 | | 2N397 | 2 |
| 2N317 | PNP | | 100 | −6 | −200 | 85 | 20 | 400 | 20T | | −2 | −5 | | |
| 2N318 | PNP | Photo | 50 | −12 | −20 | | | | .75T | | | | | |

| JEDEC No. | Type | Use | MAXIMUM RATINGS | | | | ELECTRICAL PARAMETERS | | | | | | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $P_C$ mw @ 25°C | $BV_{CE}$ $BV_{CB}$* | Ic ma | $T_J$°C | MIN. $h_{fe}$-$h_{FE}$* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ $V_{CB}$ | | |
| 2N319 | PNP | AF | 225 | −20 | −200 | 85 | 34T* | −20 | 2T | | −16 | −25 | 2N319, 2N1413 | 4, 2 |
| 2N320 | PNP | AF | 225 | −20 | −200 | 85 | 50T* | −20 | 2.5T | | −16 | −25 | 2N320, 2N1414 | 4, 2 |
| 2N321 | PNP | AF | 225 | −20 | −200 | 85 | 80T* | −20 | 3.0T | | −16 | −25 | 2N321, 2N1415 | 4, 2 |
| 2N322 | PNP | AF | 140 | −16 | −100 | 60 | 45T | −20 | 2T | | −16 | −16 | 2N322 | 4 |
| 2N323 | PNP | AF | 140 | −16 | −100 | 60 | 68T | −20 | 2.5T | | −16 | −16 | 2N323 | 4 |
| 2N324 | PNP | AF | 140 | −16 | −100 | 60 | 85T | −20 | 3.0T | | −16 | −16 | 2N324 | 4 |
| 2N325 | PNP | | 12W | −35 | −2A | 85 | 30* | −500 | .15 | | −500 | −30 | | |
| 2N326 | NPN | | 7W | 35 | 2A | 85 | 30* | 500 | .15 | | 500 | 30 | | |
| 2N327 | PNP | | 335 | −50* | −100 | 160 | 9 | .1 | .3T | 30 | −.1 | −30 | | |
| 2N327A | PNP | | 350 | −50* | −100 | 160 | 9* | 1 | .2T | | −.1 | −30 | | |
| 2N328 | PNP | | 335 | −35* | −100 | 160 | 18 | 1 | .35T | 32 | −.1 | −30 | | |
| 2N328A | PNP | | 350 | −50* | −100 | 160 | 18* | 1 | .3T | | −.1 | −30 | | |
| 2N329 | PNP | | 335 | −30* | −100 | 160 | 36 | 1 | .6T | 34 | −.1 | −30 | | |
| 2N329A | PNP | | 350 | −50* | −100 | 160 | 36* | 1 | .5T | | −.1 | −30 | | |
| 2N330 | PNP | | 335 | −45* | −50 | 160 | 9 | 1 | .5 | 30 | −.1 | −30 | | |
| 2N330A | PNP | | 350 | −50* | −100 | 160 | 25T | 1 | .5 | 34T | −.1 | −30 | | |
| 2N331 | PNP | | 200 | −30* | −200 | 85 | 50T | | | 44T | −16 | −30 | 2N1415 | 2 |
| 2N332 | NPN | Si AF | 150 | 45* | 25 | 200 | 9 | 1 | 10T | 14T | 2 | 30 | 2N332 | 4 |
| 2N332A | NPN | Si AF | 500 | 45 | 25 | 175 | 9 | | 2.5 | 11 | .500 | 30 | 2N332A | 4 |
| 2N333 | NPN | Si AF | 150 | 45* | 25 | 200 | 18 | 1 | 12* | 14T | 2 | 30 | 2N333 | 4 |
| 2N333A | NPN | Si AF | 500 | 45 | 25 | 175 | 18 | | 2.5 | 11 | .500 | 30 | 2N333A | 4 |
| 2N334 | NPN | Si AF | 150 | 45* | 25 | 200 | 18 | 1 | 8 | 13T | 2 | 30 | 2N334 | 4 |
| 2N334A | NPN | Si AF | 500 | 45 | 25 | 175 | 18 | | 8.0 | 12 | .500 | 30 | 2N334A | 4 |
| 2N335 | NPN | Si AF | 150 | 45* | 25 | 200 | 37 | 1 | 14* | 13T | 2 | 30 | 2N335 | 4 |
| 2N335A | NPN | Si AF | 500 | 45 | 25 | 175 | 37 | | 2.5 | 12 | .500 | 30 | 2N335 | 4 |
| 2N335B | NPN | Si AF | 500 | ⑫ | 25 | 175 | 37 | | 2.5 | 12T | .500 | 30 | 2N335B | 4 |
| 2N336 | NPN | Si AF | 150 | 45* | 25 | 200 | 76 | 1 | 15* | 12T | 2 | 30 | 2N336 | 4 |
| 2N336A | NPN | Si AF | 500 | 45 | 25 | 175 | 76 | | 2.5 | 12 | .500 | 30 | 2N336A | 4 |
| 2N337 | NPN | Si AF | 125 | 45* | 20 | 200 | 19 | 1 | 10 | | 1 | 20 | 2N337 | 4 |
| 2N337A | NPN-G | | 500 | 45 | 20 | 200S | 35T | | 30.0 | | .10 | | 2N337A | 4 |
| 2N338 | NPN | Si AF | 125 | 45* | 20 | 200 | 39 | 1 | 20 | | 1 | 20 | 2N338 | 4 |
| 2N338A | NPN-G | | 500 | 45 | 20 | 200S | 75T | | 45.0 | | .10 | | 2N338A | 4 |
| 2N339 | NPN | | 1W | 55* | 60 | 150 | .9α | −5 | | 30 | 1 | 30 | 2N656A | 2 |
| 2N339A | NPN | | 1000 | 60 | | 200S | 53T | | | | 1.0 | | 2N656A | 2 |
| 2N340 | NPN | | 1W | 85* | 60 | 150 | .9α | −5 | | 30 | 1 | 30 | 2N657A | 2 |
| 2N340A | NPN | | 1000 | 85 | | 150J | 50T | | | 30 | 1.0 | | 2N657A | 2 |
| 2N341 | NPN | | 1W | 125* | 60 | 150 | .9α | −5 | | 30 | 1 | 30 | 2N657A | 2 |
| 2N341A | NPN | | 1000 | 125 | | 200S | 53T | | | 30 | 1.0 | | 2N657A | 2 |
| 2N342 | NPN | | 1W | 60* | 60 | 150 | .9α | −5 | | 30 | 1 | 30 | 2N656A | 2 |
| 2N342A | NPN-G | | 1000 | 85 | 60 | 150J | 20T | | | 30 | 1.0 | | 2N657A | 2 |
| 2N342B | GD | | 1000 | 85 | 60 | 150J | 21T | | 6.00 | | 50 | | 2N335B, 2N657A | 4, 2 |
| 2N343 | NPN | | 1W | 60* | 60 | 150 | .966α | −5 | | 30 | 1 | 30 | 2N656A | 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N343B | GD | | 1000 | 65 | 60 | 150J | 59T | | 6.00 | | 100 | | 2N335B, 2N656A | 4, 2 |
| 2N344 | PNP | | 40 | −5 | −5 | 85 | 11 | | 30 fos | | −3 | −5 | 2N962 | 8 |
| 2N345 | PNP | | 40 | −5 | −5 | 85 | 25 | | 30 fos | | −3 | −5 | 2N962 | 8 |
| 2N346 | PNP | | 40 | −5 | −5 | 85 | 10 | | 60 fos | | −3 | −5 | 2N962 | 8 |
| 2N348 | NPN-G | | 750 | 90 | 50 | 150J | 24T | | 3.00 | 35 | 6.0 | | 2N292 | 3 |
| 2N349 | NPN-G | | 750 | 125 | 40 | 150J | 19T | | 3.00 | 34 | 8.0 | | 2N293 | 3 |
| 2N350 | PNP | | 10W | −40* | −3A | 90 | 20* | −700 | 5 Kc | 30 | −3 ma | −30 | | |
| 2N351 | PNP | | 10W | −40* | −3A | 90 | 25* | −700 | 5 Kc | 32 | −3 ma | −30 | | |
| 2N352 | PNP | | 25W | −40 | −2A | 100 | 30 | −1A | 10 Kc | 30 | −5 ma | −1 @ 85°C | | |
| 2N353 | PNP | | 30W | −40 | −2A | 100 | 40 | −1A | 7 Kc | 30 | −5 ma | −1 @ 85°C | | |
| 2N354 | PNP | | 150 | −25* | −50 | 140 | 9 | 1 | 8 fos | | −.1 | −10 | | |
| 2N355 | PNP | | 150 | −10* | −50 | 140 | 9 | 1 | 8 fos | | −.1 | −10 | | |
| 2N356 | NPN | | 120 | 18 | 100 | 85 | 20 | 100 | 3T | | 5 | 5 | 2N634A | 2 |
| 2N356A | NPN-A | | 150 | 30 | | 100S | 35T* | | 3.00 | | 25 | | 2N634 | 2 |
| 2N357 | NPN | | 120 | 15 | 100 | 85 | 20 | 200 | 6T | | 5 | 5 | 2N634A | 2 |
| 2N357A | NPN-A | | 150 | 30 | | 100S | 40T* | | 6.00 | | 25 | | 2N634A | 2 |
| 2N358 | NPN | | 120 | 12 | 100 | 85 | 20 | 300 | 9T | | 5 | 5 | 2N635A | 2 |
| 2N358A | NPN-A | | 150 | 30 | | 100S | 40T* | | 9.00 | | 25 | | 2N635A | 2 |
| 2N359 | PNP-A | | 150 | 20 | 400 | 85 | 300T | | 1.50 | 40 | 10 | | 2N508 | 2 |
| 2N360 | PNP-A | | 150 | | 400 | 85 | 150T | | 1.20 | 37 | 10 | | 2N1415 | 2 |
| 2N361 | PNP-A | | 150 | 20 | 400 | 85 | 75T | | 1.00 | 34 | 10 | | 2N1413 | 2 |
| 2N362 | PNP-A | | 150 | 18 | 100 | 85 | 90T | | 2.00 | 42 | 15 | | 2N324 | 4 |
| 2N363 | PNP-A | | 150 | 32 | 100 | 85 | 50T | | 1.50 | 39 | 15 | | 2N1414 | 2 |
| 2N364 | NPN | | 150 | 30* | 50 | 85 | 9 | −1 | 1 | | 10 | 30 | 2N1694 | 2 |
| 2N365 | NPN | | 150 | 30* | 50 | 85 | 19 | −1 | 1 | | 10 | 30 | 2N1694 | 2 |
| 2N366 | NPN | | 150 | 30* | 50 | 85 | 49 | −1 | 1 | | 10 | 30 | | |
| 2N367 | NPN | | 100 | −30* | −50 | 75 | 9 | 1 | .3 | | −30 | −30 | 2N1413 | 2 |
| 2N368 | PNP | | 150 | −30* | −50 | 75 | 19 | 1 | .4 | | −20 | −30 | 2N1413 | 2 |
| 2N369 | PNP | | 150 | −30* | −50 | 75 | 49 | 1 | .5 | | −20 | −30 | 2N1415 | 2 |
| 2N370 | PNP | | 80 | −24* | −20 | 85 | 60T | 1 | 30T | 31M | −10 | −12 | | |
| 2N371 | PNP | | 80 | −24* | −20 | 85 | .984T | 1 | 30T | 17.6M | −10 | −12 | | |
| 2N372 | PNP | | 80 | −24* | −20 | 85 | 60T | 1 | 30T | 12.5M | −10 | −12 | | |
| 2N373 | PNP | | 80 | −24* | −10 | 85 | 60T | 1 | 30T | 40T | −16 | −12 | | |
| 2N374 | PNP | | 80 | −24* | −10 | 85 | 60T | 1 | 30T | 40T | −16 | −12 | | |
| 2N375 | PNP | | 45W | −60 | −3A | 95 | 35 | 1A | 7 Kc | | −3 ma | −60 | | |
| 2N376 | PNP | | 10W | −40* | −3A | 90 | 60T | 1A | 5 Kc | 35T | | | | |
| 2N377 | NPN | Sw | 150 | 20 | 200 | 100 | 20* | 30 | 6T | | 5 | 1 | 2N377 | 2 |
| 2N377A | NPN | | 150 | 40 | 200 | 100 | 20* | 200 | 6T | | 40 | 40 | 2N377 | 2 |
| 2N378 | PNP | | 50W | −40 | −5A | 100 | 15* | 2A | 5 Kc | | −500 | −25 | | |
| 2N379 | PNP | | 50W | −80 | −5A | 100 | 20* | 2A | 5 Kc | | −500 | −25 | | |
| 2N380 | PNP | | 50W | −60 | −5A | 100 | 30* | 2A | 7 Kc | | −500 | −25 | | |
| 2N381 | PNP | | 200 | −25 | −200 | 85 | 50T | 20 | 1.2T | 31T | −10T | −25 | 2N320, 2N1924 | 4, 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVce BVcb* | Ic ma | Tj°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ Vcb | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N382 | PNP | | 200 | −25 | −200 | 85 | 75T | 20 | 1.5T | 33T | −10T | −25 | 2N321, 2N1927 | 4, 2 |
| 2N383 | PNP | | 200 | −25 | −200 | 85 | 100T | 20 | 1.8T | 35T | −10T | −25 | 2N321, 2N1175 | 4, 2 |
| 2N384 | PNP | | 120 | −30 | −10 | 85 | 60T | 1.5 | 100T | 15 | −16 | −12 | | |
| 2N385 | NPN | | 150 | 25 | 200 | 100 | 30* | 30 | 4 | | 35 | 25 | 2N385 | 2 |
| 2N385A | NPN-A | | 150 | 40 | 200 | 100J | 70T | | 8.00 | | 40 | | 2N385A | 2 |
| 2N386 | PNP | | 12.5W | −60 | −3A | 100 | 20 | −2.5A | 7 Kc | | −5 ma | −60 | | |
| 2N387 | PNP | | 12.5W | −80 | −3A | 100 | 20 | −2.5A | 6 Kc | | −5 ma | −80 | | |
| 2N388 | NPN | Sw | 150 | 20 | 200 | 100 | 60* | 30 | 5 | | 10 | 25 | 2N388 | 2 |
| 2N388A | NPN | | 150 | 40 | 200 | 100 | 30* | 200 | 5 | | 40 | 40 | 2N388 | 2 |
| 2N389 | NPN | | 85W | 60 | | 200 | 12 | 1A | | | 10 ma | 60 @ 100°C | | |
| 2N392 | PNP | | 70W | −60* | −5A | 95 | 60 | 3A | 6 Kc | | −8 ma | −60 | | |
| 2N393 | PNP | | 50 | −6 | −50 | 85 | 20* | −50 | 40 $f_{\alpha b}$ | | −5 | −5 | 2N711A | 8 |
| 2N394 | PNP | Sw | 150 | −10 | −200 | 85 | 20* | −10 | 4 | | −6 | −10 | 2N394 | 2 |
| 2N394A | PNP-A | | 150 | 30 | 200 | 100S | 70T* | | 7.00 | | 6.0 | | 2N394A | 2 |
| 2N395 | PNP | Sw | 200 | −15 | −200 | 100 | 20* | −10 | 3 | | −6 | −15 | 2N395 | 2 |
| 2N396 | PNP | Sw | 200 | −20 | −200 | 100 | 30* | −10 | 5 | | −6 | −20 | 2N396 | 2 |
| 2N396A | PNP | Sw | 200 | 20 | 200 | 100 | 30* | 10 | 5 | | −6 | −20 | 2N396A | 2 |
| 2N397 | PNP | Sw | 200 | −15 | −200 | 100 | 40* | −10 | 10 | | −6 | −15 | 2N397 | 2 |
| 2N398 | PNP | | 50 | −105 | −110 | 85 | 20* | −5 ma | | | −14 | −2.5 | 2N1614 | 1 |
| 2N398A | PNP | | 150 | 105 | | 100J | 20T | | 1.00 | | | | 2N1924 | 2 |
| 2N399 | PNP | | 25W | −40 | −3A | 90 | | | 8 Kc | 33T | −1 ma | −25 | | |
| 2N400 | PNP | | 25W | −40 | 3.0A | 95 | 1 | | | 40 | 2 ma | −25 | | |
| 2N401 | PNP | | 25W | −40 | −3A | 90 | | | 8 Kc | 30T | −1 ma | −25 | | |
| 2N402 | PNP | | 180 | −20 | −150 | 85 | .96αT | 1 | .6T | 37T | −15 | −20 | 2N320, 2N1413 | 4, 2 |
| 2N403 | PNP | | 180 | −20 | −200 | 85 | .97αT | 1 | .85T | 32 | −15 | −20 | 2N319, 2N1413 | 4, 2 |
| 2N404 | PNP | Sw | 120 | −24 | −100 | 85 | | | 4 | | −5 | −12 | 2N404 | 2 |
| 2N404A | PNP-A | Sw | 150 | 40 | 150 | 100 | | | 8.00 | | 20 | | 2N404A | 2 |
| 2N405 | PNP | | 150 | −18 | −35 | 85 | 35T* | 1 | .65T | 43T | −14 | −12 | 2N322 | 4 |
| 2N406 | PNP | | 150 | −18 | −35 | 85 | 35T* | 1 | .65T | 43T | −14 | −12 | 2N322 | 4 |
| 2N407 | PNP | | 150 | −18 | −70 | 85 | 65T* | −50 | | 33T | −14 | −12 | 2N323 | 4 |
| 2N408 | PNP | | 150 | −18 | −70 | 85 | 65T* | −50 | | 33T | −14 | −12 | 2N323 | 4 |
| 2N409 | PNP | | 80 | −13 | −15 | 85 | .98αT | 1 | 6.7T | 38T | −10 | −13 | 2N394 | 2 |
| 2N410 | PNP | | 80 | −13 | −15 | 85 | .98αT | 1 | 6.7T | 38T | −10 | −13 | 2N394 | 2 |
| 2N411 | PNP | | 80 | −13 | −15 | 85 | 75T | .6 | | 32T | −10 | −13 | 2N397 | 2 |
| 2N412 | PNP | | 80 | −13 | −15 | 85 | 75T | .6 | | 32T | −10 | −13 | 2N397 | 2 |
| 2N413 | PNP | IF Sw | 150 | −18 | −200 | | 30 | | 6T | | −5 | −12 | 2N413 | 2 |
| 2N413A | PNP | | 150 | −15 | −200 | 85 | 30T | 1 | 2.5T | 33T | −5 | −12 | 2N394 | 2 |
| 2N414 | PNP | IF Sw | 150 | −15 | −200 | | 60 | | 7T | | −5 | −12 | 2N414 | 2 |
| 2N414A | PNP | | 150 | −15 | −200 | 85 | 60T | 1 | 7T | 35T | −5 | −12 | 2N394, 2N414 | 2 |
| 2N415 | PNP | | 150 | −10 | −200 | 85 | 80T | 1 | 10T | 30T | −5 | −12 | 2N394 | 2 |
| 2N415A | PNP | | 150 | −10 | −200 | 85 | 80T | 1 | 10T | 39T | −5 | −12 | 2N394 | 2 |
| 2N416 | PNP | | 150 | −12 | −200 | 85 | 80T | 1 | 10T | 20T | −5 | −12 | 2N394 | 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N417 | PNP | | 150 | −10 | −200 | 85 | 140T | 1 | 20T | 27T | −5 | −12 | 2N394 | 2 |
| 2N418 | PNP | | 25W | 80 | 5A | 100 | 40* | 4A | 400 Kc | | 15 ma | −60 | | |
| 2N420 | PNP | | 25W | 45 | 5A | 100 | 40* | 4A | 400 Kc | 10 m | 10 ma | −25 | | |
| 2N420A | PNP | | 25W | 70 | 5A | 100 | 40* | 4A | 400 Kc | | 15 ma | −60 | | |
| 2N422 | PNP | | 150 | −20 | −100 | 85 | 50T | 1 | .8T | 38T | −15 | −20 | 2N320, 2N1175A | 4, 2 |
| 2N425 | PNP | | 150 | −20 | −400 | 85 | 20* | 1 | 2.5 | | −25 | −30 | 2N394 | 2 |
| 2N426 | PNP | | 150 | −18 | −400 | 85 | 30* | 1 | 3 | | −25 | −30 | 2N395 | 2 |
| 2N427 | PNP | | 150 | −15 | −400 | 85 | 40* | 1 | 5 | | −25 | −30 | 2N396, 2N427 | 2, 4 |
| 2N428 | PNP | | 150 | −12 | −400 | 85 | 60* | 1 | 10 | | −25 | −30 | 2N397 | 2 |
| 2N438 | NPN | | 100 | 25 | | 85 | 20* | 50 | 2.5 | | 10 | 25 | 2N634A | 2 |
| 2N438A | NPN | | 150 | 25 | | 85 | 20* | 50 | 2.5 | | 10 | 25 | 2N634A | 2 |
| 2N439 | NPN | | 100 | 20 | | 85 | 30 | 50 | 5 | | 10 | 25 | 2N634A | 2 |
| 2N439A | NPN | | 150 | 20 | | 85 | 30* | 50 | 5 | | 10 | 25 | 2N634A | 2 |
| 2N440 | NPN | | 100 | 15 | | 85 | 40* | 50 | 10 | | 10 | 25 | 2N635A | 2 |
| 2N440A | NPN | | 150 | 15 | | 85 | 40* | 50 | 10 | | 10 | 25 | 2N635A | 2 |
| 2N444 | NPN | | 120 | 15 | | 85 | 15T | | .5T | | 2T | 10 | 2N634A | 2 |
| 2N444A | NPN-A | | 150 | 40 | | 100S | 30T | | .50 | | 25 | | 2N634A | 2 |
| 2N445 | NPN | | 100 | 12 | | 85 | 35T | | 2T | | 2T | 10 | 2N634A | 2 |
| 2N445A | NPN-A | | 150 | 30 | | 100S | 90T* | | 2.00 | | 25 | | 2N634A | 2 |
| 2N446 | NPN | | 100 | 10 | | 85 | 60T | | 5T | | 2T | 10 | 2N634A | 2 |
| 2N446A | NPN-A | | 150 | 30 | | 100S | 150T* | | 5.00 | | 25 | | 2N634A | 2 |
| 2N447 | NPN | | 100 | 6 | | 85 | 125T | | 9T | | 2T | 10 | 2N635A | 2 |
| 2N447A | NPN-A | | 150 | 30 | | 100S | 200T* | | 9.00 | | 25 | | 2N635A | 2 |
| 2N448 | NPN | IF | 65 | 15 | 20 | 85 | 8* | 1 | 5T | 23 | 5 | 15 | 2N448, 2N292 | 3, 3 |
| 2N449 | NPN | IF | 65 | 15 | 20 | 85 | 34* | 1 | 8T | 24.5 | 5 | 15 | 2N449, 2N293 | 3, 3 |
| 2N450 | PNP | Sw | 150 | −12 | −125 | 85 | 30* | −10 | 5 | | −6 | −12 | 2N450, 2N394A | 7, 2 |
| 2N456 | PNP | | 50 | −40 | 5A | 95 | 130T* | 1A | | | −2 ma | −40 | | |
| 2N457 | PNP | | 50 | −60 | 5A | 95 | 130T* | 1A | | | −2 ma | −60 | | |
| 2N458 | PNP | | 50 | −80 | 5A | 95 | 130T* | 1A | | | −2 ma | −80 | | |
| 2N459 | PNP | | 50 | −60 | 5A | 100 | 20* | 2A | 5 Kc | | 100 ma | −60 | | |
| 2N460 | PNP | | 200 | −45* | −400 | 100 | .94α | 1 | 1.2T | 34T | −15 | −45 | 2N524 | 2 |
| 2N461 | PNP | | 200 | −45* | −400 | 100 | .97α | 1 | 1.2T | 37T | −15 | −45 | 2N461 | 2 |
| 2N462 | PNP | | 150 | −40* | −200 | 75 | 20* | −200 | .5 | | −35 | −35 | 2N1614, 2N527 | 1, 2 |
| 2N463 | PNP | | 37.5W | −60 | 5A | 100 | 20* | −2A | 4 mc | | −300 | −40 | | |
| 2N464 | PNP | | 150 | −40 | −100 | 85 | 14 | 1 | .7T | 40T | −15 | −20 | 2N1614, 2N527 | 1, 2 |
| 2N465 | PNP | | 150 | −30 | −100 | 85 | 27 | 1 | .8T | 42T | −15 | −20 | 2N1414, 2N1924 | 2, 2 |
| 2N466 | PNP | | 150 | −20 | −100 | 85 | 56 | 1 | 1T | 44T | −15 | −20 | 2N321, 2N1175 | 4, 2 |
| 2N467 | PNP | | 150 | −15 | −100 | 85 | 112 | 1 | 1.2T | 45T | −15 | −20 | 2N508 | 2 |
| 2N469 | PNP | | 50 | | | 75 | 10 | 1 | 1T | | −50 | −6 | | |
| 2N470 | NPN-GD | | 200 | 15 | | 175A | 16T | | | | | | 2N335 | 4 |
| 2N471 | NPN-GD | | 200 | 30 | | 175A | 16T | | | | | | 2N335 | 4 |
| 2N471A | NPN-GD | | 200 | 30 | | 175A | 25T | | | | | | 2N335 | 4 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N472 | NPN-GD | | 200 | 45 | | 175A | 16T | | | | | | 2N335 | 4 |
| 2N472A | PNP-A | | 200 | 45 | | 100S | 18T | | 8.00 | | 50 | | 2N335 | 4 |
| 2N473 | NPN-GD | | 200 | 15 | | 175A | 30T | | 11.0 | | | | 2N333 | 4 |
| 2N474 | NPN-GD | | 200 | 30 | | 175A | 30T | | 11.0 | | | | 2N333 | 4 |
| 2N474A | NPN-GD | | 200 | 30 | | 175A | 50T | | 11.0 | | | | 2N333 | 4 |
| 2N475 | NPN-GD | | 200 | 45 | | 175A | 30T | | 11.0 | | | | 2N333 | 4 |
| 2N475A | NPN | | 200 | 45 | | 200S | 35T | | 8.00 | | 50 | | 2N533 | 4 |
| 2N478 | NPN-GD | | 200 | 15 | | 175A | 60T | | 11.0 | | | | 4C30 | 4 |
| 2N479 | NPN-GD | | 200 | 30 | | 175A | 60T | | 11.0 | | | | 4C30 | 4 |
| 2N479A | NPN-GD | | 200 | 30 | | 175A | 80T | | | | | | 2N335 | 4 |
| 2N480 | NPN-GD | | 200 | 45 | | 175A | 60T | | 11.0 | | .50 | | 2N335 | 4 |
| 2N480A | NPN-GD | | 200 | 45 | | 175A | 60T | | 11.0 | | | | 2N335 | 4 |
| 2N481 | PNP | | 150 | −12 | −20 | 85 | 50T | 1 | 3T | | −10 | −12 | 2N395 | 2 |
| 2N482 | PNP | | 150 | −12 | −20 | 85 | 50T | 1 | 3.5T | | −10 | −12 | 2N395 | 2 |
| 2N483 | PNP | | 150 | −12 | −20 | 85 | 60T | 1 | 5.5T | | −10 | −12 | 2N394 | 2 |
| 2N484 | PNP | | 150 | −12 | −20 | 85 | 90T | 1 | 10T | | −10 | −12 | 2N394 | 2 |
| 2N485 | PNP | | 150 | −12 | −10 | 85 | 50T | 1 | 7.5T | | −10 | −12 | 2N394 | 2 |
| 2N486 | PNP | | 150 | −12 | −10 | 85 | 100T | 1 | 12T | | −10 | −12 | 2N394 | 2 |
| 2N489 | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N489 | 5 |
| 2N489A | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N489A | 5 |
| 2N489B | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N489B | 5 |
| 2N490 | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N490 | 5 |
| 2N490A | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N490A | 5 |
| 2N490B | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N490B | 5 |
| 2N491 | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N491 | 5 |
| 2N491A | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N491A | 5 |
| 2N491B | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N491B | 5 |
| 2N492 | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N492 | 5 |
| 2N492A | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N492A | 5 |
| 2N492B | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N492B | 5 |
| 2N493 | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N493 | 5 |
| 2N493A | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N493A | 5 |
| 2N493B | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N493B | 5 |
| 2N494 | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N494 | 5 |
| 2N494A | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N494A | 5 |
| 2N494B | | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N494B | 5 |
| 2N495 | PNP | | 150 | −25 | −50 | 140 | 9 | 1 | 8 $f_{os}$ | | −.1 | −10 | | |
| 2N496 | PNP | | 150 | −10 | −50 | 140 | 9 | 1 | 8 $f_{os}$ | | −.1 | −10 | | |
| 2N497 | NPN | Si AF | 4W | 60 | 500 | 200 | 12* | 200 | | | 10 | 30 | 2N497 | 2 |
| 2N497A | NPN | Si AF | 5W | 60 | 500 | 200 | 12* | 200 | | | 10 | 30 | 2N497A | 2 |
| 2N498 | NPN | Si AF | 4W | 100 | 500 | 200 | 12* | 200 | | | 10 | 30 | 2N498 | 2 |
| 2N498A | NPN | Si AF | 5W | 100 | 500 | 200 | 12* | 200 | | | 10 | 30 | 2N498A | 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVce BVcb* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ Vcb | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N499 | PNP | | 30 @ 45°C | −18 | −50 | 85 | 6 | 2 | | 10 | 100 | −30 | 2N994 | 8 |
| 2N500 | PNP | | 50 @ 45°C | −15 | | 85 | | | | | 100 | −20 | | |
| 2N501 | PNP | | 25 @ 45°C | −15* | −50 | 85 | 20* | −10 | | | 100 | −15 | 2N960 | 8 |
| 2N501A | PNP | | 25 @ 45°C | −15* | −50 | 100 | 20* | −10 | | 8 | 25 | −15 | 2N994 | 8 |
| 2N502 | PNP | | 25 @ 41°C | −20 | | 85 | 9 | 2 | 200 | 8 | −100 | −20 | 2N994 | 8 |
| 2N502A | PNP | | 25 @ 45°C | −30* | | 100 | 9 | 2 | | | 100 | −30 | | |
| 2N503 | PNP | | 25 @ 41°C | −20 | −50 | 85 | 9 | 2 | 100 | 11 | −100 | −20 | 2N994 | 8 |
| 2N505 | PNP | | 125 | 40 | 250 | 85J | 40T | | 8.00 | | | | 2N396 | 2 |
| 2N506 | PNP | | 50 | −40* | −100 | 85 | 25 | −10 | .6 | | −15 | −30 | 2N320, 2N413 | 4, 2 |
| 2N507 | NPN | | 50 | 40 | 100 | 85 | 25 | 10 | .6 | | 15 | 30 | | |
| 2N508 | PNP | AF Out | 140 | −16 | −100 | 85 | 125T* | −20 | 3.5T | | −16 | −16 | 2N508 | 2 |
| 2N509 | PNP | | 225 | −30* | −40 | 100 | .96α | 10 | 750T | | −5 | −20 | | |
| 2N514 | PNP | | 80W | −40 | −25A | 95 | 12* | −25 | | | −2.0 | −20 | | |
| 2N514A | PNP | | 80W | −60 | −25A | 95 | 12* | −25 | | | 2.0 | −30 | | |
| 2N514B | PNP | | 80W | −80 | −25A | 95 | 12* | −25 | 7.0T | | −2.0 | −40 | | |
| 2N515 | NPN | | 50 | 18 | 10 | 75 | 4 | 1 | 2 | 23 | 50 | 18 | 2N293 | 3 |
| 2N516 | NPN | | 50 | 18 | 10 | 75 | 4 | 1 | 2 | 25 | 50 | 18 | 2N293 | 3 |
| 2N517 | NPN | | 50 | 18 | 10 | 75 | 4 | 1 | 2 | 27 | 50 | 18 | 2N1121 | 3 |
| 2N519 | PNP | | 100 | −15 | | 85 | 15 | 1 | .5 | | −2 | −5 | 2N394 | 2 |
| 2N519A | NPN-A | | 150 | 25 | | 100S | 35T* | | .50 | | 25 | | 2N394 | 2 |
| 2N520 | PNP | | 100 | −12 | | 85 | 20 | 1 | 3 | | −2 | −5 | 2N394 | 2 |
| 2N520A | PNP-A | | 150 | 25 | | 100S | 100T* | | 3.00 | | 25 | | 2N394 | 2 |
| 2N521 | PNP | | 100 | −10 | | 85 | 35 | 1 | 8 | | −2 | −5 | 2N397 | 2 |
| 2N521A | PNP-A | | 150 | 25 | | 100S | 150T* | | 8.00 | | 25 | | 2N397 | 2 |
| 2N522 | PNP | | 100 | −8 | | 85 | 60 | 1 | 15 | | −2 | −5 | | |
| 2N523 | PNP | | 100 | −6 | | 85 | 80 | 1 | 21 | | −2 | −5 | | |
| 2N524 | PNP | AF | 225 | −30 | −500 | 100 | 16 | −1 | .8 | | −10 | −30 | 2N524 | 2 |
| 2N525 | PNP | AF | 225 | −30 | −500 | 100 | 30 | −1 | 1 | | −10 | −30 | 2N525 | 2 |
| 2N526 | PNP | AF | 225 | −30 | −500 | 100 | 44 | −1 | 1.3 | | −10 | −30 | 2N526 | 2 |
| 2N527 | PNP | AF | 225 | −30 | −500 | 100 | 60 | −1 | 1.5 | | −10 | −30 | 2N527 | 2 |
| 2N528 | PNP | | 2.5W | −40 | | 100 | 20* | −0.5 | | | −15 | −30 | | |
| 2N529 | PNP-NPN | | 100 | 15 | | 85 | 15 | 1 | 2.5T | | 5 | 5 | | |
| 2N530 | PNP-NPN | | 100 | 15 | | 85 | 20 | 1 | 3T | | 5 | 5 | 2N394 | 2 |
| 2N531 | PNP-NPN | | 100 | 15 | | 85 | 25 | 1 | 3.5T | | 5 | 5 | 2N395 | 2 |
| 2N532 | PNP-NPN | | 100 | 15 | | 85 | 30 | 1 | 4T | | 5 | 5 | 2N395 | 2 |
| 2N533 | PNP-NPN | | 100 | 15 | | 85 | 35 | 1 | 4.5T | | 5 | 5 | | |
| 2N534 | PNP | | 25 @ 50°C | −50 | −25 | 65 | 35 | −1 | | | −15 | −50 | 2N1057, 2N1924 | 1, 2 |
| 2N535 | PNP | | 50 | −20 | −20 | 85 | 35 | −1 | 2T | | −10 | −12 | 2N1415, 2N1175A | 2, 2 |
| 2N535A | PNP | | 50 | −20 | −20 | 85 | 35 | −1 | 2T | | −10 | −12 | 2N1415, 2N1175A | 2, 2 |
| 2N535B | PNP | | 50 | −20 | −20 | 85 | 35 | −1 | 2T | | −10 | −12 | 2N508, 2N1175A | 2, 2 |
| 2N536 | PNP | | 50 | −20 | −30 | 85 | 100* | −30 | 1 | | −10 | −12 | 2N508 | 2 |
| 2N538 | PNP | | 10W @ 70°C | −80* | | 95 | 40 | 2A | 8T Kc | | −20 ma | −80 | | |

| JEDEC No. | Type | Use | MAXIMUM RATINGS | | | | ELECTRICAL PARAMETERS | | | | | | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Pc mw @ 25°C | $BV_{CE}$ $BV_{CB}$* | Ic ma | $T_J$°C | MIN. $h_{fe}$-$h_{FE}$* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ $V_{CB}$ | | |
| 2N538A | PNP | | 10W @ 70°C | −80* | | 95 | 40 | 2A | 8T Kc | | −20 ma | −80 | | |
| 2N539 | PNP | | 10W @ 70°C | −80* | | 95 | 27 | 2A | 7T Kc | | −20 ma | −80 | | |
| 2N539A | PNP | | 10W @ 70°C | −80 | | 95 | 27 | 2A | 7T Kc | | −20 ma | −80 | | |
| 2N540 | PNP | | 10W @ 70°C | −80 | | 95 | 18 | 2A | 6T Kc | | −20 | −80 | | |
| 2N540A | PNP | | 10W @ 70°C | −80 | | 95 | 18 | 2A | 6T Kc | | −20 | −80 | | |
| 2N544 | PNP | | 80 | −24* | −10 | 85 | 60T | 1 | 30T | 30.4 | −16 | −12 | | |
| 2N545 | NPN-GD | | 5000 | 60 | | 175A | 25T* | | 4.00 | | | | 2N497A | 2 |
| 2N546 | NPN-GD | | 5000 | 30 | | 175A | 25T* | | 4.00 | | | | 2N497A | 2 |
| 2N547 | NPN-GD | | 5000 | 60 | | 175A | 35T* | | 4.00 | | | | 2N656A | 2 |
| 2N548 | NPN-GD | | 5000 | 30 | | 175A | 35T* | | 4.00 | | | | 2N656A | 2 |
| 2N549 | NPN-GD | | 5000 | 60 | | 175A | 35T* | | 4.00 | | | | 2N656A | 2 |
| 2N550 | NPN-GD | | 5000 | 30 | | 175A | 35T* | | 4.00 | | | | 2N656A | 2 |
| 2N551 | NPN-GD | | 5000 | 60 | | 175A | 30T* | | 4.00 | | | | 2N656A | 2 |
| 2N552 | NPN-GD | | 5000 | 30 | | 175A | 30T* | | 4.00 | | | | 2N656A | 2 |
| 2N553 | PNP | | 12W @ 71°C | −80* | −4A | 95 | 40 | −.5A | 20 Kc | | −2 ma | −60 | | |
| 2N554 | PNP | | 10W @ 80°C | −40* | −3A | 90 | 30T* | −.5A | 8T Kc | 20 | −50T | −2 | | |
| 2N555 | PNP | | 10W @ 80°C | −30 | −3A | 90 | 20 | −.5A | 5 Kc | 34T | −7 ma | −30 | | |
| 2N556 | NPN | | 100 | 25* | 200 | 85 | 35* | 1 | | | | | 2N634A | 2 |
| 2N557 | NPN | | 100 | 20* | 200 | 85 | 20* | 1 | | | | | 2N634A | 2 |
| 2N558 | NPN | | 100 | 15* | 200 | 75 | 60* | 1 | | | | | 2N635A | 2 |
| 2N559 | PNP | | 150 | −15 | −50 | 100 | 25* | 10 | | | −50 | −5 @ 65°C | 2N705 | 8 |
| 2N560 | NPN | | | .50 | | | 20* | −100 | | | .10 | −20 | 2N1613 | 4 |
| 2N561 | PNP | | 50W | −50 | −5A | 100 | 65T | −1A | .5 | 24.6 | −500 | −30 | | |
| 2N563 | PNP | | 150 | −25 | −300 | 85 | 10* | 1 | .8T | | −5 | −10 | 2N44 | 1 |
| 2N564 | PNP | | 120 | −25 | −300 | 85 | 10* | 1 | .8T | | −5 | −10 | 2N524 | 2 |
| 2N565 | PNP | | 150 | −25 | −300 | 85 | 30* | 1 | 1T | | −5 | −10 | 2N43 | 1 |
| 2N566 | PNP | | 120 | −25 | −300 | 85 | 30* | 1 | 1T | | −5 | −10 | 2N525 | 2 |
| 2N567 | PNP | | 150 | −25 | −300 | 85 | 50* | 1 | 1.5T | | −5 | −10 | 2N43, 2N526 | 1, 2 |
| 2N568 | PNP | | 120 | −25 | −300 | 85 | 50* | 1 | 1.5T | | −5 | −10 | 2N526 | 2 |
| 2N569 | PNP | | 150 | −20 | −300 | 85 | 70* | 1 | 2T | | −5 | −10 | 2N241A, 2N1175 | 1, 2 |
| 2N570 | PNP | | 120 | −20 | −300 | 85 | 70* | 1 | 2T | | −5 | −10 | 2N527, 2N1415 | 1, 2 |
| 2N571 | PNP | | 150 | −10 | −300 | 85 | 100* | 1 | 3T | | −5 | −10 | 2N508 | 2 |
| 2N572 | PNP | | 120 | −10 | −300 | 85 | 100* | 1 | 3T | | −5 | −10 | 2N508 | 2 |
| 2N574 | PNP | | 25W @ 75°C | −60* | −15A | 95 | 10* | −10A | 6T Kc | | −7 ma | −60 | | |
| 2N574A | PNP | | 25W @ 75°C | −80* | −15A | 95 | 10* | −10A | 6T Kc | | −20 ma | −80 | | |
| 2N575 | PNP | | 25W @ 75°C | −60* | −15A | 95 | 19* | −10A | 5T Kc | | −7 ma | −60 | | |
| 2N575A | PNP | | 25W @ 75°C | −80* | −15A | 95 | 19* | −10A | 5T Kc | | −20 ma | −80 | | |
| 2N576 | NPN | | 200 | 20 | 400 | 100 | 80T* | 30 | 5T | | 20 | 20 | 2N635A | 2 |
| 2N576A | NPN | | 200 | 20 | 400 | 100 | 20* | 400 | 5T | | 40 | 40 | 2N635A | 2 |
| 2N578 | PNP | | 120 | −14 | −400 | 85 | 10* | 1 | 3 | | −5 | −12 | 2N394 | 2 |
| 2N579 | PNP | | 120 | −14 | −400 | 85 | 20* | 1 | 5 | | −5 | −12 | 2N396 | 2 |
| 2N580 | PNP | | 120 | −14 | −400 | 85 | 30* | 1 | 10 | | −5 | −12 | 2N397 | 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ °C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N581 | PNP | | 80 | −15 | −100 | 85 | 20* | −20 | 4 | | −6 | −6 | 2N394 | 2 |
| 2N582 | PNP | | 120 | −14 | −100 | 85 | 40* | −20 | 14 | | −5 | −12 | 2N397 | 2 |
| 2N583 | PNP | | 150 | −15 | −200 | 85 | 20* | −20 | 4 | | −6 | −6 | 2N394 | 2 |
| 2N584 | PNP | | 120 | −14 | −100 | 85 | 40* | −20 | 14 | | −5 | −12 | 2N397 | 2 |
| 2N585 | NPN | | 120 | 24 | 200 | 85 | 20* | 20 | 3 | | 8 | 12 | 2N634, 2N1302 | 2, 2 |
| 2N586 | PNP | | 250 | −45* | −250 | 85 | 35T* | −250 | | | −16 | −45 | 2N525, 2N1925 | 2, 2 |
| 2N587 | NPN | | 150 | 20 | 200 | | 20* | 200 | | | 50 | 40 | 2N634A | 2 |
| 2N588 | PNP | | 30 @ 45°C | −15 | −50 | 85 | | | | | 15 | −15 | 2N711A | 8 |
| 2N591 | PNP | | 50 | −32 | −20 | 100 | 70T | 2 | .7T | 41T | −6.5 | −10 | 2N324, 2N526 | 4, 2 |
| 2N592 | PNP | | 125 | −20 | | 85 | 20* | 1 | .4T | | −5 | −5 | 2N1414 | 2 |
| 2N593 | PNP | | 125 | −30 | | 85 | 30* | .5 | .6T | | −5 | −5 | 2N1414 | 2 |
| 2N594 | NPN | | 100 | 20 | | 85 | 20* | 1 | 1.5 | | 5 | 5 | | |
| 2N595 | NPN | | 100 | 15 | | 85 | 35* | 1 | 3 | | 5 | 5 | | |
| 2N596 | NPN | | 100 | 10 | | 85 | 50* | 1 | 5 | | 5 | 5 | 2N634 | 2 |
| 2N597 | PNP | | 250 | −40 | −400 | 100 | 40* | −100 | 3 | | −25 | −45 | 2N526, 2N527 | 2, 2 |
| 2N598 | PNP | | 250 | −20 | −400 | 100 | 50* | −100 | 5 | | −25 | −30 | | |
| 2N599 | PNP | | 250 | −20 | −400 | 100 | 100* | −100 | 12 | | 25 | −30 | 2N508 | 2 |
| 2N600 | PNP | | 750 | −20 | −400 | 100 | 50* | −100 | 5 | | −25 | −30 | | |
| 2N601 | PNP | | 0.75 | −20 | −400 | 100 | 2.5 | 3 | 12 | | 25 | −30 | | |
| 2N602 | PNP | | 120 | −20 | | 85 | 20* | .5 | | | −8 | −10 | 2N395, 2N711B | 2, 8 |
| 2N603 | PNP | | 120 | −20 | | 85 | 30* | .5 | | | −8 | −10 | 2N396, 2N711B | 2, 8 |
| 2N604 | PNP | | 120 | −20 | | 85 | 40* | .5 | | | −8 | −10 | 2N397, 2N711B | 2, 8 |
| 2N605 | PNP | | 120 | −15 | | 85 | 40T | −1 | | 20 | −10 | −12 | 2N394 | 2 |
| 2N606 | PNP | | 120 | −15 | | 85 | 60T | −1 | | 25 | −10 | −12 | 2N395 | 2 |
| 2N607 | PNP | | 120 | −15 | | 85 | 80T | −1 | | 30 | −10 | −12 | 2N396 | 2 |
| 2N608 | PNP | | 120 | −15 | | 85 | 120T | −1 | | 35 | −10 | −12 | 2N396 | 2 |
| 2N609 | PNP | | 180 | −20 | −200 | 85 | 90T* | 100 | | 30T | −25 | −20 | 2N321, 2N324 | 4, 4 |
| 2N610 | PNP | | 180 | −20 | −200 | 85 | 65T* | 100 | | 28T | −25 | −20 | 2N320, 2N323 | 4, 4 |
| 2N611 | PNP | | 180 | −20 | −200 | 85 | 45T* | 100 | | 26T | −25 | −20 | 2N320, 2N322 | 4, 4 |
| 2N612 | PNP | | 180 | −20 | −150 | 85 | .96αT | 1 | .6T | 37 | −25 | −20 | 2N319, 2N1098 | 4, 2 |
| 2N613 | PNP | | 180 | −20 | −200 | 85 | .97αT | 1 | .85T | 32 | −25 | −20 | 2N320, 2N1097 | 4, 2 |
| 2N614 | PNP | | 125 | −15 | −150 | 85 | 4.5T | .5 | 3T | 26T | −6 | −20 | 2N395 | 2 |
| 2N615 | PNP | | 125 | −15 | −150 | 85 | 7.5T | .5 | 5T | 34T | −6 | −20 | 2N395 | 2 |
| 2N616 | PNP | | 125 | −12 | −150 | 85 | 25T | .5 | 9T | 20T | −6 | −15 | 2N394 | 2 |
| 2N617 | PNP | | 125 | −12 | −150 | 85 | 15T | .5 | 7.5T | 30T | 6 | −15 | 2N394 | 2 |
| 2N618 | PNP | | 45W | −80* | −3A | 90 | 60* | −1A | 5 Kc | | −3 ma | −60 | | |
| 2N622 | NPN | | 400 | 50* | 50 | 160 | 25T* | .5 | .3 | 34T | .1 | 30 | | |
| 2N624 | PNP | | 100 | −20 | −10 | 100 | 20 | 2 | 12.5 | 20T | −30 | −30 | | |
| 2N625 | NPN | | 2.5W | 30 | | 100 | 30* | 50 | | | 100 | −40 | | |
| 2N631 | PNP | | 170 | −20 | −50 | 85 | 150T | 10 | 1.2T | 35T | −25 | −20 | 2N508 | 2 |
| 2N632 | PNP | | 150 | −24 | −50 | 85 | 100T | 10 | 1T | 25T | −25 | −20 | 2N324, 2N1175 | 4, 2 |
| 2N633 | PNP | | 150 | −30 | −50 | 85 | 60T | 10 | .8T | 25T | −25 | −20 | 2N323, 2N1415 | 4, 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVce BVcb* | Ic ma | Tj°C | ELECTRICAL PARAMETERS MIN. hfe-hfe* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ Vcb | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N634 | NPN | Sw | 150 | 20 | 300 | 85 | 15* | 200 | 5 | | 5 | 5 | 2N634A | 2 |
| 2N634A | NPN | Sw | 150 | 20 | 300 | 85 | 40* | 10 | 5 | | 6 | 25 | 2N634A | 2 |
| 2N635 | NPN | Sw | 150 | 20 | 300 | 85 | 25* | 200 | 10 | | 5 | 5 | 2N635A | 2 |
| 2N635A | NPN | Sw | 150 | 20 | 300 | 85 | 80* | 10 | 10 | | 6 | 25 | 2N635A | 2 |
| 2N636 | NPN | Sw | 150 | 20 | 300 | 85 | 35* | 200 | 15 | | 5 | 5 | 2N636A | 2 |
| 2N636A | NPN | Sw | 150 | 15 | 300 | 85 | 100* | 10 | 15 | | 6 | 25 | 2N636A | 2 |
| 2N637 | PNP | | 25W | −40 | −5A | 100 | 30* | −3A | | | 1 ma | −25 | | |
| 2N637A | PNP | | 25W | −70 | −5A | 100 | 30* | −3A | | | 5 ma | −60 | | |
| 2N637B | PNP | | 25W | −80 | −5A | 100 | 30* | −3A | | | 5 ma | −60 | | |
| 2N638 | PNP | | 25W | −40 | −5A | 100 | 20* | −3A | | | 1 ma | −25 | | |
| 2N638A | PNP | | 25W | −70 | −5A | 100 | 20* | −3A | | | 5 ma | −60 | | |
| 2N638B | PNP | | 25W | −80 | −5A | 100 | 20* | −3A | | | 5 ma | −60 | | |
| 2N639 | PNP | | 25W | −40 | −5A | 100 | 15* | −3A | | | 1 ma | −25 | | |
| 2N639A | PNP | | 25W | −70 | −5A | 100 | 15* | −3A | | | 5 ma | −60 | | |
| 2N639B | PNP | | 25W | −80 | −5A | 100 | 15* | −3A | | | 5 ma | −60 | | |
| 2N640 | PNP | | 80 | −34* | −10 | 85 | .984αT | −1 | 42T | 28T | −5 | −12 | 2N711B | 8 |
| 2N641 | PNP | | 80 | −34* | −10 | 85 | .984αT | −1 | 42T | 28T | −7 | −12 | 2N711B | 8 |
| 2N642 | PNP | | 80 | −34* | −10 | 85 | .984αT | −1 | 42T | 28T | −7 | −12 | 2N711B | 8 |
| 2N643 | PNP | | 120 | −29 | −100 | 85 | 20* | −5 | 20 | | −10 | −7 | | |
| 2N644 | PNP | | 120 | −29 | −100 | 85 | 20* | −5 | 40 | | −10 | −7 | | |
| 2N645 | PNP | | 120 | −29 | −100 | 85 | 20* | −5 | 60 | | −10 | −7 | | |
| 2N647 | NPN | | 100 | 25 | 50 | 85 | 70T* | −50 | | 54T | 14 | 25 | 2N388 | 2 |
| 2N649 | NPN | | 100 | 18 | 50 | 85 | 65T* | −50 | | 54T | 14 | 12 | 2N388 | 2 |
| 2N650 | PNP-A | | 200 | 45 | 250 | 100J | 40T | | 2.00 | 42 | 15 | | 2N1924 | 2 |
| 2N650A | PNP-A | | 200 | 45 | 500 | 100C | | | .75 | | 50 | | 2N1924 | 2 |
| 2N651 | PNP-A | | 200 | 45 | 250 | 100J | 75T | | 2.50 | 44 | 15 | | 2N1925 | 2 |
| 2N652 | PNP-A | | 200 | 45 | 250 | 100J | 160T | | 3.00 | 46 | 15 | | 2N1925 | 2 |
| 2N652A | PNP-A | | 200 | 45 | 500 | 100C | 160T | | 1.25 | | 50 | | 2N1926 | 2 |
| 2N653 | PNP-A | | 200 | 30 | 250 | 100J | 40T | | 2.00 | 42 | 15 | | 2N1926 | 2 |
| 2N654 | PNP-A | | 200 | 30 | 250 | 100J | 75T | | 2.50 | 44 | 15 | | 2N1414 | 2 |
| 2N655 | PNP-A | | 200 | 30 | 250 | 100J | 160T | | 3.50 | 46 | 15 | | 2N1175 | 2 |
| 2N656 | NPN | Si AF | 4W | 60 | 500 | 200 | 30* | 200 | | | 10 | 30 | 2N656, 2N508 | 2, 2 |
| 2N656A | NPN | Si AF | 5W | 60 | 500 | 200 | 30* | 200 | | | 10 | 30 | 2N656A | 2 |
| 2N657 | NPN | Si AF | 4W | 100 | 500 | 200 | 30* | 200 | | | 10 | 30 | 2N657 | 2 |
| 2N657A | NPN | Si AF | 5W | 100 | 500 | 200 | 30* | 200 | | | 10 | 30 | 2N657A | 2 |
| 2N658 | PNP | | 175 | −16 | −1A | 85 | 25* | −1 | 2.5 | | −6 | −12 | 2N394 | 2 |
| 2N659 | PNP | | 175 | −14 | −1A | 85 | 40* | −1 | 5.0 | | −25 | −25 | 2N396 | 2 |
| 2N660 | PNP | | 175 | −11 | −1A | 85 | 60* | −1 | 10 | | −25 | −25 | 2N397 | 2 |
| 2N661 | PNP | | 175 | −9 | −1A | 85 | 80* | −1 | 15 | | −25 | −25 | | |
| 2N662 | PNP | | 175 | −11 | −1A | 85 | 30* | −1 | 4 | | −25 | −25 | 2N396 | 2 |
| 2N665 | PNP | | 35W | −80* | 5A (Ie) | 95 | 40* | −.5A | 20 Kc | | −2 ma | −30 @ 71°C | | |
| 2N679 | NPN | | 150 | 20 | | 85 | 20* | 30 | 2 | | 25 | 25 | | |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N680 | NPN | | 150 | 20 | 50 | 85J | 35T | | | | 14 | | 2N1413 | 2 |
| 2N695 | PNP-M | | 75 | 15 | 50 | 100J | 40T | | 350 | | | | 2N705 | 8 |
| 2N696 | NPN-PL | Sw | 600 | 60* | | 175J | 20* | | | | 1.0 | 30 | 2N696 | 4 |
| 2N696A | NPN-PL | Sw | 800 | 60* | | 200J | 45T | | 150 | | .10 | | 2N2194A | 4 |
| 2N697 | NPN-PL | Sw | 600 | 60* | | 175J | 40* | | | | 1.0 | 30 | 2N697 | 4 |
| 2N697A | NPN-M | | 800 | 60* | | 200 | 70T | | 150 | | .10 | | 2N2193A | 4 |
| 2N698 | NPN-PL | Sw | 800 | 120* | | 200J | 40T* | | 70.0 | | .005 | 75 | 2N698 | 4 |
| 2N699 | NPN-PL | Sw | 600 | 120* | | 175J | 40* | | | | 2.0 | 60 | 2N699 | 4 |
| 2N699A | NPN-M | | 800 | 120* | | 200 | 70T | | 180 | | .10 | | 2N1893 | 4 |
| 2N699B | NPN-PL | | 870 | 120* | | 200J | 80T | | 120 | | .01 | | 2N1893 | 4 |
| 2N700 | PNP-M | | 75 | 25 | 50 | 100J | 10T | | 500 | 23 | | | 2N994 | 8 |
| 2N702 | NPN | | 600 | 25 | 50 | 175 | 20* | 10 | | | 0.5 | 10 | 2N706 | 8 |
| 2N703 | NPN | | 600 | 25 | 50 | 175 | 10* | 10 | | | 0.5 | 10 | 2N753 | 8 |
| 2N705 | PNP | Sw | 300 | 15* | 50 | 100 | 25* | | | | | | 2N705 | 8 |
| 2N705A | PNP-A | | 175 | 40 | 200 | 85J | 75T | | 2.00 | 44 | | | 2N705A | 8 |
| 2N706 | NPN-PEP | Sw | 300 | 25* | 200 | 175J | 20 | | | | 0.5 | | 2N706 | 8 |
| 2N706A | NPN-PEP | Sw | 300 | 25* | | 175J | 40T | | 750 | | 0.5 | | 2N706A | 8 |
| 2N706B | NPN-M | Sw | 300 | 25* | | 175J | 40T* | | 400 | | 10 | | 2N914 | 8 |
| 2N707 | NPN | | 1W | 28 | | | 9* | 10 | | | 3.5 | 15 | 2N915 | 8 |
| 2N707A | NPN-M | | 300 | 70 | 200 | 175 | 30T* | | 500 | | 5.0 | | 2N915 | 8 |
| 2N708 | NPN-PEP | Sw | 360 | 40 | | 200J | 50T* | | 500 | | .025 | | 2N708 | 8 |
| 2N710 | PNP-M | Sw | 300 | 15 | 50 | 100 | 25* | | | | | | 2N710 | 8 |
| 2N711 | PNP-M | Sw | 150 | 12 | 50 | 100J | 30T* | | 360 | 22 | 3.0 | | 2N711 | 8 |
| 2N711A | PNP-M | Sw | 150 | 15* | 100 | 100S | 25* | | | | 1.5 | 5 | 2N711A | 8 |
| 2N711B | PNP-M | Sw | 150 | 18* | 100 | 100S | 30* | | | | 1.5 | 10 | 2N711B | 8 |
| 2N715 | NPN-M | | 500 | 50 | | 175J | 30T* | | 150 | | .01 | | 2N915 | 8 |
| 2N716 | NPN-M | | 500 | 70 | | 175J | 30T* | | 150 | | 10 | | 2N915 | 8 |
| 2N717 | NPN-PL | Sw | 400 | 60 | | 175J | 40T* | | 150 | | 1.0 | | 2N717 | 8 |
| 2N718 | NPN-PL | Sw | 400 | 60 | | 175J | 75T* | | 150 | | 1.0 | | 2N718 | 8 |
| 2N718A | NPN-PL | Sw | 500 | 75 | | 200J | 70T* | | 160 | | .01 | | 2N718A | 8 |
| 2N719 | NPN-PL | Sw | 400 | 120 | | 175J | 30T* | | 180 | | 2.0 | | 2N719 | 8 |
| 2N719A | NPN-PL | Sw | 300 | 120 | | 200J | 30T* | | 100 | | .01 | | 2N719A | 8 |
| 2N720 | NPN-PL | Sw | 400 | 120 | | 175J | 65T* | | 180 | | 2.0 | | 2N720 | 8 |
| 2N721A | NPN-PL | Sw | 500 | 120 | | 200J | 65T* | | 110 | | .01 | | 2N720A | 8 |
| 2N725 | NPN-M | | 150 | 15 | 50 | | 20T* | | | | | | 2N725 | 8 |
| 2N728 | NPN-D | | 500 | 30 | | 175 | 40T* | | 150 | | 5.0 | | 2N706 | 8 |
| 2N729 | NPN-D | | 500 | 15 | 3.0 | 175 | 40T* | | 150 | | 5.0 | | 2N717 | 8 |
| 2N735 | NPN-D | | 1000 | 80 | 50 | 175 | 40T | | 40.0 | | 1.0 | | 2N759 | 8 |
| 2N736 | NPN-D | | 1000 | 80 | 50 | 175 | | | 50.0 | | 1.0 | | 2N760 | 8 |
| 2N741 | PNP-M | | 150 | 15 | 100 | 100J | 25T* | | 360 | 22 | | | 2N960 | 8 |
| 2N741A | PNP-M | | 150 | 20 | 100 | 100 | 25T* | | 360 | 22 | 3.0 | | 2N960 | 8 |
| 2N743 | NPN-EM | | 300 | 25 | 200 | 300S | 40T* | | | | | | 2N914 | 8 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | $BV_{CE}$ $BV_{CB}$* | Ic ma | $T_J$°C | ELECTRICAL PARAMETERS MIN. $h_{fe}$-$h_{FE}$* @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. $I_{CO}$ (μa) @ $V_{CB}$ | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N744 | NPN-EM | | 300 | 25 | 200 | 300S | 80T* | | | | 2N914 | 8 |
| 2N753 | NPN-PEP | Sw | 300 | 25 | | 175J | 80T | 750 | | | 2N753 | 8 |
| 2N754 | NPN-M | | 300 | 60 | 50 | 175J | 50T | 45.0 | | 1.0 | 2N915 | 8 |
| 2N758 | NPN-M | | 500 | 45 | 100 | 200A | 50T | 50.0 | | | 2N759 | 8 |
| 2N759 | NPN-PL | AF | 500 | 45 | 100 | 200A | 65T | 50.0 | | | 2N759 | 8 |
| 2N760 | NPN-PL | AF | 500 | 45 | 100 | 200A | 150T | 50.0 | | | 2N760 | 8 |
| 2N761 | NPN-M | | 500 | 45 | 100 | 200A | 35T* | 50.0 | | | 2N759 | 8 |
| 2N762 | NPN-M | | 500 | 45 | 100 | 200A | 70T* | 50.0 | | | 2N759 | 8 |
| 2N768 | PNP-MD | | 35 | 12 | 100 | 100 | 40T* | 175 | | 25 | 2N966 | 8 |
| 2N769 | PNP-M | | 35 | 12 | 100 | 100J | 55T* | 900 | | 3.0 | 2N961 | 8 |
| 2N779 | PNP-MD | | 60 | 15 | 50 | 100 | 90T* | 480 | | 25 | 2N964 | 8 |
| 2N779A | PNP-MD | | 60 | 15 | 100 | 100 | 60T* | 450 | | 3.0 | 2N994 | 8 |
| 2N780 | NPN-M | | 300 | 45 | | 175J | 20T | 30.0 | | | 2N760 | 8 |
| 2N781 | PNP-EM | | 150 | 15 | 200 | 100 | 25T | | | 3.0 | 2N781 | 8 |
| 2N782 | PNP-EM | | 150 | 12 | 200 | 100 | 20T | | | 3.0 | 2N782 | 8 |
| 2N783 | NPN-EM | | 300 | 40 | 200 | 175 | 40T | | | .25 | 2N914 | 8 |
| 2N784 | NPN-EM | | 300 | 30 | 200 | 175 | 25T | | | .25 | 2N914 | 8 |
| 2N796 | PNP-M | | 150 | 13 | 100 | 85A | 75T* | 80.0 | | 3.0 | 2N634A | 2 |
| 2N815 | NPN-FA | | 75 | 25 | 200 | | 80T* | 8.00 | 14 | 10 | 2N635A | 2 |
| 2N816 | NPN-FA | | 75 | 25 | 200 | 100J | 80T* | 8.00 | 14 | 10 | 2N635A | 2 |
| 2N818 | NPN-FA | | 75 | 30 | 400 | 85J | 25T | 2.50 | | 10 | 2N1302 | 2 |
| 2N819 | NPN-FA | | 75 | 30 | 400 | 85J | 30T | 5.00 | | 10 | 2N634A | 2 |
| 2N820 | NPN-FA | | 75 | 30 | 400 | 85J | 30T | 5.00 | | 10 | 2N634A | 2 |
| 2N821 | NPN-FA | | 75 | 30 | 400 | 85J | 70T* | 10.0 | | 10 | 2N635A | 2 |
| 2N822 | NPN | | 75 | 30 | 400 | 85J | 70T* | 10.0 | | 10 | 2N635A | 2 |
| 2N823 | NPN | | 75 | 25 | 400 | 85J | 40T | 12.0 | | 5.0 | 2N635A | 2 |
| 2N824 | NPN | | 75 | 25 | 400 | 85J | 40T | 12.0 | | 5.0 | 2N635A | 2 |
| 2N828 | PNP-D | | 150 | 15 | 200 | 150S | 40T* | 400 | | 3.0 | 2N828 | 8 |
| 2N834 | NPN-PEP | Sw | 300 | 40 | 200 | 175J | 40T* | 500 | | .50 | 2N834 | 8 |
| 2N835 | NPN-M | | 300 | 25 | 200 | 175 | 40T* | 450 | | .50 | 2N834 | 8 |
| 2N839 | NPN-M | | 300 | 45 | 50 | 175J | 35T | 30.0 | | 1.0 | 2N759 | 8 |
| 2N840 | NPN-M | | 300 | 45 | 50 | 175 | 70T | 30.0 | | 1.0 | 2N759 | 8 |
| 2N841 | NPN-M | | 300 | 45 | 50 | 175 | 140T | 40.0 | | 1.0 | 2N760 | 8 |
| 2N844 | NPN-M | | 300 | 60 | 50 | 175 | 80T* | 50.0 | 14 | 1.0 | 2N718A | 8 |
| 2N845 | NPN-M | | 300 | 100 | 50 | 175 | 80T* | 50.0 | 14 | 1.0 | 2N720A | 8 |
| 2N846 | PNP-MD | | 60 | 15 | 50 | 100S | 35T* | 450 | | 25 | 2N960 | 8 |
| 2N849 | NPN-M | | 450 | 25 | | 175J | 40T* | | | 10 | 2N706 | 8 |
| 2N850 | NPN-M | | 450 | 25 | | 175J | 80T* | | | 10 | 2N753 | 8 |
| 2N870 | NPN-PL | | 500 | 100 | | 200J | 70T* | 110 | | .01 | | |
| 2N871 | NPN | | 500 | 100 | | 200J | 120T* | 130 | | .01 | 2N871 | 8 |
| 2N909 | NPN-D | | 400 | 60 | | 175J | 55T | 160 | | 1.0 | 2N956 | 8 |
| 2N910 | NPN-PL | | 500 | 100 | | 200J | 100T | 60.0 | | .025 | | |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVce BVcb* | Ic ma | Tj°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ Vcb | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N911 | NPN-PL | | 500 | 100 | | 200J | 50T | | 50.0 | | .025 | | | |
| 2N912 | NPN-PL | | 500 | 100 | | 200J | 30T | | 40.0 | | .025 | | | |
| 2N914 | NPN-PEP | Sw | 360 | 40 | | 200J | 30T | | 400 | | .025 | | 2N914 | 8 |
| 2N915 | NPN-PL | AF | 360 | 70 | | 200J | 40T | | 400 | | .01 | | 2N915 | 8 |
| 2N916 | NPN-PL | AF | 360 | 45 | | 200J | 50T | | 500 | | .01 | | 2N916 | 8 |
| 2N929 | NPN-PL | | 300 | 45 | | 175J | 40 | | 30.0 | | .01 | | 2N915 | 8 |
| 2N930 | NPN-PL | | 300 | 45 | | 175J | 100 | | 30.0 | | .01 | | 2N915 | 8 |
| 2N956 | NPN-PL | | 500 | 75 | | 200J | 100T | | 200 | | .01 | | 2N956 | 8 |
| 2N960 | PNP | Sw | 150 | 15 | | 100 | 20T | | 460 | | | | 2N960 | 8 |
| 2N961 | PNP-EM | Sw | 150 | 12 | | 100 | 20T | | 460 | | | | 2N961 | 8 |
| 2N962 | PNP-EM | Sw | 150 | 12 | | 100 | 20T | | 460 | | | | 2N962 | 8 |
| 2N964 | PNP-EM | Sw | 150 | 15 | | 100 | 40T* | | 460 | | | | 2N964 | 8 |
| 2N965 | PNP-EM | Sw | 150 | 12 | | 100 | 40T* | | 460 | | | | 2N965 | 8 |
| 2N966 | PNP-EM | Sw | 150 | 12 | | 100 | 40T* | | 460 | | | | 2N966 | 8 |
| 2N968 | PNP | | 150 | 15 | | 100J | 20T* | | 320 | | 3.0 | | | |
| 2N969 | PNP | | 150 | 12 | | 100 | 20T* | | 320 | | | | 2N961 | 8 |
| 2N970 | PNP | | 150 | 12 | | 100 | 20T* | | 320 | | 3.0 | | 2N962 | 8 |
| 2N971 | PNP | | 150 | 7.0 | | 100 | 20T* | | 320 | | 10 | | 2N963 | 8 |
| 2N972 | PNP | | 150 | 15 | | 100 | 40T* | | 320 | | 3.0 | | 2N964 | 8 |
| 2N973 | PNP | | 150 | 12 | | 100 | 40T* | | 320 | | 3.0 | | 2N965 | 8 |
| 2N974 | PNP | | 150 | 12 | | 100 | 40T* | | 320 | | 3.0 | | 2N966 | 8 |
| 2N975 | PNP | | 150 | 7.0 | | 100 | 40T* | | 320 | | 10 | | | |
| 2N994 | PNP | Sw | 200 | 15 | 150 | 150S | 75* | | | | 3.0 | | 2N994 | 8 |
| 2N1000 | NPN-A | | 150 | 40 | | 100S | 35T* | | 7.00 | | 15 | | 2N634A | 2 |
| 2N1008 | PNP-A | | 167 | 20 | 300 | 75J | 90T | | 1.00 | | | | 2N1415 | 2 |
| 2N1008A | PNP | | 167 | 40 | 300 | 85J | 90T | | 1.00 | | | | 2N526 | 2 |
| 2N1008B | PNP | | 167 | 60 | 300 | 85J | 90T | | 1.00 | | | | 2N1925 | 2 |
| 2N1009 | PNP-A | | 150 | 25 | 20 | 85A | 40T | | .50 | | 800 | | 2N395 | 2 |
| 2N1010 | NPN | | 20 | 10 | 2 | 85 | 35T | −.3 | 2T | | 10 | 10 | 2N1694 | 2 |
| 2N1012 | NPN-A | | 150 | 40 | | 100S | 50T | | 3.00 | | 25 | | 2N635A | 2 |
| 2N1015 | NPN | | 150 @ 45°C | 30 | 75A | 150 | 10* | 2A | 20T Kc | | 20 ma | 30 | | |
| 2N1015A | NPN | | 150 @ 45°C | 60 | 75A | 150 | 10* | 2A | 20T Kc | | 20 ma | 60 | | |
| 2N1015B | NPN | | 150 @ 45°C | 100 | 7.5A | 150 | 10* | 2A | 20T Kc | | 20 ma | 100 | | |
| 2N1015C | NPN | | 150 @ 45°C | 150 | 7.5A | 150 | 10* | 2A | 20T Kc | | 20 ma | 150 | | |
| 2N1015D | NPN | | 150 @ 45°C | 200 | 7.5A | 150 | 10* | 2A | 20T Kc | | 20 ma | 200 | | |
| 2N1015E | NPN | | 150 @ 45°C | 250 | 7.5A | 150 | 10* | 2A | 20T Kc | | 20 ma | 250 | | |
| 2N1015F | NPN | | 150 @ 45°C | 300 | 7.5A | 150 | 10* | 2A | 20T Kc | | 20 ma | 300 | | |
| 2N1016 | NPN | | 150 @ 45°C | 30 | 7.5A | 150 | 10* | 5A | 20T Kc | | 20 ma | 30 | | |
| 2N1016A | NPN | | 150 @ 45°C | 60 | 7.5A | 150 | 10* | 5A | 20T Kc | | 20 ma | 60 | | |
| 2N1016B | NPN | | 150 @ 45°C | 100 | 7.5A | 150 | 10* | 5A | 20T Kc | | 20 ma | 100 | | |
| 2N1016C | NPN | | 150 @ 45°C | 150 | 7.5A | 150 | 10* | 5A | 20T Kc | | 20 ma | 150 | | |
| 2N1016D | NPN | | 150 @ 45°C | 200 | 7.5A | 150 | 10* | 5A | 20T Kc | | 20 ma | 200 | | |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N1016E | NPN | | 150 @ 45°C | 250 | 7.5A | 150 | 10* | 5A | 20T Kc | | 20 ma | 250 | | |
| 2N1016F | NPN | | 150 @ 45°C | 300 | 7.5A | 150 | 10* | 5A | 20T Kc | | 20 ma | 300 | | |
| 2N1017 | PNP | | 150 | −10 | −400 | 85 | 70* | 1 | 15 | | −25 | −30 | | |
| 2N1021 | PNP | | 50W | −100 | −5 | 95 | 70T* | −1A | | | −2 ma | −100 | | |
| 2N1022 | PNP | | 50W | −120 | −5 | 95 | 70T* | −1A | | | −2 ma | −120 | | |
| 2N1038 | PNP | | 20W | −40 | −3A | 95 | 35* | −1A | | | −125 | .5 | | |
| 2N1039 | PNP | | 20W | −60 | −3A | 95 | 35* | −1A | | | −125 | .5 | | |
| 2N1040 | PNP | | 20W | −80 | −3A | 95 | 35* | −1A | | | −125 | .5 | | |
| 2N1041 | PNP | | 20W | −100 | −3A | 95 | 35* | −1A | | | −125 | .5 | | |
| 2N1046 | PNP | | 15W | −8 | −3A | 65 | 70* | −0.5A | | | −1 ma | −40 | | |
| 2N1047 | NPN | | 40W @ 25°C | 80* | 500 | 200 | 12* | 500 | | | 15 | 30 | 7E1 | 12 |
| 2N1048 | NPN | | 40W @ 25°C | 120* | 500 | 200 | 12* | 500 | | | 15 | 30 | 7E3 | 12 |
| 2N1049 | NPN | | 40W @ 25°C | 80* | 500 | 200 | 30* | 500 | | | 15 | 30 | 7E2 | 12 |
| 2N1050 | NPN | | 40W @ 25°C | 120* | 500 | 200 | 30* | 500 | | | 15 | 30 | 2N2204 | 12 |
| 2N1056 | PNP | Obsolete | 240 | −50 | −300 | 100 | 18* | −20 | .5 | | −25 | −70 | 2N1614, 2N1924 | 1, 2 |
| 2N1057 | PNP | Sw | 240 | −45 | −300 | 100 | 34* | −20 | .5 | | −16 | −45 | 2N1057, 2N1924 | 1, 2 |
| 2N1058 | NPN | | 50 | 20 | 50 | 75 | 10 | 1 | 4 | 22.5 | 50 | 18 | 2N292 | 3 |
| 2N1059 | NPN | | 180 | 15 | 100 | 75 | 50* | 35 | 10 Kc | 25 | 50 | 40 | 2N635A | 2 |
| 2N1067 | NPN | | 5W | 30 | .5A | 175 | 15* | 200 | .75 | | 500 | 60 | | |
| 2N1068 | NPN | | 10W | 30 | 1.5A | 175 | 15* | 750 | .75 | | 500 | 60 | | |
| 2N1069 | NPN | | 50W | 45 | 4A | 175 | 10* | 1.5A | .5 | | 1 ma | 60 | | |
| 2N1070 | NPN | | 50W | 45 | 4A | 175 | 10* | 1.5A | .5 | | 1 ma | 60 | | |
| 2N1086 | NPN | Osc | 65 | 9 | 20 | 85 | 17* | 1 | 8T | 24T | 3 | 5 | 2N1086 | 3 |
| 2N1086A | NPN | Osc | 65 | 9 | 20 | 85 | 17* | 1 | 8T | 24T | 3 | 5 | 2N1086A | 3 |
| 2N1087 | NPN | Osc | 65 | 9 | 20 | 85 | 17* | 1 | 8T | 26T | 3 | 5 | 2N1087 | 3 |
| 2N1090 | NPN | | 120 | 15 | 400 | 85 | 50* | 20 | 5 | | 8 | 12 | 2N635A | 2 |
| 2N1091 | NPN | | 120 | 12 | 400 | 85 | 40* | 20 | 10 | | 8 | 12 | 2N635A | 2 |
| 2N1092 | NPN | | 2W | 30 | 500 | 175 | 15* | 200 | .75 | | 500 | 60 | | |
| 2N1093 | PNP-A | | 150 | 30 | 250 | 85J | 125T | | 8.00 | | 6.0 | | 2N1307 | 2 |
| 2N1097 | PNP | AF Out | 140 | −16 | −100 | 85 | 55T | 1 | | | −16 | −16 | 2N1097 | 2 |
| 2N1098 | PNP | AF Out | 140 | −16 | −100 | 85 | 45T | 1 | | | −16 | −16 | 2N1098 | 2 |
| 2N1099 | PNP | | 30W | 80* | | 95 | 35* | 5A | 10 Kc | | 8 ma | −80 | | |
| 2N1100 | PNP | | 30W | 100* | | 95 | 25* | 5A | 10 Kc | | 8 ma | −100 | | |
| 2N1101 | NPN | | 180 | 15 | 100 | 75 | 25* | 35 | 10 Kc | | 50 | 20 | 2N635A | 2 |
| 2N1102 | NPN | | 180 | 25 | 100 | 75 | 25* | 35 | 10 Kc | | 50 | 40 | 2N635A | 2 |
| 2N1107 | PNP | | 30 | 16* | 5 | 85 | 33 | −0.5 | 40 | | −10 | −12 | | |
| 2N1108 | PNP | | 30 | 16* | 5 | 85 | 30 | −0.5 | 35 | | −10 | −12 | | |
| 2N1109 | PNP | | 30 | 16* | 5 | 85 | 15 | −0.5 | 35 | | −10 | −12 | | |
| 2N1110 | PNP | | 30 | 16* | 5 | 85 | 26 | −0.5 | 35 | | −10 | −12 | | |
| 2N1111 | PNP | | 30 | 20* | 5 | 85 | 22 | −0.5 | 35 | | −10 | −12 | | |
| 2N1114 | NPN-A | | 150 | 25 | 200 | 100J | 110T* | | 10.0 | | 30 | | 2N635A | 2 |
| 2N1115 | PNP | Sw | 150 | −20 | −125 | 85 | 35 | −60 | 5 | | −6 | −20 | 2N1115, 2N396A | 7, 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N1115A | PNP | Sw | 150 | −35 | −125 | 85 | 35 | −60 | 5 | | −6 | −20 | 2N1115A, 2N656A | 7, 2 |
| 2N1116 | NPN-GD | | 5000 | 60 | | 175A | 70T* | | 4.00 | | | | 2N656A | 2 |
| 2N1117 | NPN-GD | | 5000 | 60 | | 175A | 70T* | | 4.00 | | | | 2N656A | 2 |
| 2N1118 | PNP | | 150 | −25 | −50 | 140 | 9 | | | | 1.0 | −25 | | |
| 2N1118A | PNP | | 150 | −25 | −50 | 140 | 15 | 1 | | | 0.1 | −10 | | |
| 2N1119 | PNP | | 150 | −10 | −50 | 140 | 6* | −15 | | | 0.1 | −10 | | |
| 2N1121 | NPN | IF | 65 | 15 | 20 | 85 | 34* | 1 | 8 Kc | | 5 | 15 | 2N1121 | 3 |
| 2N1122 | PNP | | −25 @ 45°C | −10 | −50 | 85 | 35 | 1.0 | | | 5 | −5 | 2N994 | 8 |
| 2N1122A | PNP | | −25 @ 45°C | | −50 | 85 | 35 | 1.0 | | | 5 | −5 | 2N994 | 8 |
| 2N1123 | PNP | | 750 | −40 | −400 | 100 | 40* | −100 | 3 | | −25 | −45 | | |
| 2N1128 | PNP-A | | 150 | 25 | 250 | 85J | 120T | | 1.25 | | 20 | | 2N324 | 4 |
| 2N1129 | PNP-A | | 150 | 25 | 250 | 85J | 165T* | | .75 | | 25 | | 2N508 | 2 |
| 2N1130 | PNP-A | | 150 | 30 | 250 | 85J | 110T* | | .75 | | 25 | | 2N1926 | 2 |
| 2N1141 | PNP | | 750 | | 100 | 100 | 12 | −10 | 750T | | −5 | −15 | | |
| 2N1142 | PNP | | 750 | | 100 | 100 | 10 | −10 | 600T | | −5 | −15 | | |
| 2N1143 | PNP | | 750 | | 100 | 100 | 8 | −10 | 480T | | −5 | −15 | | |
| 2N1144 | PNP | AF Out | 140 | −16 | −100 | 85 | 55T | 1 | | | −16 | −16 | 2N1144, 2N1097 | 2, 2 |
| 2N1145 | PNP | AF Out | 140 | −16 | −100 | 85 | 45T | 1 | | | −16 | −16 | 2N1145, 2N1098 | 2, 2 |
| 2N1149 | NPN | | 150 | 45* | 25 | 175 | −0.9 | −1 | 4T | 35T | 2 | 30 | 2N1276 | 4 |
| 2N1150 | NPN | | 150 | 45* | 25 | 175 | −0.948 | −1 | 5T | 39T | 2 | 30 | 2N1277 | 4 |
| 2N1151 | NPN | | 150 | 45* | 25 | 175 | −0.948 | −1 | 8T | 39T | 2 | 30 | 2N1278 | 4 |
| 2N1152 | NPN | | 150 | 45* | 25 | 175 | −0.9735 | −1 | 6T | 42T | 2 | 30 | 2N1278 | 4 |
| 2N1153 | NPN | | 150 | 45* | 25 | 175 | −0.987 | −1 | 7T | 42.5T | 2 | 30 | 2N1279 | 4 |
| 2N1154 | NPN | | 750 | 50* | 60 | 150 | −0.9 | −5 | | 30 | 5 | 50 | 2N333 | 4 |
| 2N1155 | NPN | | 750 | 80* | 50 | 150 | −0.9 | −5 | | 30 | 6 | 80 | 2N333 | 4 |
| 2N1156 | NPN | | 750 | 120* | 40 | 150 | −0.9 | −5 | | 30 | 8 | 120 | | |
| 2N1157 | PNP | | | −60* | | 95 | 38* | −10A | | | −7.0 ma | −60 | | |
| 2N1157A | PNP | | | −80* | | 95 | 38* | −10A | | | −20 ma | −80 | | |
| 2N1159 | PNP | | 20W @ 71°C | 80* | −65 | −65 | 30* | 3A | 10T Kc | | 8 ma | −80 | | |
| 2N1160 | PNP | | 20W @ 71°C | 80* | | −65 | 20* | 5A | 10T Kc | | 8 ma | −80 | | |
| 2N1168 | PNP | | 45W | −50* | 5A (IE) | 95 | 110T | 1A | 10T Kc | 37T | −8 ma | −50 | | |
| 2N1171 | PNP | | | −12 | 400 | 85 | 30* | 1 | 10 | | 5 | −12 | 2N397 | 2 |
| 2N1172 | PNP | | | 40* | | −65 | 30 | 100 | | 34T | 0.2 ma | −40 | | |
| 2N1175 | PNP-A | | 200 | 35 | 200 | 85J | 90T* | | 4.20 | | 12 | | 2N1175 | 2 |
| 2N1175A | PNP-A | | 200 | 35 | 200 | 85J | 90T* | | 4.20 | | 12 | | 2N1175A | 2 |
| 2N1177 | PNP | | 80 | −30* | −10 | 71 | 100 | | 140 | | −12 | −12 | | |
| 2N1178 | PNP | | 80 | −30* | −10 | 71 | 40 | | 140 | | −12 | −12 | | |
| 2N1179 | PNP | | 80 | −30* | −10 | 71 | 80 | | 140 | | −12 | −12 | | |
| 2N1180 | PNP | | 80 | −30* | −10 | 71 | 80 | | 100 | | −12 | −12 | | |
| 2N1183 | PNP | | 1W | −20 | −3.0 | 100 | 20* | −400 | 500 Kc | −250 | −250 | −45 | | |
| 2N1183A | PNP | | 1W | −30 | −3.0 | 100 | 20* | −400 | 500 Kc | | −250 | −80 | | |
| 2N1183B | PNP | | 1W | −40 | −3.0 | 100 | 20* | −400 | 500 Kc | | −250 | −80 | | |

| JEDEC No. | Type | Use | MAXIMUM RATINGS | | | | ELECTRICAL PARAMETERS | | | | | | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Pc mw @ 25°C | BVce BVcb* | Ic ma | Tj°C | MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ Vcb | | |
| 2N1184 | PNP | | 1W | −20 | −3.0 | 100 | 40* | −400 | 500 Kc | | −250 | −45 | | |
| 2N1184A | PNP | | 1W | −30 | −3.0 | 100 | 40* | −400 | 500 Kc | | −250 | −80 | | |
| 2N1184B | PNP | | 1W | −40 | −3.0 | 100 | 40* | −400 | 500 Kc | | −250 | −80 | | |
| 2N1186 | PNP | | 200 | 60 | | 100J | 50T | | 1.50 | | | | 2N1924 | 2 |
| 2N1187 | PNP | | 200 | 60 | | 100J | 85T | | 2.00 | | | | 2N1926 | 2 |
| 2N1188 | PNP | | 200 | 60 | | 100J | 155T | | 2.50 | | | | 2N1926 | 2 |
| 2N1191 | PNP-A | | 175 | 40 | 200 | 85J | 40T | | 1.50 | 42 | | | 2N1414 | 2 |
| 2N1192 | PNP-A | | 175 | 40 | 200 | 85J | 75T | | 2.00 | 44 | | | 2N1175 | 2 |
| 2N1193 | PNP-A | | 175 | 40 | 200 | 85J | 160T | | 2.50 | 46 | | | 2N508 | 2 |
| 2N1198 | NPN | Sw | 65 | 25 | 75 | 85 | 17* | 8 | 5 | | 1.5 | 15 | 2N1198, 2N167 | 3, 3 |
| 2N1199 | NPN | | 100 | 20 | 100 | 150 | 12* | 20 | | | 0.7 | −10 | | |
| 2N1202 | PNP | | | −60 | | 95 | 40* | −0.5A | | | −2.0 ma | −80 | | |
| 2N1203 | PNP | | | −70 | | 95 | 25* | −2A | | | −2.0 ma | −120 | | |
| 2N1213 | PNP | | 75 | −25 | −100 | 71 | | | | | −5 | −12 | | |
| 2N1214 | PNP | | 75 | −25 | −100 | 71 | | | | | −5 | −12 | | |
| 2N1215 | PNP | | 75 | −25 | −100 | 71 | | | | | −5 | −12 | | |
| 2N1216 | PNP | | 75 | −25 | −100 | 71 | | | | | −5 | −12 | | |
| 2N1217 | NPN | | 75 | 20 | 25 | | 40* | .5 | 6.0 | | 29 | 15 | 2N1217 | 3 |
| 2N1224 | PNP | | 120 | −40 | −10 | 100 | 20 | −1.5 | 30 | 15 | −12 | −12 | | |
| 2N1225 | PNP | | 120 | −40 | −10 | 100 | 20 | −1.5 | 100 | 15 | −12 | −12 | | |
| 2N1226 | PNP | | 120 | −60 | −10 | 100 | 20 | −1.5 | 30 | 15 | −12 | −12 | | |
| 2N1228 | PNP | | 400 | −15 | | 160 | 14 | | 1.2T | | −0.1 | −12 | | |
| 2N1229 | PNP | | 400 | −15 | | 160 | 28 | | 1.2T | | −0.1 | −12 | | |
| 2N1230 | PNP | | 400 | −35 | | 160 | 14 | | 1.2T | | −0.1 | −30 | | |
| 2N1231 | PNP | | 400 | −35 | | 160 | 28 | | 1.2T | | −0.1 | −30 | | |
| 2N1232 | PNP | | 400 | −60 | | 160 | 14 | | 1.0T | | −0.1 | −50 | | |
| 2N1233 | PNP | | 400 | −60 | | 160 | 28 | | 1.0T | | −0.1 | −50 | | |
| 2N1234 | PNP | | 400 | −110 | | 160 | 14 | | 8T | | −0.1 | −90 | | |
| 2N1238 | PNP | | 1W free air | −15 | | 160 | 14 | | 1.2T | | −0.1 | −12 | | |
| 2N1239 | PNP | | 1W free air | −15 | | 160 | 28 | | 1.2T | | −0.1 | −12 | | |
| 2N1240 | PNP | | 1W free air | −35 | | 160 | 14 | | 1.2T | | −0.1 | −30 | | |
| 2N1241 | PNP | | 1W free air | −35 | | 160 | 28 | | 1.2T | | −0.1 | −30 | | |
| 2N1242 | PNP | | 1W free air | −60 | | 160 | 14 | | 1.0T | | −0.1 | −50 | | |
| 2N1243 | PNP | | 1W free air | −60 | | 160 | 28 | | 1.0T | | −0.1 | −50 | | |
| 2N1244 | PNP | | 1W free air | −110 | | 160 | 14 | | .8T | | −0.1 | −90 | | |
| 2N1247 | NPN | | 200 | 6.0 | | 175A | 25T | | 5.00 | | | | | |
| 2N1248 | NPN | | 200 | 6.0 | | 175A | 20T | | 5.00 | | | | | |
| 2N1251 | NPN | | 150 | 15 | 100 | 85 | 70 | | 7.5 | | 50 | 20 | 2N635A | 2 |
| 2N1252 | NPN | | 2W | 20 | | 175 | 15* | 150 | | | 10 | 20 | | |
| 2N1253 | NPN | | 2W | 20 | | 175 | 40* | 150 | | | 10 | 20 | | |
| 2N1261 | PNP | | | −45 | | 95 | 20* | | | | | | | |
| 2N1262 | PNP | | | −45 | | 95 | 30* | | | | −2.0 | −60 | | |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N1263 | PNP | | | −45 | | 95 | 45* | | | | −20 | −60 | | |
| 2N1264 | PNP | | 50 | −20* | 50 | 75 | 15 | 1.5 | | | 50 | −20 | | |
| 2N1265 | PNP | | 50 | −10* | 100 | 85 | 25 | 1 | 600 | | 100 | | 2N1097 | 2 |
| 2N1266 | PNP | | 80 | −10* | | 85 | 10 | 1 | | | 100 | −10 | 2N1098 | 2 |
| 2N1273 | PNP-A | | 150 | 15 | 150 | 85J | 50T | | 2.00 | | | | 2N1097 | 2 |
| 2N1274 | PNP-A | | 150 | 25 | 150 | 85J | 50T | | 2.00 | | | | 2N1414 | 2 |
| 2N1276 | NPN | Si AF | 150 | 30 | 25 | 150 | 10T | 10 | 15 | 37T | 1 | 30 | 2N1276 | 4 |
| 2N1277 | NPN | Si AF | 150 | 30 | 25 | 150 | 20T | 10 | 15 | 39T | 1 | 30 | 2N1277 | 4 |
| 2N1278 | NPN | Si AF | 150 | 30 | 25 | 150 | 33T | 10 | 15 | 44T | 1 | 30 | 2N1278 | 4 |
| 2N1279 | NPN | Si AF | 150 | 30 | 25 | 150 | 80T | 10 | 15 | 45T | 1 | 30 | 2N1279 | 4 |
| 2N1280 | PNP | | 200 | 16 | 400 | 85 | 40 | −20 | 5 | | −10 | −10 | 2N396 | 2 |
| 2N1281 | PNP | | 200 | 12 | 400 | 85 | 60 | −20 | 7 | | −10 | −10 | 2N396 | 2 |
| 2N1282 | PNP | | 200 | 6 | 400 | 85 | 70 | −20 | 10 | | −10 | −10 | 2N397 | 2 |
| 2N1284 | PNP | | 150 | 15 | 400 | 85 | 30 | −10 | 5 | | −6 | −20 | 2N396 | 2 |
| 2N1287 | PNP | | 165 | 20* | 300 | 85 | 40 | | 1.00 | | 10 | | 2N526 | 2 |
| 2N1287A | PNP | | 165 | 20* | 300 | 85 | 40 | | 1.00 | | 10 | | 2N527 | 2 |
| 2N1288 | NPN | Obsolete | 75 | 5 | 50 | 85 | 50* | 10 | 40 | | 5 | 5 | | |
| 2N1289 | NPN | Obsolete | 75 | .15 | 50 | 85 | 50* | 10 | 40 | | 5 | 15 | | |
| 2N1291 | PNP | | 20W | 30 | 3 | 85 | 40* | 0.5 | | | 5 | −2 | | |
| 2N1293 | PNP | | 20W | 60 | 3 | 85 | 40* | 0.5 | | | 5 | −2 | | |
| 2N1295 | NPN | | 20W | 80 | 3 | 85 | 40* | 0.5 | | | 5 | −2 | | |
| 2N1297 | PNP | | 20W | 100 | 3 | 85 | 40* | 0.5 | | | 5 | −2 | | |
| 2N1299 | NPN | | 150 | 20 | 200 | 100 | 35* | 50 | 4.0 | | 100 | 40 | 2N377, 2N634A | 2, 2 |
| 2N1300 | PNP | | 150 | −12 | −100 | 85 | 50 | −10 | | | −3 | | 2N711B | 8 |
| 2N1301 | PNP | | 150 | −12 | −100 | 85 | 50 | −10 | | | −3 | | 2N711B | 8 |
| 2N1302 | NPN | | 150 | 25* | 300 | 100 | 50 | | 3.00 | | 6.0 | | 2N1302 | 2 |
| 2N1303 | NPN | | 150 | 30* | 300 | 100 | 50 | | 3.00 | | 6.0 | | 2N1303 | 2 |
| 2N1304 | NPN | Sw | 300 | 20 | 300 | 100 | 40* | 10 | 5 | | 6 | 25 | 2N1304 | 2 |
| 2N1305 | NPN | | 150 | 30* | 300 | 100 | 70 | | 5.00 | | 6.0 | | 2N1305 | 2 |
| 2N1306 | NPN | Sw | 300 | 15 | 300 | 100 | 60* | 10 | 10 | | 6 | 25 | 2N1306 | 2 |
| 2N1307 | NPN | | 150 | 30* | 300 | 100 | 100 | | 10.0 | | 6.0 | | 2N1307 | 2 |
| 2N1308 | NPN | Sw | 300 | 15 | 300 | 100 | 80* | 10 | 15 | | 6 | 25 | 2N1308 | 2 |
| 2N1309 | NPN | | 150 | 30* | 300 | 100 | 150 | | 15.0 | | 6.0 | | 2N1309 | 2 |
| 2N1310 | NPN | | 120 | 90 | | | 20* | 5 | 1.5T | | 7 | 5 | 2N1510 | 3 |
| 2N1313 | PNP | | 180 | −15 | 400 | 100 | 40* | | 6 | | 2.5 | −0.5 | 2N396 | 2 |
| 2N1316 | PNP | | 200 | 15 | 400 | 85 | 50* | | 10 | | −5 | −12 | 2N397 | 2 |
| 2N1317 | PNP | | 200 | 12 | 400 | 85 | 45* | | 10 | | −6 | −12 | 2N397 | 2 |
| 2N1318 | PNP | | 200 | 6 | 400 | 85 | 40* | | 10 | | −7 | −10 | 2N397 | 2 |
| 2N1343 | PNP | | 150 | 16 | 400 | 85 | 15* | −50 | 4 | | −6 | −15 | 2N395 | 2 |
| 2N1344 | PNP | | 150 | 10 | 400 | 85 | 60* | −20 | 7 | | 10 | −15 | 2N397, 2N396 | 2, 2 |
| 2N1345 | PNP | | 150 | 8 | 400 | 85 | 30* | −400 | 10 | | −6 | −12 | 2N397 | 2 |
| 2N1346 | PNP | | 150 | 10 | 400 | 85 | 40* | −14 | 10 | | −5 | −5 | 2N397 | 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCB BVCB* | Ic ma | TJ °C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N1347 | PNP | | 150 | 12 | 200 | 85 | 30* | 10 | 5 | | −6 | −12 | 2N396 | 2 |
| 2N1348 | PNP | | 200 | 40* | 400 | 85 | 95* | | 5.0 | | 10 | | 2N1305 | 2 |
| 2N1352 | PNP | | 150 | 20 | 200 | 85 | 40* | | 2.5T | | −5 | −30 | 2N526, 2N1925 | 2, 2 |
| 2N1353 | PNP | | 200 | 10 | 200 | 85 | 25* | 10 | 1.5 | | 6 | 10 | 2N394, 2N397 | 2, 2 |
| 2N1354 | PNP | | 200 | 15 | 200 | 85 | 25* | 10 | 3 | | 6 | 15 | 2N395 | 2 |
| 2N1355 | PNP | | 200 | 20 | 200 | 85 | 30* | 10 | 5 | | 6 | 20 | 2N396 | 2 |
| 2N1356 | PNP | | 200 | 30* | 200 | 85 | 80* | | 8.0 | | 6.0 | | 2N397 | 2 |
| 2N1357 | PNP | | 200 | 15 | 200 | 85 | 40* | 10 | 10 | | 6 | 15 | 2N397 | 2 |
| 2N1358 | PNP | | | 80* | | 95 | 40* | 1.2 | 100 | | | | | |
| 2N1366 | Alloy | Sw | 150 | 20* | | | 70* | | 10.0 | | | | 2N397 | 2 |
| 2N1367 | Alloy | Sw | 150 | 20* | | | 70* | | 10.0 | | | | 2N1307 | 2 |
| 2N1370 | PNP | | 150 | 25* | 150 | 100 | 80* | | 2.0 | | | | 2N1415 | 2 |
| 2N1371 | PNP | | 150 | 45* | 150 | 100 | 80 | | 2.0 | | | | 2N1415 | 2 |
| 2N1372 | PNP | | 210 | 25* | 200 | 100 | 45 | | 2.0 | | | | 2N1415 | 2 |
| 2N1373 | PNP | | 250 | 45* | 200 | 100 | 45 | | 2.0 | | | | 2N1924 | 2 |
| 2N1374 | PNP | | 250 | 25* | 200 | 100 | 70 | | 2.0 | | | | 2N1415 | 2 |
| 2N1375 | PNP | | 250 | 45* | 200 | 100 | 70 | | 2.0 | | | | 2N1925 | 2 |
| 2N1376 | PNP | | 250 | 25* | 200 | 100 | 95 | | 2.0 | | | | 2N1175 | 2 |
| 2N1377 | PNP | | 250 | 45* | 200 | 100 | 95 | | 2.0 | | | | 2N1926 | 2 |
| 2N1378 | PNP | | 250 | 12* | 200 | 100 | 200 | | 2.0 | | | | 2N508 | 2 |
| 2N1379 | PNP | | 250 | 25* | 200 | 100 | 200 | | 2.0 | | | | 2N1175 | 2 |
| 2N1380 | PNP | | 250 | 12* | 200 | 100 | 100 | | 2.0 | | | | 2N1097 | 2 |
| 2N1381 | PNP | | 250 | 25* | 200 | 100 | 100 | | 2.0 | | | | 2N1414 | 2 |
| 2N1382 | PNP | | 200 | 25* | 200 | 85 | 80 | | 2.0 | | | | 2N1415 | 2 |
| 2N1383 | PNP | | 200 | 25* | 200 | 85 | 50 | | 2.0 | | | | 2N1414 | 2 |
| 2N1389 | NPN | | 250 | 50* | 50 | 175 | | | 25 | 15 | | | 2N696 | 4 |
| 2N1404 | PNP | | 150 | 25* | 300 | 85 | 100* | | 4.00 | | 5.0 | | 2N404 | 2 |
| 2N1408 | PNP | | 150 | 50* | | 100 | 25 | | | | | | 2N1924 | 2 |
| 2N1411 | PNP | | 25 @ 45°C | −5 | −50 | 85 | 20* | −50 | | | 5 | −5 | 2N962 | 8 |
| 2N1413 | PNP | AF Sw | 200 | −25 | −200 | 85 | 25* | −20 | 0.8 | | −12 | −30 | 2N1413 | 2 |
| 2N1414 | PNP | AF Sw | 200 | −25 | −200 | 85 | 34* | −20 | 1.0 | | −12 | −30 | 2N1414 | 2 |
| 2N1415 | PNP | AF Sw | 200 | −25 | −200 | 85 | 53* | −20 | 1.3 | | −12 | −30 | 2N1415 | 2 |
| 2N1420 | NPN-M | | 600 | 60* | | 175 | 140* | | 250 | | | | 2N1711 | 4 |
| 2N1420A | NPN-PL | | 800 | 60* | | 200 | 120* | | 200 | | | | 2N1711 | 4 |
| 2N1427 | PNP | | 25 @ 45°C | −6 | −50 | 85 | 20* | −50 | | | 5 | −6 | 2N782 | 8 |
| 2N1428 | PNP | | 100 | −6 | −50 | 140 | 12* | −5 | | | 0.1 | −6 | | |
| 2N1429 | PNP | | 100 | −6 | −50 | 140 | 12* | −5 | | | 0.1 | −6 | | |
| 2N1431 | NPN | | 180 | 15 | 100 | 75 | 75* | 35 | | | 50 | 20 | 2N635A | 2 |
| 2N1432 | PNP | | 100 | −45 | 10 | 100 | 30 | 2 | | | 15 | −45 | | |
| 2N1433 | PNP | | | −50 | 3.5 | 95 | 20* | 2 | 5 | | 0.1 | −2 | | |
| 2N1434 | PNP | | | −50 | 3.5 | 95 | 45* | 2 | 5 | | 0.1 | −2 | | |
| 2N1435 | PNP | | | −50 | 3.5 | 95 | 30* | 2 | 5 | | 0.1 | −2 | | |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVce BVcb* | Ic ma | Tj°C | ELECTRICAL PARAMETERS MIN. hfe-hfe* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ Vcb | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N1436 | PNP | | 50 | −15* | −50 | 100 | 20* | −10 | | | | | | |
| 2N1446 | PNP | | 200 | 25 | 400 | 85 | 16* | 20 | .8 | | 10 | 30 | 2N524 | 2 |
| 2N1447 | PNP | | 200 | 25 | 400 | 85 | 35* | 20 | 1.5 | | 10 | 30 | 2N525 | 2 |
| 2N1448 | PNP | | 200 | 25 | 400 | 85 | 50* | 20 | 2 | | 10 | 30 | 2N526 | 2 |
| 2N1449 | PNP | | 200 | 25 | 400 | 85 | 70* | 20 | 2.5 | | 10 | 30 | 2N527 | 2 |
| 2N1450 | PNP | | 120 | 30* | 100 | 85 | 20* | 10 | | | 10 | 7 | | |
| 2N1451 | PNP | | 200 | 45* | 400 | 85 | 45* | | 1.50 | | 15 | | 2N1413 | 2 |
| 2N1452 | PNP | | 200 | 45* | 400 | 85 | 60* | | 2.20 | | 15 | | 2N1414 | 2 |
| 2N1471 | PNP | | 200 | 12* | 200 | 85 | 160* | | 5.0 | | 5.0 | | 2N508 | 2 |
| 2N1472 | NPN | | 100 | 25 | 100 | 150 | 20 | 10 | | | 0.5 | 10 | | |
| 2N1473 | NPN | | | 20 | 400 | 75 | 25* | 400 | 4 | | 100 | 40 | 2N635A | 2 |
| 2N1478 | PNP | | 250 | −30* | −400 | 100 | 40* | −100 | 3 | | 5 | 1.5 | 2N396, 2N1415 | 2, 2 |
| 2N1479 | NPN | | 4W | 60* | 1.5 | 175 | 15* | 200 | 1.5 | 60 | 10 | 30 | 2N497A | 8 |
| 2N1480 | NPN | | 4W | 100* | 1.5 | 175 | 15* | 200 | 1.5 | 100 | 10 | 30 | 2N497A | 8 |
| 2N1481 | NPN | | 4W | 60* | 1.5 | 175 | 35* | 200 | 1.5 | 60 | 10 | 30 | 2N656A | 8 |
| 2N1482 | NPN | | 4W | 100* | 1.5 | 175 | 35* | 200 | 1.5 | 100 | 10 | 30 | 2N656A | 8 |
| 2N1483 | NPN | | 15W | 60* | 3 | 175 | 15* | 750 | 1.25 | | 15 | 30 | | |
| 2N1484 | NPN | | 15W | 100* | 3 | 175 | 15* | 750 | 1.25 | | 15 | 30 | | |
| 2N1485 | NPN | | 15W | 60* | 3 | 175 | 35* | 750 | 1.25 | | 15 | 30 | | |
| 2N1486 | NPN | | 15W | 100* | 3 | 175 | 35* | 750 | 1.25 | | 15 | 30 | | |
| 2N1487 | NPN | | 60W | 60* | 6 | 175 | 10* | 1.5 | 1 | | 25 | 30 | | |
| 2N1488 | NPN | | 60W | 100* | 6 | 175 | 10* | 1.5 | 1 | | 25 | 30 | | |
| 2N1489 | NPN | | 60W | 60* | 6 | 175 | 25* | 1.5 | 1 | | 25 | 30 | | |
| 2N1490 | NPN | | 60W | 100* | 6 | 175 | 25* | 1.5 | 1 | | 25 | 30 | | |
| 2N1499 | PNP | | 25 | −25* | −50 | 85 | 20* | −10 | | | 5 | −5 | 2N711A | 8 |
| 2N1499A | PNP | | 60 | 20* | 50 | 100 | 50* | | 110 | | 3.0 | | 2N711B | 8 |
| 2N1500 | PNP | | 50 | −15* | −50 | 100 | 20* | −50 | | | 5 | −5 | 2N960 | 8 |
| 2N1501 | PNP | | | −60* | | 95 | 25* | −2A | | | −2 | −60 | | |
| 2N1502 | PNP | | | −40* | | 95 | 25* | −2A | | | −2 | −40 | | |
| 2N1507 | NPN | | 0.6W | 60* | 500 | 175 | 100* | 150 | | | 1 | 30 | 2N711 | 8 |
| 2N1510 | NPN | Neon Indicator | 75 | 70 | 20 | 85 | 8* | 1 | | | 5 | 75 | 2N1510 | 3 |
| 2N1514 | NPN | | 2.5 | 100V | 8.0 Amps | 175 | 75* | | 1000 Kc | | 25 | 30 | 2N1924 | 2 |
| 2N1524 | PNP | | 80 | 24* | 10 | 85 | 60* | | 33.0 | | 16 | | 2N1924 | 2 |
| 2N1525 | PNP | | 80 | 24* | 10 | 85 | 60* | | 33.0 | | 16 | | 2N1925 | 2 |
| 2N1564 | NPN | | 1200 | 80* | 50 | 175 | 70 | | 40 | | 1.0 | | 2N698 | 4 |
| 2N1565 | NPN | | 1200 | 80* | 50 | 175 | 120 | | 50 | | 1.0 | | 2N699 | 4 |
| 2N1566 | NPN | | 1200 | 80* | 50 | 175 | 120 | | 50 | | 1.0 | | 2N699 | 4 |
| 2N1566A | NPN | | 600 | 80 | 100 | 200 | 125 | | 200 | | .50 | | 2N699 | 4 |
| 2N1572 | PNP | | 600 | 125 | | | 35 | | | | | | 2N698 | 4 |
| 2N1573 | PNP | | 600 | 125 | | | 70* | | | | | | 2N699 | 4 |
| 2N1574 | PNP | | 600 | 125 | | | 140* | | | | | | 2N699 | 4 |
| 2N1586 | NPN | | 150 | 15 | 25 | | 18 | | 4.0 | | | | 2N1276 | 4 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCB BVCB* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N1587 | NPN | | 150 | 30 | 25 | | 18 | | 4.0 | | | | 2N1276 | 4 |
| 2N1588 | NPN | | 150 | 60 | 25 | | 18 | | 4.0 | | | | 2N332 | 4 |
| 2N1589 | NPN | | 150 | 15 | 25 | | 50 | | 6.0 | | | | 2N1277 | 4 |
| 2N1590 | NPN | | 150 | 30 | 25 | | 50 | | 6.0 | | | | 2N1277 | 4 |
| 2N1591 | NPN | | 150 | 60 | 25 | | 50 | | 6.0 | | | | 2N334 | 4 |
| 2N1592 | NPN | | 150 | 15 | 25 | | 140 | | 7.0 | | | | 2N1279 | 4 |
| 2N1593 | NPN | | 150 | 30 | 25 | | 140 | | 7.0 | | | | 2N1279 | 4 |
| 2N1594 | NPN | | 150 | 60 | 25 | | 140 | | 7.0 | | | | 2N337 | 4 |
| 2N1605 | NPN | | 150 | 24 | 100 | 100 | 40* | 20 | 4 | | 5 | 12 | | |
| 2N1605A | NPN | | 200 | 40 | 100 | 100 | 60* | | 6.0 | | 10 | | | |
| 2N1613 | NPN-PL | Sw | 800 | 75 | | 200 | 80* | | 160 | | .01 | | 2N1613 | 4 |
| 2N1614 | PNP | Sw | 240 | −65* | −300 | 85 | 18* | −20 | 0.5 | | −25 | −65 | 2N1614 | 1 |
| 2N1624 | NPN | | 150 | 25 | | 100 | 120* | | 8.0 | | 10 | | 2N634A | 2 |
| 2N1644 | NPN | | 600 | 60 | | 175 | 75* | | 150 | | 1.0 | | 2N697 | 4 |
| 2N1644A | NPN | | 600 | 60* | | 175 | 75* | | 150 | | 1.0 | | 2N697 | 4 |
| 2N1646 | PNP | | 150 | 15* | | 100S | 20* | | | | 3.0 | | | |
| 2N1671 | PN | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N1671 | 5 |
| 2N1671A | PN | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N1671A | 5 |
| 2N1671B | PN | Si Uni | SEE G-E FAMILY OF SPECIFICATIONS SECTION | | | | | | | | | | 2N1671B | 5 |
| 2N1672 | NPN | | 120 | 40* | | | 50 | | 2.0 | | 25 | | 2N1302 | 2 |
| 2N1672A | NPN | | 120 | 40* | | 85 | 20* | | 2.0 | | | | 2N634A | 2 |
| 2N1684 | PNP | | 100 | 25* | 100 | 100 | | | 8.0 | | 20 | | 2N397 | 2 |
| 2N1694 | NPN | | 75 | 20* | 25 | 85S | 30* | | 9.0 | | 1.5 | | 2N1694 | 2 |
| 2N1700 | NPN | | 5000 | 60* | 1.0 Amp | 200 | 20 | | 1.20 | | 75 | | 2N656A | 2 |
| 2N1705 | PNP | | 200 | 18* | 400 | 100 | 110 | | 4.0 | | 10 | | 2N527 | 2 |
| 2N1706 | PNP | | 200 | 25* | 400 | 100 | 90 | | 3.0 | | 10 | | 2N527 | 2 |
| 2N1707 | PNP | | 200 | 30* | 400 | 100 | 95 | | 3.0 | | 15 | | 2N527 | 2 |
| 2N1711 | NPN | | 800 | 30* | 500 | 175 | 35 | | 230 | | | | 2N1711 | 4 |
| 2N1714 | NPN | | 7.5 | 90 | 1.0 Amp | 175 | | | 16 | | | | 7D2 | 11 |
| 2N1715 | NPN | | 7.5 | 150 | 1.0 Amp | 175 | | | 16 | | | | 7D4 | 11 |
| 2N1716 | NPN | | 7.5 | 90 | 1.0 Amp | 175 | | | 16 | | | | 7D13 | 11 |
| 2N1717 | NPN | | 7.5 | 150 | 1.0 Amp | 175 | | | 16 | | | | 7D4 | 11 |
| 2N1718 | NPN | | 7.5 | 90 | 1.0 Amp | 175 | | | 16 | | | | 7G2 | |
| 2N1719 | NPN | | 7.5 | 150 | 1.0 Amp | 175 | | | 16 | | | | 7G4 | |
| 2N1720 | NPN | | 7.5 | 90 | 1.0 Amp | 175 | | | 16 | | | | 7G13 | |
| 2N1721 | NPN | | 7.5 | 150 | 1.0 Amp | 175 | | | 16 | | | | 7G4 | |
| 2N1726 | PNP | | 60 | 20 | 50 | 100 | 120* | | 150 | | | | 2N964 | 8 |
| 2N1727 | PNP | | 60 | 20 | 50 | 100 | 150* | | 150 | | | | 2N960 | 8 |
| 2N1728 | PNP | | 60 | 20 | 50 | 100 | 100* | | 150 | | | | 2N960 | 8 |
| 2N1754 | PNP | | 50 | 13* | 100 | 85 | 50* | | 75 | | | | 2N711A | 8 |
| 2N1779 | NPN | | 100 | 25* | 100 | 100 | 40* | | 5.0 | | 10 | | 2N634A | 2 |
| 2N1780 | NPN | | 100 | 25* | 100 | 100 | 40* | | 8.0 | | 10 | | 2N634A | 2 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVCE BVCB* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ VCB | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N1781 | NPN | | 100 | 25* | 100 | 100 | 60* | | 6.0 | | 20 | | 2N634A | 2 |
| 2N1785 | PNP | | 45 | 10* | 50 | 85 | 60* | | 125 | | 10 | | 2N966 | 8 |
| 2N1786 | PNP | | 45 | 10* | 50 | 85 | 60* | | 125 | | 10 | | 2N962 | 8 |
| 2N1787 | PNP | | 45 | 15* | 50 | 85 | 60* | | 125 | | 10 | | 2N960 | 8 |
| 2N1808 | NPN | | 150 | 25* | 300 | 100S | 60* | | 4.0 | | 5.0 | | 2N634A | 2 |
| 2N1889 | NPN-PL | | 800 | 100* | | 200J | 70* | | 110 | | .01 | | | |
| 2N1890 | NPN-PL | | 800 | 100* | | 200J | 120* | | 130 | | .01 | | | |
| 2N1893 | NPN-PL | Sw | 800 | 120* | | 200J | 85* | | 110 | | .01 | | 2N1893 | 4 |
| 2N1924 | PNP | AF | 225 | −60* | −500 | 85 | 30* | −100 | 1.0 | | −10 | 45 | 2N1924 | 2 |
| 2N1925 | PNP | AF | 225 | −60* | −500 | 85 | 47* | −100 | 1.3 | | −10 | 45 | 2N1925 | 2 |
| 2N1926 | PNP | AF | 225 | −60* | −500 | 85 | 65* | −100 | 1.5 | | −10 | 45 | 2N1926 | 2 |
| 2N1954 | PNP | | 200 | 60* | 1.0 Amp | 100J | 120 | | | | 20 | | 2N1926 | 2 |
| 2N1955 | PNP | | 200 | 60* | 1.0 Amp | 100J | 200 | | | | 20 | | 2N1926 | 2 |
| 2N1956 | PNP | | 200 | 60* | 1.0 Amp | 100J | 120 | | | | 20 | | 2N1926 | 2 |
| 2N1958 | NPN | | 600 | 60* | 500 | 175 | 45 | | | | .50 | | 2N2194A | 4 |
| 2N1959 | NPN | | 600 | 60* | 500 | 175 | 80 | | | | .50 | | 2N2193A | 4 |
| 2N1960 | PNP | | 150 | 15* | 200 | 100 | 25 | | | | 3.0 | | 2N781 | 8 |
| 2N1961 | PNP | | 150 | 12* | 200 | 100 | 20 | | | | 3.0 | | 2N782 | 8 |
| 2N1969 | PNP | | 150 | 30* | 400 | 100 | 125 | | 10 | | 5.0 | | 2N1307 | 2 |
| 2N1973 | PNP | | 800 | 100* | | 200J | 100 | | 60 | | .025 | | | |
| 2N1974 | PNP | | 800 | 100* | | 200J | 50 | | 50 | | .025 | | | |
| 2N1975 | PNP | | 800 | 100* | | 200J | 30 | | 40 | | .025 | | | |
| 2N1986 | NPN | | 600 | 50* | | 150J | 150* | | 50.0 | | 5.0 | | 2N697 | 4 |
| 2N1987 | NPN | | 600 | 50* | | 150J | 50* | | 50.0 | | 5.0 | | 2N696 | 4 |
| 2N1997 | PNP | | 250 | 45* | 500 | 100S | 75* | | 3.0 | | 6.0 | | 2N527 | 2 |
| 2N1998 | PNP | | 250 | 35* | 500 | 100S | 100* | | 6.50 | | 6.0 | | 2N527 | 2 |
| 2N2022 | PNP | | 150 | 15* | 50 | 100J | 35 | | | | 3.0 | | 2N828 | 8 |
| 2N2042 | PNP | | 200 | 105* | | | 50 | | .50 | | | | 2N1925 | 2 |
| 2N2042A | PNP | | 200 | 105* | 200 | 100 | 50 | | .50 | | 25 | | 2N1925 | 2 |
| 2N2043 | PNP | | 200 | 105* | | | 113 | | .75 | | | | 2N1926 | 2 |
| 2N2043A | PNP | | 200 | 105* | 200 | 100 | 113 | | .75 | | 25 | | 2N1926 | 2 |
| 2N2049 | NPN-PL | | 800 | 75* | | 200J | 60* | | 50 | | .01 | | | |
| 2N2060 | NPN-PL | | 500 | 100* | | 200J | 35* | | | | 2.0 | | 2N2060 | 8 |
| 2N2085 | NPN | | 150 | 33* | 500 | 100 | 100 | | 8.0 | | 5.0 | | 2N635A | 2 |
| 2N2086 | NPN | | 600 | 120* | 500 | 300S | 70* | | 225 | | 2.0 | | 2N2194 | 4 |
| 2N2087 | NPN | | 600 | 120* | 500 | 300S | 65* | | 225 | | 2.0 | | 2N2193 | 4 |
| 2N2106 | NPN-M | AF | 125 | 60* | | 150J | | | 15MC | | .20 | 30 | 2N2106 | 2 |
| 2N2107 | NPN-M | AF | 125 | 60* | | 150J | | | 15MC | | .20 | 30 | 2N2107 | 2 |
| 2N2108 | NPN-M | AF | 125 | 60* | | 150J | | | 15MC | | .20 | 30 | 2N2108 | 2 |
| 2N2169 | PNP | | 60 | 15* | | 100S | 85* | | | | 3.0 | | 2N781 | 8 |
| 2N2192 | NPN-PEP | Sw | 800 | 60 | 1.0 Amp | 300S | 100* | 150 | | | 10 mμa | 30 | 2N2192 | 4 |
| 2N2192A | NPN-PEP | Sw | 800 | 60 | 1.0 Amp | 300S | 100* | 150 | | | 10 mμa | 30 | 2N2192A | 4 |

| JEDEC No. | Type | Use | MAXIMUM RATINGS Pc mw @ 25°C | BVce BVcb* | Ic ma | TJ°C | ELECTRICAL PARAMETERS MIN. hfe-hFE* | @ Ic ma | MIN. fhfb mc | MIN. Ge db | MAX. Ico (μa) | @ Vcb | Closest GE | Dwg. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N2193 | NPN-PEP | Sw | 800 | 80 | 1.0 Amp | 300S | 40* | 150 | | | 10 mμa | 30 | 2N2193 | 4 |
| 2N2193A | NPN-PEP | Sw | 800 | 80 | 1.0 Amp | 300S | 40* | 150 | | | 10 mμa | 30 | 2N2193A | 4 |
| 2N2194 | NPN-PEP | Sw | 800 | 60 | 1.0 Amp | 300S | 20* | 150 | | | 10 mμa | 30 | 2N2194 | 4 |
| 2N2194A | NPN-PEP | Sw | 800 | 60 | 1.0 Amp | 300S | 20* | 150 | | | 10 mμa | 30 | 2N2194A | 4 |
| 2N2195 | NPN-PEP | Sw | 600 | 45 | 1.0 Amp | 300S | 20* | 150 | | | 100 mμa | 60 | 2N2195 | 4 |
| 2N2195A | NPN-PEP | Sw | 600 | 45 | 1.0 Amp | 300S | 20* | 150 | | | 100 mμa | 60 | 2N2195A | 4 |
| 2N2196 | NPN | Power | 2W | 80* | | 175 | 10* | | 15T | | 75 | 80 | 2N2196 | 9 |
| 2N2197 | NPN | Power | 2W | 80* | | 175 | 20* | | 15T | | 75 | 80 | 2N2197 | 9 |
| 2N2201 | NPN | Power | 15W | 120* | | 175J | 30* | | 15MC | | 50 | 120 | 2N2201 | 9 |
| 2N2202 | NPN | Power | 15W | 120* | | 175J | 30* | | 15MC | | 50 | 120 | 2N2202 | 10 |
| 2N2203 | NPN | Power | 15W | 120* | | 175J | 30* | | 15MC | | 50 | 120 | 2N2203 | 11 |
| 2N2204 | NPN | Power | 15W | 120* | | 175J | 30* | | 15MC | | 50 | 120 | 2N2204 | 12 |
| 4D20 | NPN | Sw | 150 | 40* | 25 | 150J | 33* | | | 1.0 | | | 4D20 | 4 |
| 4D21 | NPN | Sw | 150 | 40* | 25 | 150J | 88* | | | 1.0 | | | 4D21 | 4 |
| 4D22 | NPN | Sw | 150 | 40* | 25 | 150J | 185* | | | 1.0 | | | 4D22 | 4 |
| 4D24 | NPN | Sw | 125 | 15* | 25 | 125J | 33* | | | 1.0 | | | 4D24 | 4 |
| 4D25 | NPN | Sw | 125 | 15* | 25 | 125J | 88* | | | 1.0 | | | 4D25 | 4 |
| 4D26 | NPN | Sw | 125 | 15* | 25 | 125J | 133* | | | 1.0 | | | 4D26 | 4 |
| 4C28 | NPN | Sw | 150 | 40* | 25 | 125J | 15 | | 12.0 | 2.0 | | | 4C28 | 4 |
| 4C29 | NPN | Sw | 150 | 40* | 25 | 125J | 30 | | 12.0 | 2.0 | | | 4C29 | 4 |
| 4C30 | NPN | Sw | 150 | 40* | 25 | 125J | 55 | | 12.0 | 2.0 | | | 4C30 | 4 |
| 4C31 | NPN | Sw | 150 | 40* | 25 | 125J | 115 | | 12.0 | 2.0 | | | 4C31 | 4 |
| 7B1 | NPN | Power | 15W | 80* | | 175 | 12* | | 15T | | 50 | 80 | 7B1 | 9 |
| 7C1 | NPN | Power | 15W | 80* | | 175 | 12* | | 15T | | 50 | 80 | 7C1 | 10 |
| 7D1 | NPN | Power | 15W | 80* | | 175 | 12* | | 15T | | 50 | 80 | 7D1 | 11 |
| 7E1 | NPN | Power | 15W | 80* | | 175 | 12* | | 15T | | 50 | 80 | 7E1 | 12 |
| 7F1 | NPN | Power | 7W | 80* | | 175 | 12* | | 15T | | 50 | 80 | 7F1 | 13 |
| 7B2 | NPN | Power | 15W | 80* | | 175 | 30* | | 15T | | 50 | 80 | 7B2 | 9 |
| 7C2 | NPN | Power | 15W | 80* | | 175 | 30* | | 15T | | 50 | 80 | 7C2 | 10 |
| 7D2 | NPN | Power | 15W | 80* | | 175 | 30* | | 15T | | 50 | 80 | 7D2 | 11 |
| 7E2 | NPN | Power | 15W | 80* | | 175 | 30* | | 15T | | 50 | 80 | 7E2 | 12 |
| 7F2 | NPN | Power | 7W | 80* | | 175 | 30* | | 15T | | 50 | 80 | 7F2 | 13 |
| 7B3 | NPN | Power | 15W | 120* | | 175 | 12* | | 15T | | 50 | 120 | 7B3 | 9 |
| 7C3 | NPN | Power | 15W | 120* | | 175 | 12* | | 15T | | 50 | 120 | 7C3 | 10 |
| 7D3 | NPN | Power | 15W | 120* | | 175 | 12* | | 15T | | 50 | 120 | 7D3 | 11 |
| 7E3 | NPN | Power | 15W | 120* | | 175 | 12* | | 15T | | 50 | 120 | 7E3 | 12 |
| 7F3 | NPN | Power | 7W | 120* | | 175 | 12* | | 15T | | 50 | 120 | 7F3 | 13 |

## ABBREVIATIONS

AF—Audio Frequency Amplifier and General Purpose
AF Out—High current AF Output
AF Sw—Low frequency switch
GD—Grown Diffused
IF—Intermediate Frequency Amplifier
J—Operating Junction Temperature
lo IF—Low IF (262 Kc) Amplifier
NPN-A—NPN Alloyed
NPN-D—NPN Diffused
NPN-EM—NPN Epitaxial Mesa
NPN-FA—NPN Fused Alloyed
NPN-G—NPN Grown
NPN-GD—NPN Grown Diffused
NPN-M—NPN Mesa
NPN-PL—NPN Planar
NPN-PEP—NPN Planar Epitaxial Passivated
NPN-PM—NPN Planar Epitaxial Mesa
Osc—High gain High frequency RF oscillator
PNP-A—PNP Alloyed
PNP-D—PNP Diffused
PNP-EM—PNP Epitaxial Mesa
PNP-M—PNP Mesa
PNP-MD—PNP Micro-Alloyed Diffused
Pt—Point contact types
Pwr—Power output 1 watt or more
RF—Radio Frequency Amplifier
S—Storage Temperature
Si—Silicon High Temperature Transistors (all others germanium)
Sw—High current High frequency switch
T—Typical Values
UNI—Unijunction Transistor

**NOTE:** *Closest GE types* are given only as a general guide and are based on available published electrical specifications. However, General Electric Company makes no representation as to the accuracy and completeness of such information. Since manufacturing techniques are not identical, the General Electric Company makes no claim, nor does it warrant, that its transistors are exact equivalents or replacements for the types referred to.

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